North South University

Department of Electrical & Computer Engineering

LAB REPORT- 03

Course Code: **EEE141L**

Course Title: **Electrical Circuits Lab**

Section: **07**

Lab Number: **03**

Experiment Name:

Loading Effect of Voltage Divider Circuit

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Submitted by Group Number: **02**

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1. **Experiment Name:** Loading Effect of Voltage Divider Circuit

2. **Objective:**
   - To analyse the behaviour of a voltage divider circuit in the absence of a load resistor and evaluate the output voltage (V_{out}) under different load conditions.
   - To investigate the loading effect of the voltage divider circuit and assess its impact on V_{out}.
   - To compare theoretical predictions with practical measurements of V_{out} and analyse the accuracy of the voltage divider circuit model.

3. **Theory:**

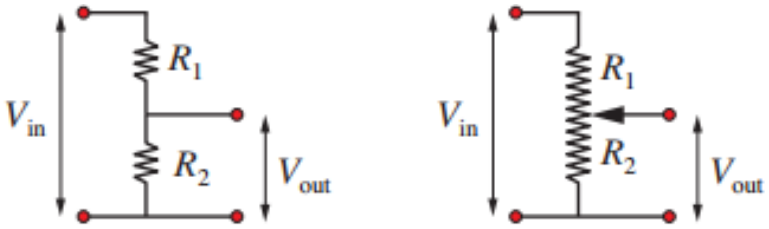


Figure 1: A voltage divider on the left, and potentiometer on the right.

The voltage divider circuit operates based on the principle of proportionality, as described by the Voltage Divider Rule. According to this rule, the output voltage (V_{out}) across one of the resistors (R_2) is determined by the ratio of its resistance to the total resistance of the series combination of resistors (R_1 and R_2). Mathematically, the Voltage Divider Rule is expressed as:

$$V_{out} = V_{in} \times \frac{R_2}{R_1 + R_2}$$

Where:

- V_{out} = Output voltage across R2R2
- V_{in} =Input voltage
- R_1= Resistance of the first resistor
- R_2= Resistance of the second resistor

When there is no load resistor connected (No-Load circuit), the output voltage is solely determined by the resistance ratio between R_1 and R_2. In this scenario, adjusting the value of R_2 (e.g., using a potentiometer) enables the manipulation of the output voltage within the range of 0 to V_{in}.

However, when a load resistor (R_L) is introduced in parallel to R_2, the effective resistance seen by R_2changes due to the parallel combination of R_2 and R_L. In this scenario, the output voltage is calculated using the modified voltage divider formula:

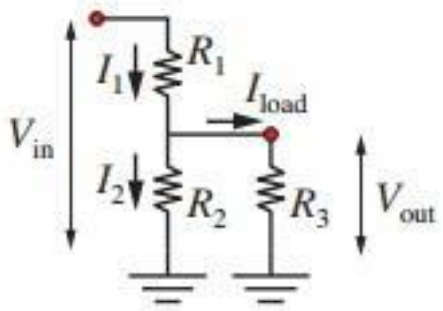
$$V_{out} = V_{in} \frac{R_2 || R_L}{R_1 + (R_2 || R_L)}$$

Where:

$R_2 \| R_L$ represents the parallel combination of R_2 and R_L calculated as $\frac{R_2 \times R_L}{R_2 + R_L}$

This equation accounts for the loading effect caused by the additional current drawn by the load resistor R_L. As R_L decreases, the effective resistance across R_2 decreases, resulting in a larger current flow and a reduction in the output voltage. Conversely, increasing R_L leads to a higher effective resistance across R_2, mitigating the loading effect and allowing for a closer approximation to the desired output voltage.

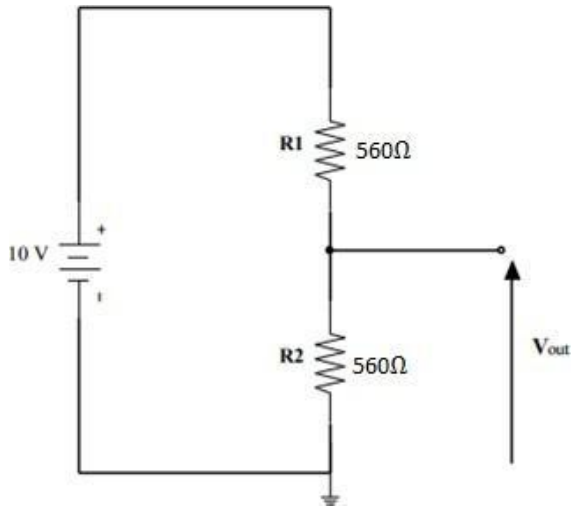
In practical circuit design, minimizing the loading effect is crucial for maintaining accurate voltage division and ensuring the proper functioning of the voltage divider circuit. This often involves selecting a load resistor with a much larger value than the parallel combination of R_2 and R_L, thereby minimizing the impact of the load on the output voltage. Additionally, careful consideration of component tolerances and circuit impedance can further optimize the performance of the voltage divider circuit in real-world applications.



4. Apparatus List:

Name	Quantity
Trainer Board	1
MM (Digital Multi meter)	1
560Ω Resistors	2
Variable Resistor (0-10kΩ)	1

5. **Circuit diagram:**



6. **Experimental Procedure:**
    - Construct the voltage divider circuit according to the provided circuit diagram.
    - Measure the unloaded output voltage (Vout) using the DMM and record the value.
    - Connect a 10kΩ variable load resistor in parallel with R_2 of the circuit.
    - Adjust the variable resistor to different resistance values (1kΩ, 4kΩ, 7kΩ, and 10kΩ).
    - Record the corresponding values of Vout for each load resistor value.

7. Results:

Table 1:

R_L	V_{out} (Measured)	V_{out} (Calculated)	%Error
No resistor	5.02 V	5 V	0.40%
1k	3.94 V	3.91 V	0.77%
4k	4.69 V	4.67 V	0.43%
7k	4.84 V	4.81 V	0.62%
10k	4.88 V	4.86 V	0.41%

8. Question/Answer:

- Explain the loading effect of our circuit:

  The loading effect of the circuit refers to the deviation of the measured output voltage (V_{out}) from the calculated or expected value due to the presence of an external load resistor (R_L). As R_L is connected in parallel to the output resistor (R_2), it alters the effective resistance seen by R_2, thereby affecting the voltage division across the circuit. This results in a decrease in

Vout compared to the ideal value calculated without the presence of a load resistor. From the provided data, we observe that the measured Vout is slightly lower than the calculated Vout for all load resistor values, indicating a consistent loading effect across different load conditions

- Theoretically calculate the value of V_{out} for each load resistor:

For no resistor we know that if the resistors are same then the voltage would be divided in half, so for that the V_{out} would be 5V.

$$for\ 1k, \quad V_{out} = V_{in} \frac{R_L}{R_1+R_L} = 10v \times \frac{358.97\Omega}{560\Omega+358.97\Omega} = 3.91v$$

Where,

$$R_L = R_2||R_L = \frac{R_2 \times R_L}{R_2+R_L} = \frac{560\Omega \times 1000\Omega}{560\Omega+1000\Omega} = 358.97\Omega$$

$$for\ 4k, \quad V_{out} = V_{in} \frac{R_L}{R_1+R_L} = 10v \times \frac{491.23\Omega}{560\Omega+491.23\Omega} = 4.67v$$

Where,

$$R_L = R_2||R_L = \frac{R_2 \times R_L}{R_2+R_L} = \frac{560\Omega \times 4000\Omega}{560\Omega+4000\Omega} = 491.23\Omega$$

$$for\ 7k, \quad V_{out} = V_{in} \frac{R_L}{R_1+R_L} = 10v \times \frac{518.52\Omega}{560\Omega+518.52\Omega} = 4.81v$$

Where,

$$R_L = R_2||R_L = \frac{R_2 \times R_L}{R_2+R_L} = \frac{560\Omega \times 7000\Omega}{560\Omega+7000\Omega} = 518.52\Omega$$

$$for\ 10k, \quad V_{out} = V_{in}\frac{R_L}{R_1+R_L} = 10v \times \frac{530.3\Omega}{560\Omega+530.3\Omega} = 4.86v$$

Where,

$$R_L = R_2||R_L = \frac{R_2 \times R_L}{R_2+R_L} = \frac{560\Omega \times 10000\Omega}{560\Omega+10000\Omega} = 530.3\Omega$$

- Comparison of theoretical and experimental data:

$$\%Error = \left|\frac{V_{measured}-V_{calculated}}{V_{calculated}}\right| \times 100\%$$

So,

$$for\ 1k,\ \%Error = \left|\frac{3.94v-3.91v}{3.91v}\right| \times 100\% = 0.77\%$$
$$for\ 4k,\ \%Error = \left|\frac{4.69v-4.67v}{4.67v}\right| \times 100\% = 0.43\%$$
$$for\ 7k,\ \%Error = \left|\frac{4.84v-4.81v}{4.81v}\right| \times 100\% = 0.62\%$$
$$for\ 10k,\ \%Error = \left|\frac{4.88v-4.86v}{4.86v}\right| \times 100\% = 0.41\%$$

9. Discussion:

10.

In this experiment, we investigated the loading effect of a voltage divider circuit by comparing theoretical calculations with practical measurements of the output voltage (V_{out}) under various load resistor conditions.

- Comparison of Theoretical and Practical Values:

The comparison between theoretical and practical values of V_{out} revealed a close agreement between the two sets of data. The theoretical calculations, based on the modified voltage divider formula, accurately predicted the behaviour of the circuit under different load conditions. Despite minor discrepancies, the percentage error remained within acceptable limits, ranging from 0.40% to 0.77%. This indicates that the theoretical model effectively captures the loading effect of the circuit.

- Evaluation of the Loading Effect:

  The loading effect, characterized by a decrease in V_{out} with increasing load resistor (R_L), was observed consistently across all experimental measurements. As expected, the measured V_{out} was slightly lower than the calculated V_{out} for each load resistor value. This discrepancy is attributed to the additional current drawn by the load resistor, which alters the voltage division across the circuit. However, the observed deviation from theoretical predictions was relatively small, highlighting the overall effectiveness of the voltage divider circuit design.

- Dentification of Experimental Challenges:

  Several challenges were encountered during the experiment that may have influenced the accuracy of the results. One notable issue was the precision of the resistance values of the physical resistors used in the circuit. Variations in resistor tolerance and measurement errors could have introduced uncertainties in the calculated V_{out} values. Additionally, factors such as stray capacitance and inductance in the circuit layout may have contributed to minor deviations from theoretical predictions.

- Recommendations for Improvement:

  To enhance the accuracy and reliability of future experiments, several measures can be implemented. Using resistors with tighter tolerance specifications and carefully calibrating measurement instruments can minimize errors in resistance values and voltage measurements. Furthermore, attention to circuit layout and shielding techniques can help

reduce the influence of stray capacitance and inductance, ensuring more accurate experimental results.