Project 1 Report

Course Title: VLSI System Design
Course Code: EECE-6375

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The University of Texas Rio Grande Valley

Table of Contents

Part A:

Specification 2.5 (NMOS W/L)=(PMOS W/L)

Explain: Why?

Ans:

Because PMOS holes are less mobile than NMOS electrons, the PMOS transistor is larger than the NMOS transistor in CMOS design. An NMOS can conduct current more effectively and switch more quickly because electron mobility is roughly two to three times greater than hole mobility. The PMOS is given a wider channel, usually two to 2.5 times the width of the NMOS, to compensate for this discrepancy and guarantee that both transistors provide an equal current drive strength. By achieving symmetrical rise and fall times during switching, this sizing contributes to stable logic levels, equal propagation delays, and effective circuit performance overall.

Part B:

TABLE 1:

Gate Type	Wn	Wp	L	RT	FT	DELAY	Frequency (GHz)	SIZE / AREA
NOR	2 µm	5 µm	180 nm (0.18 µm)	41.09ps	37.88ps	20.758ps	48.17	190.38 µm²
NAND	2 µm	5 µm	180 nm (0.18 µm)	27.82 ps	92.34 ps	20.787ps	48.787	166.21875 µm²
XOR	2 µm	5 µm	180 nm (0.18 µm)	79.44 ps	70.18 ps	20.767ps	48.153	842.333µm²

Part C: NOR GATE Layout

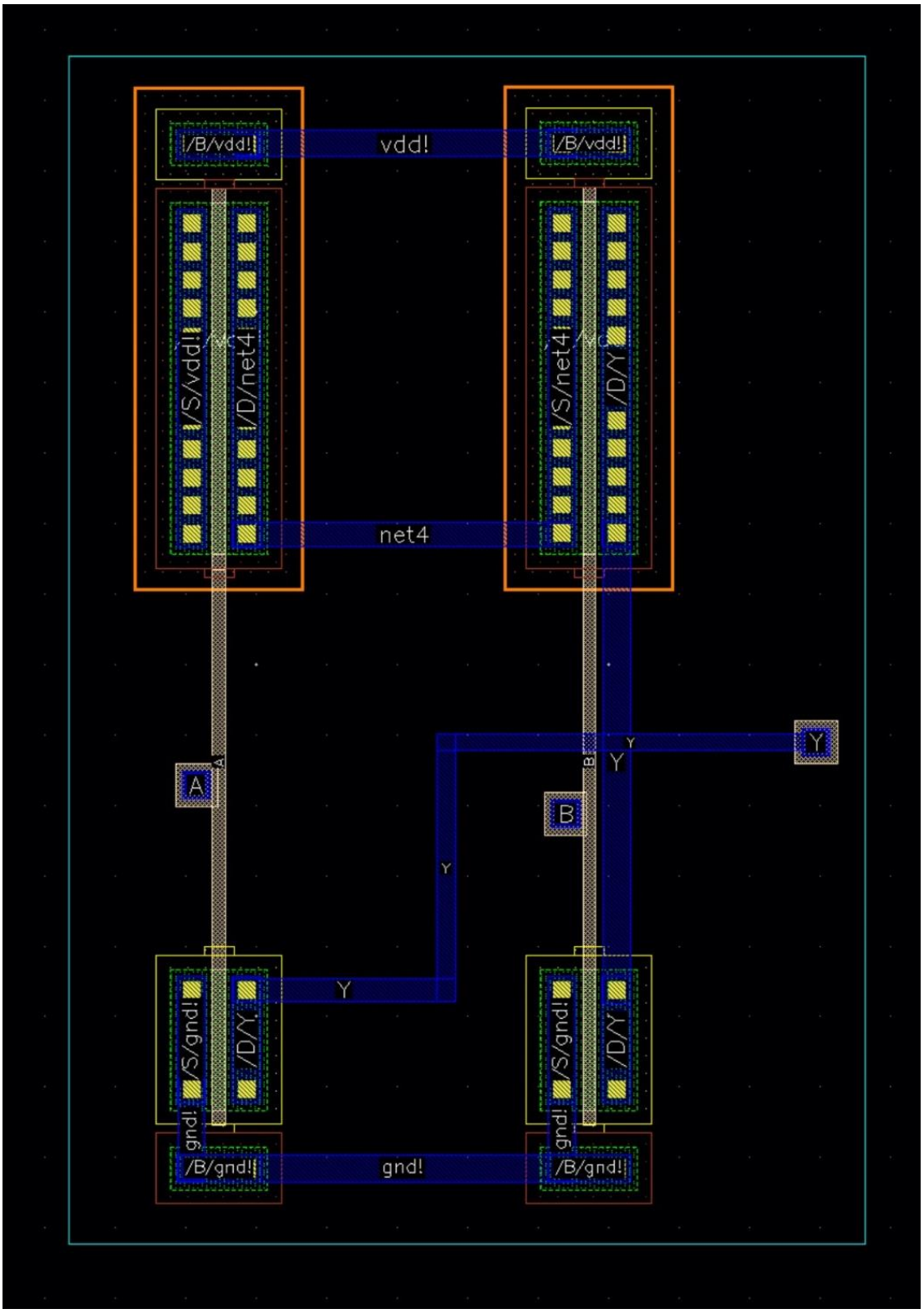

Fig.1: Layout NOR

Part C: Input-output waveforms (Truth table: 2 combinations)_NOR

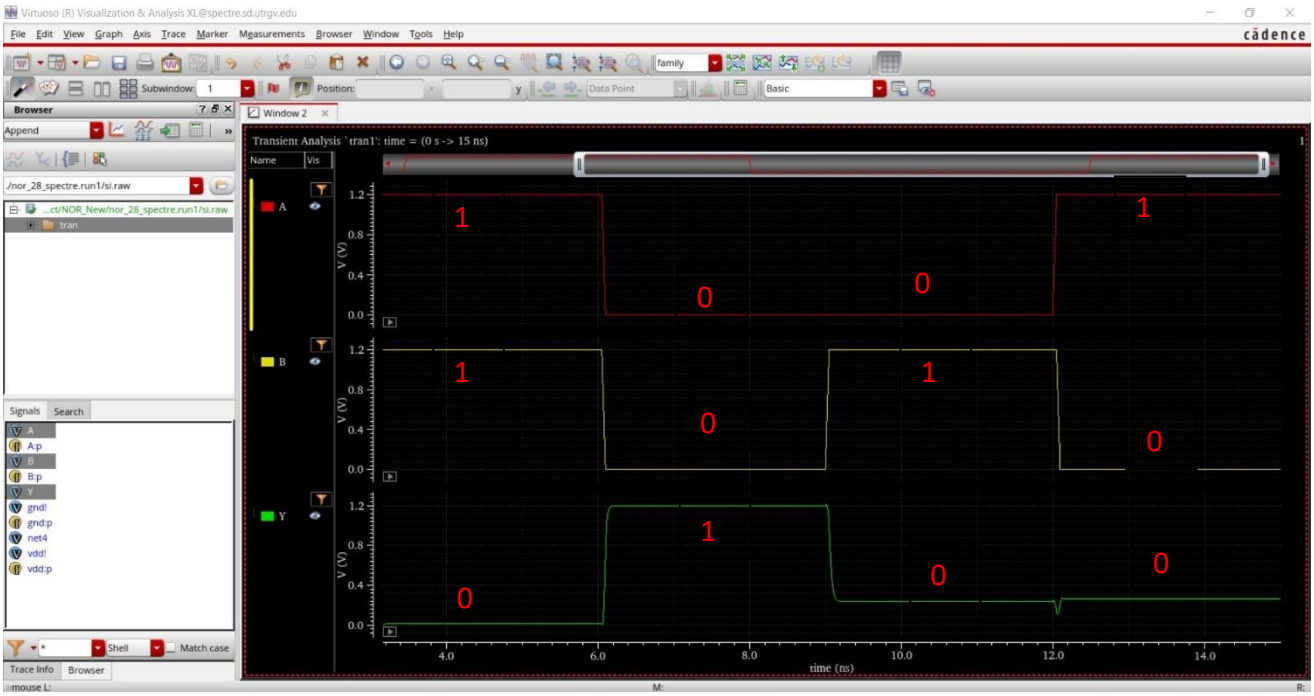

Fig.2: Input-output waveforms (Truth table: 2 combinations) of NOR Gate

Part C: Si.inp files (spectre simulation) NOR

```
// Generated for: spectre
// Generated on: Oct 28 13:42:54 2025
// Design library name: NOR_GATE
// Design cell name: NOR_GATE
// Design view name: schematic
simulator lang=spectre
global 0 vdd!

include "/home/blx188/Spectre-Models/standalone/ami06N.m"
include "/home/blx188/Spectre-Models/standalone/ami06P.m"

// Library name: NOR_GATE
// Cell name: NOR_GATE
// View name: schematic
PM1 (Y B net4 vdd!) ami06P w=(5u) l=180n as=3p ad=3p ps=11.2u pd=11.2u \
    m=(1)*(1)
PM0 (net4 A vdd! vdd!) ami06P w=(5u) l=180n as=3p ad=3p ps=11.2u pd=11.2u \
    m=(1)*(1)
NM1 (Y B 0 0) ami06N w=(2u) l=180n as=1.2p ad=1.2p ps=5.2u pd=5.2u \
    m=(1)*(1)
NM0 (Y A 0 0) ami06N w=(2u) l=180n as=1.2p ad=1.2p ps=5.2u pd=5.2u \
    m=(1)*(1)

// Spectre Source Statements
vdd (vdd! 0) vsource dc=1.2
gnd (gnd! 0) vsource dc=0
parameters vhi=1.2 tr=50p tf=50p
A (A 0) vsource type=pulse val0=0 val1=vhi rise=tr fall=tf delay=0 width=6n period=12n
B (B 0) vsource type=pulse val0=0 val1=vhi rise=tr fall=tf delay=3n width=3n period=6n
```

```
// Spectre Analyses and Output Options Statements
// Output Options
simOptions options
//+     reltol = 1.00000000E-03
//+     vabstol = 1.00000000E-06
//+     iabstol = 1.00000000E-12
//+     temp = 27
//+     save = allpub
//+     currents = selected
// Analyses
// dc1 dc oppoint=logfile homotopy=all
// tran1 tran stop=1 errpreset=moderate
tran1 tran start=0 stop=15n step=0.1n errpreset=moderate


// End of Netlist
```

Part C: Schematic NOR

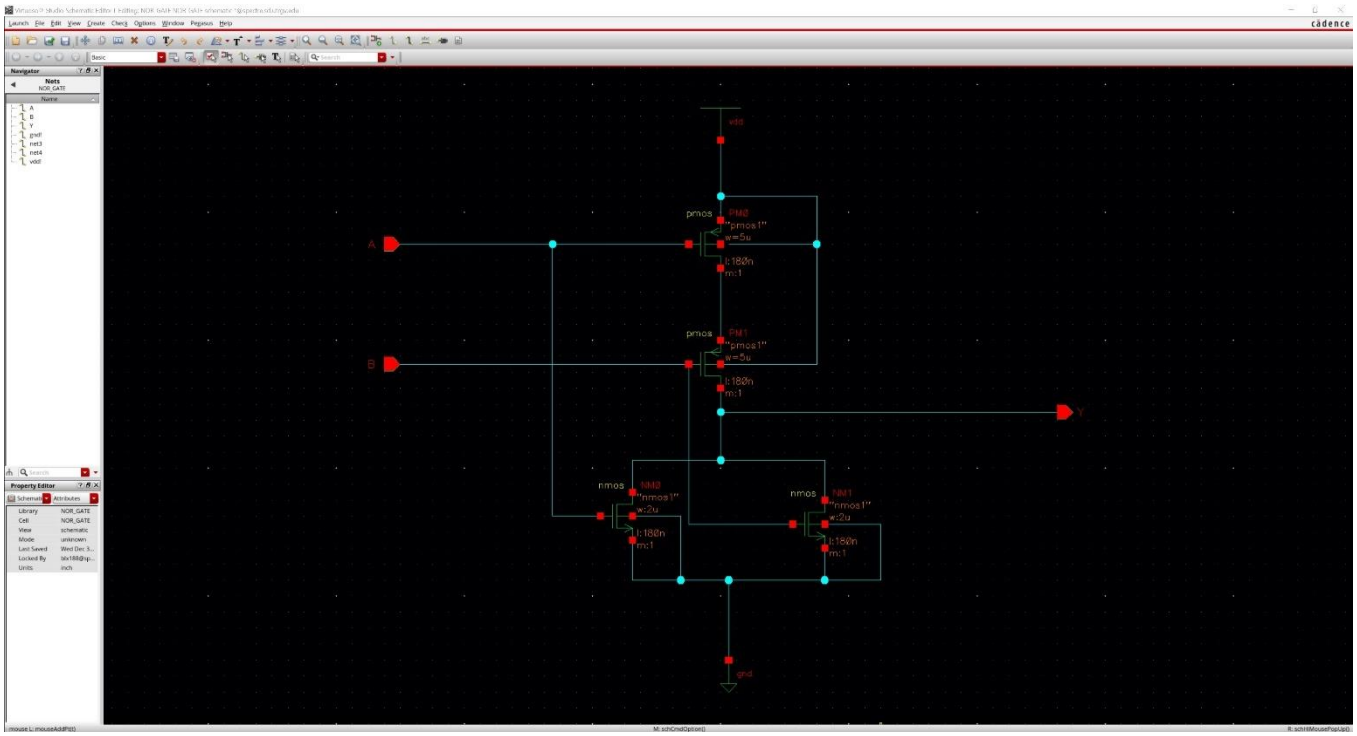

Fig.3: Circuit Schematic NOR

Part C: Symbol NOR

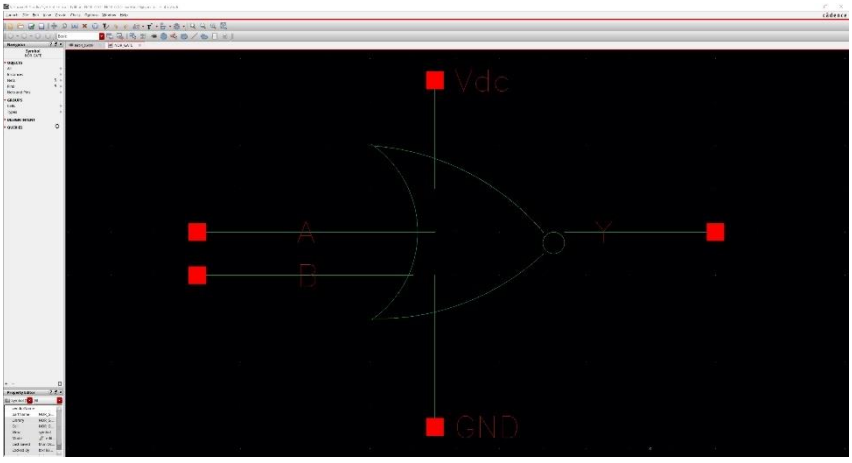

Fig.4: Symbol NOR

Part D: Layout NAND

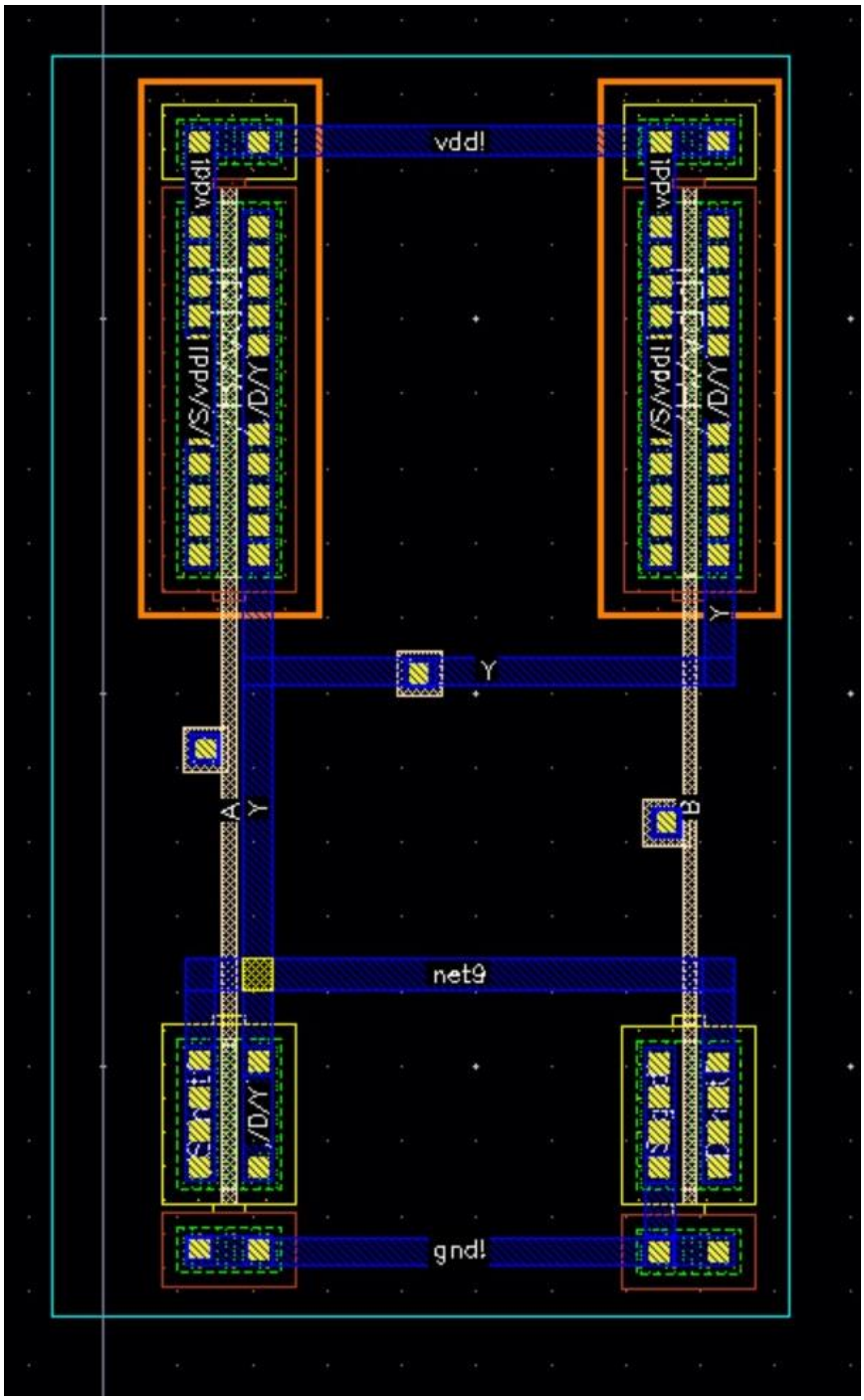

Fig.5: Layout NAND

Part D: Input-output waveforms (Truth table: 4 combinations)

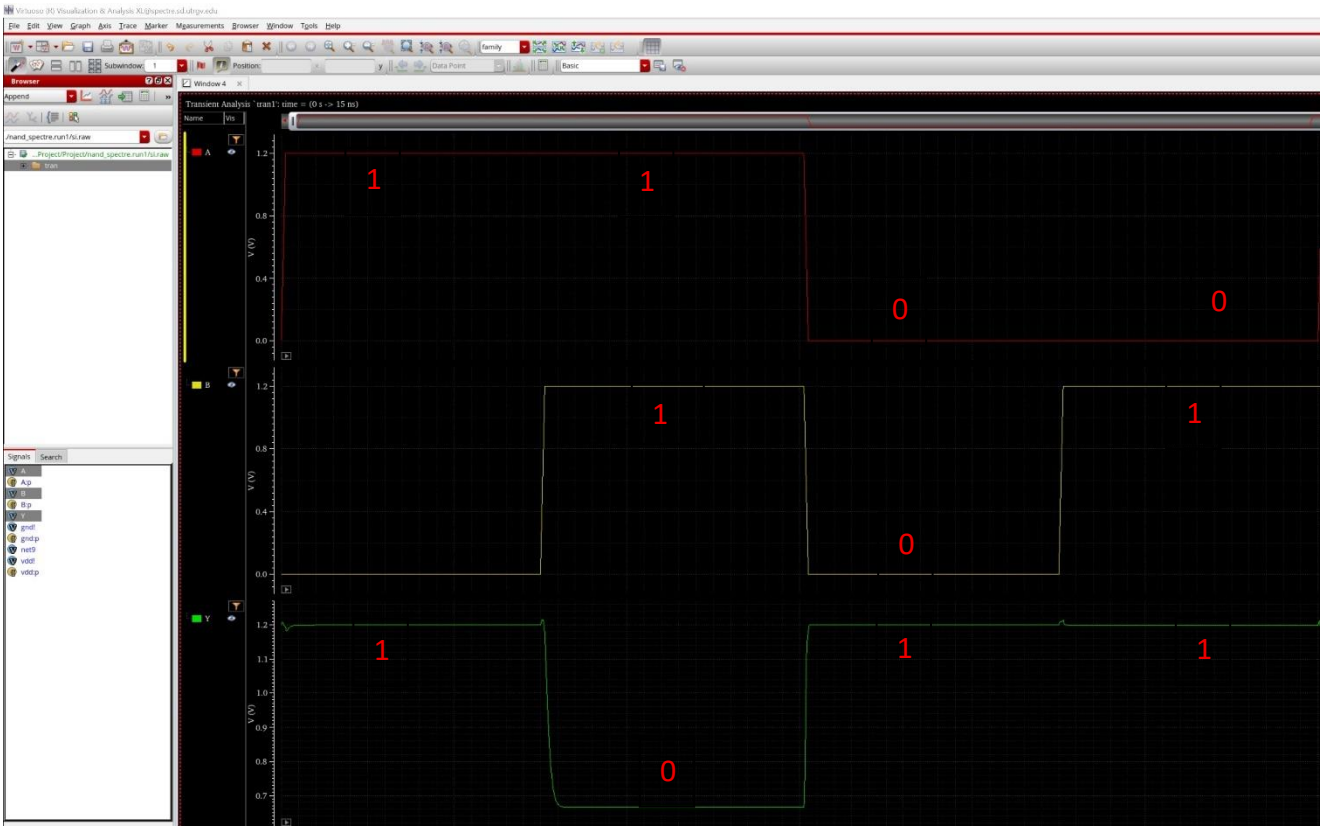

Fig.6: Simulation Output NAND

Part D: Si.inp files (spectre simulation) NAND

```
// Generated for: spectre
// Generated on: Oct 27 21:45:23 2025
// Design library name: NAND
// Design cell name: NAND_Gate
// Design view name: schematic
simulator lang=spectre
global 0 vdd!

include "/home/blx188/Spectre-Models/standalone/ami06N.m"
include "/home/blx188/Spectre-Models/standalone/ami06P.m"

// Library name: NAND
// Cell name: NAND_Gate
// View name: schematic
PM0 (Y B vdd! vdd!) ami06P w=(5u) l=180n as=3p ad=3p ps=11.2u pd=11.2u \
    m=(1)*(1)
ami06P (Y A vdd! vdd!) ami06P w=(5u) l=180n as=3p ad=3p ps=11.2u pd=11.2u \
    m=(1)*(1)
NM0 (net9 B 0 0) ami06N w=(2u) l=180n as=1.2p ad=1.2p ps=5.2u pd=5.2u \
    m=(1)*(1)
ami06N (Y A net9 0) ami06N w=(2u) l=180n as=1.2p ad=1.2p ps=5.2u pd=5.2u \
    m=(1)*(1)

// Spectre Source Statements
vdd (vdd! 0) vsource dc=1.2
gnd (gnd! 0) vsource dc=0


parameters vhi=1.2 tr=50p tf=50p
```

```
A (A 0) vsource type=pulse val0=0 val1=vhi rise=tr fall=tf delay=0 width=6n period=12n
B (B 0) vsource type=pulse val0=0 val1=vhi rise=tr fall=tf delay=3n width=3n period=6n
// Spectre Analyses and Output Options Statements
// Output Options
simOptions options
//+     reltol = 1.00000000E-03
//+     vabstol = 1.00000000E-06
//+     iabstol = 1.00000000E-12
//+     temp = 27
//+     save = allpub
//+     currents = selected
// Analyses
// dc1 dc oppoint=logfile homotopy=all
// tran1 tran stop=1 errpreset=moderate
tran1 tran start=0 stop=15n step=0.1n errpreset=moderate
// End of Netlist
```

Part D: Schematic NAND

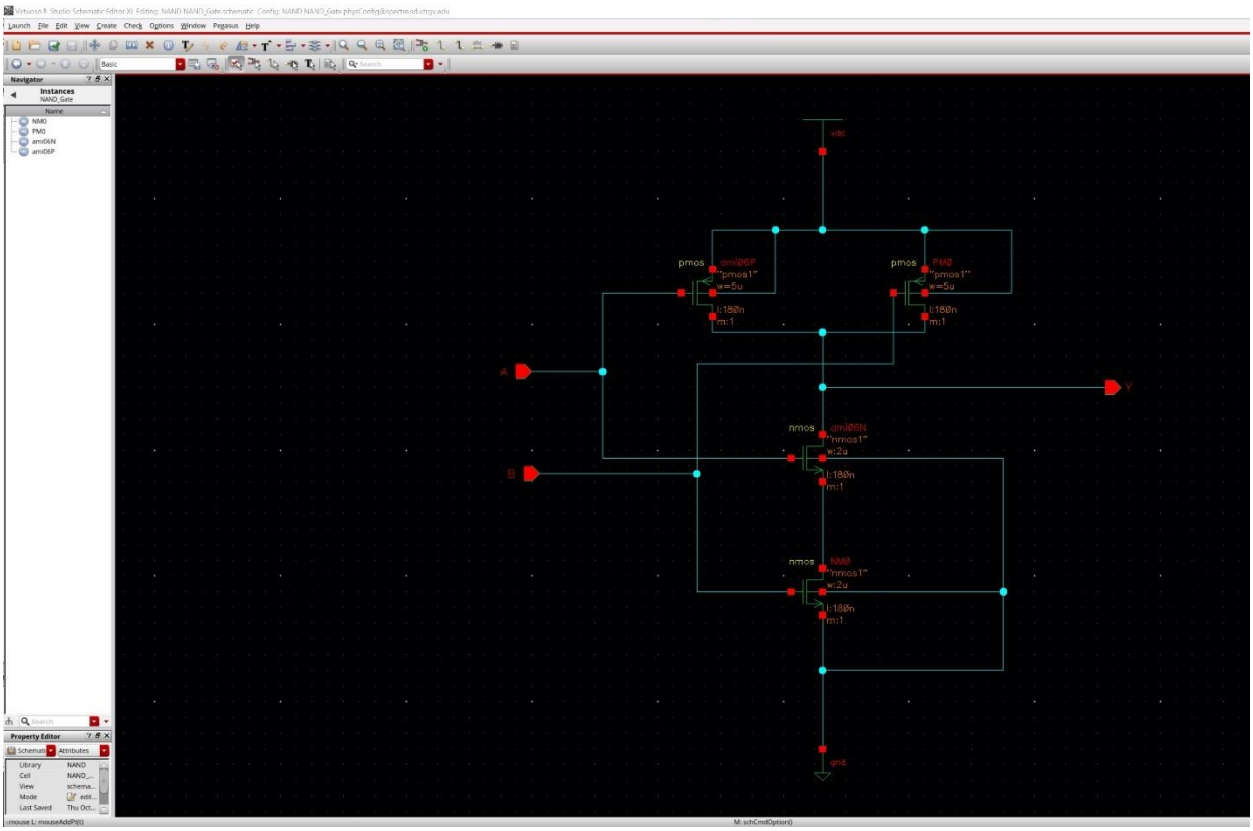

Fig.7: Schematic NAND

Part D: Symbol NAND

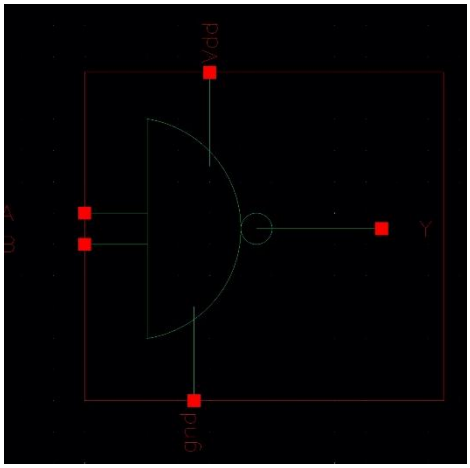

Fig.8: Symbol NAND

Part E: Layout XOR

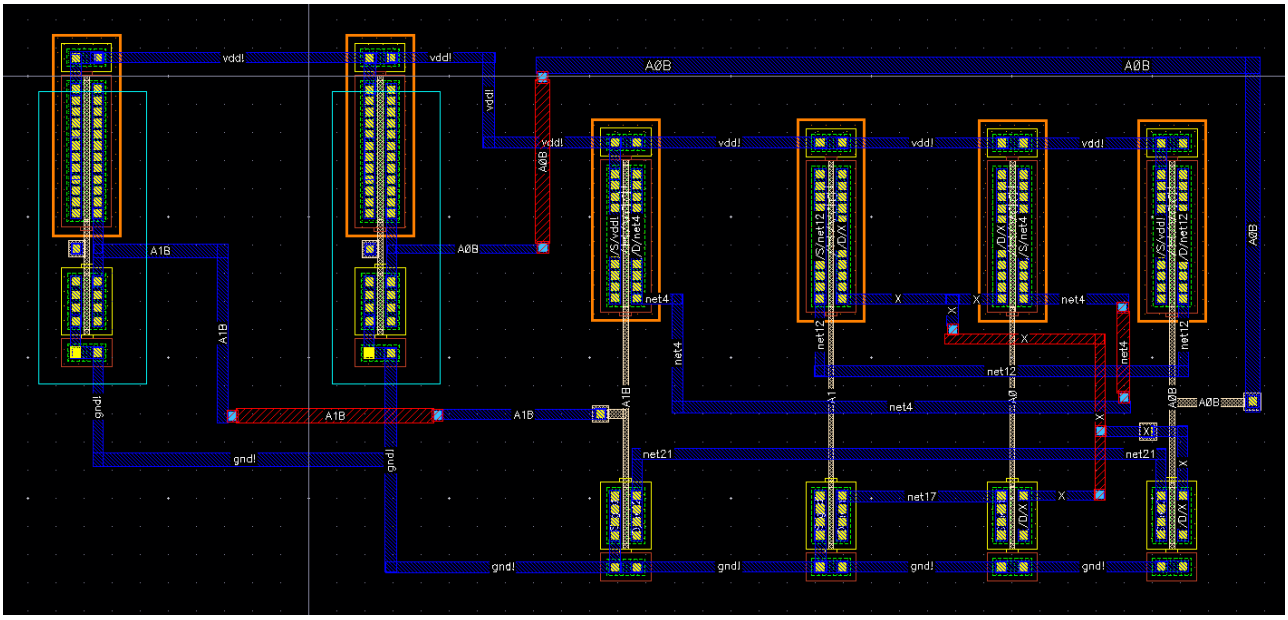

Fig.9: Layout XOR

Part E: Input-output waveforms (Truth table: 4 combinations) XOR

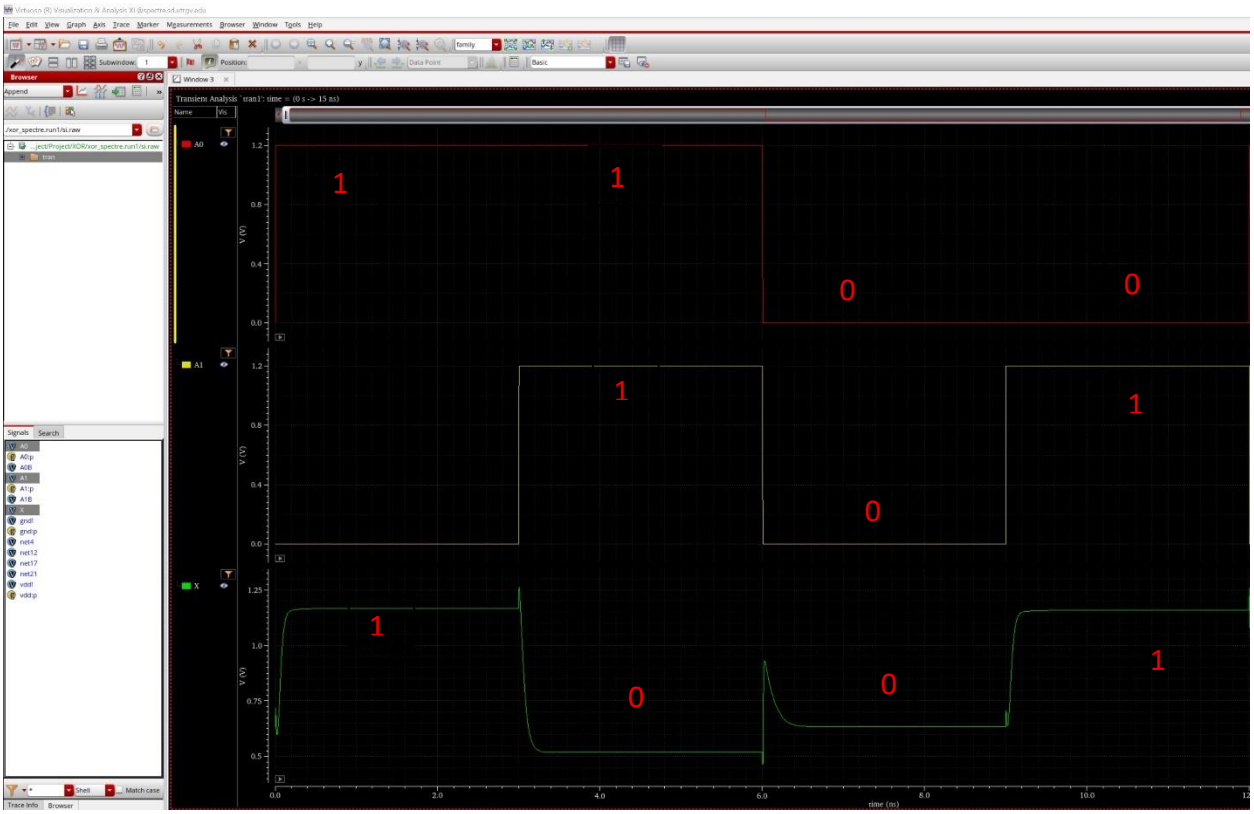

Fig.10: Input-output waveforms(XOR)

Part E: Si.inp files (spectre simulation) XOR

// Generated for: spectre

// Generated on: Oct 21 12:52:18 2025

// Design library name: XOR_Gate

// Design cell name: XOR_Gate

// Design view name: schematic

simulator lang=spectre

global 0 vdd!

include "/home/blx188/Spectre-Models/standalone/ami06N.m"

include "/home/blx188/Spectre-Models/standalone/ami06P.m"

```
// Library name: inverter_26
// Cell name: not_gate
// View name: schematic
subckt not_gate inv_in inv_out
    ami06P (inv_out inv_in vdd! vdd!) ami06P w=(5u) l=180n as=3p ad=3p \
        ps=11.2u pd=11.2u m=(1)*(1)
    ami06N (inv_out inv_in 0 0) ami06N w=(2u) l=180n as=1.2p ad=1.2p \
        ps=5.2u pd=5.2u m=(1)*(1)
ends not_gate
// End of subcircuit definition.

// Library name: XOR_Gate
// Cell name: XOR_Gate
// View name: schematic
P3 (X A1 net12 vdd!) ami06P w=(5u) l=180n as=3p ad=3p ps=11.2u pd=11.2u \
        m=(1)*(1)
P2 (net12 A0B vdd! vdd!) ami06P w=(5u) l=180n as=3p ad=3p ps=11.2u pd=11.2u \
        m=(1)*(1)
P0 (X A0 net4 vdd!) ami06P w=(5u) l=180n as=3p ad=3p ps=11.2u pd=11.2u \
        m=(1)*(1)
P1 (net4 A1B vdd! vdd!) ami06P w=(5u) l=180n as=3p ad=3p ps=11.2u pd=11.2u \
        m=(1)*(1)
N2 (net21 A1B 0 0) ami06N w=(2u) l=180n as=1.2p ad=1.2p ps=5.2u pd=5.2u \
        m=(1)*(1)
N1 (net17 A1 0 0) ami06N w=(2u) l=180n as=1.2p ad=1.2p ps=5.2u pd=5.2u \
        m=(1)*(1)
N4 (X A0B net21 0) ami06N w=(2u) l=180n as=1.2p ad=1.2p ps=5.2u pd=5.2u \
        m=(1)*(1)
```

```
N3 (X A0 net17 0) ami06N w=(2u) l=180n as=1.2p ad=1.2p ps=5.2u pd=5.2u \
      m=(1)*(1)
I0 (A1 A1B) not_gate
inverter (A0 A0B) not_gate

// Spectre Source Statements
vdd (vdd! 0) vsource dc=1.2
gnd (gnd! 0) vsource dc=0

parameters vhi=1.2 tr=5p tf=5p
// A goes low for 6 ns then high for 6 ns (period 12 ns)
A0 (A0 0) vsource type=pulse val0=0 val1=vhi rise=tr fall=tf delay=0 width=6n period=12n

// B toggles every 3 ns with period 6 ns, phased to start low then high
A1 (A1 0) vsource type=pulse val0=0 val1=vhi rise=tr fall=tf delay=3n width=3n period=6n
// Spectre Analyses and Output Options Statements
// Output Options
simOptions options
//+     reltol = 1.00000000E-03
//+     vabstol = 1.00000000E-06
//+     iabstol = 1.00000000E-12
//+     temp = 27
//+     save = allpub
//+     currents = selected
// Analyses
// dc1 dc oppoint=logfile homotopy=all
// tran1 tran stop=1 errpreset=moderate
tran1 tran start=0 stop=15n step=0.1n errpreset=moderat
// End of Netlist
```

Part E: Schematic XOR

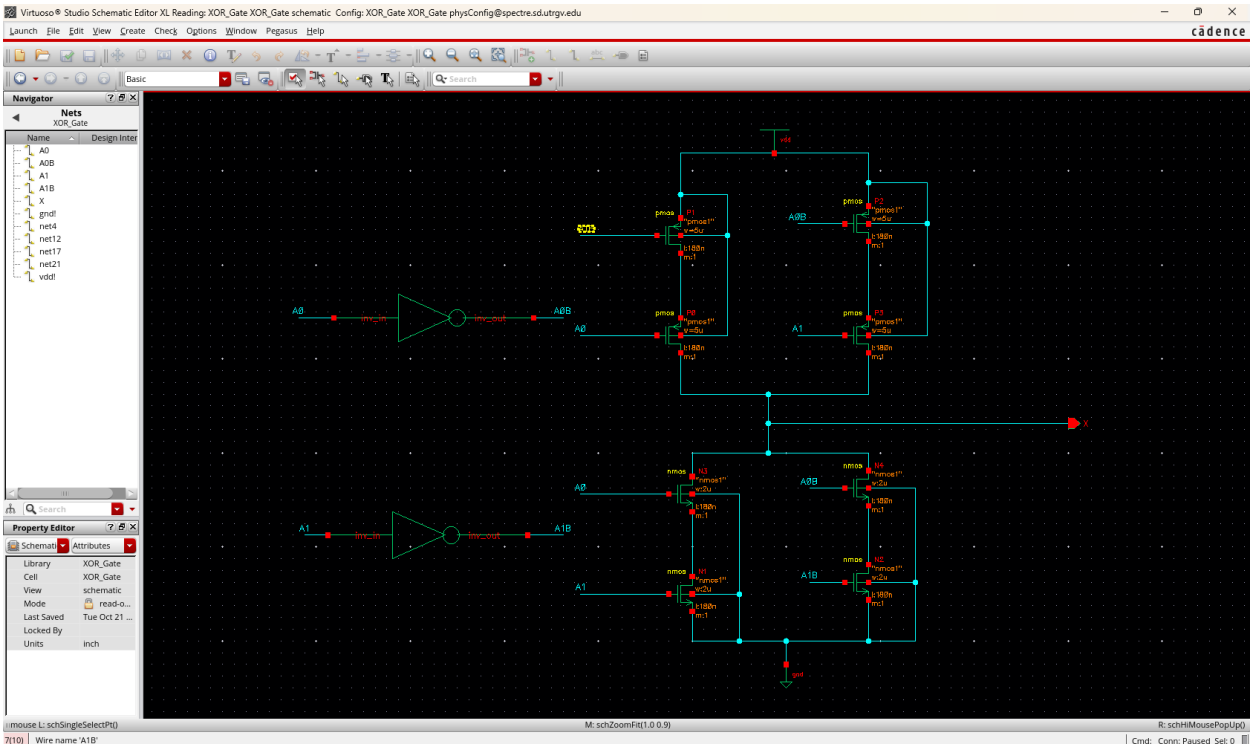

Fig.11: Circuit Schematic (XOR)

Part E: Symbol (XOR)

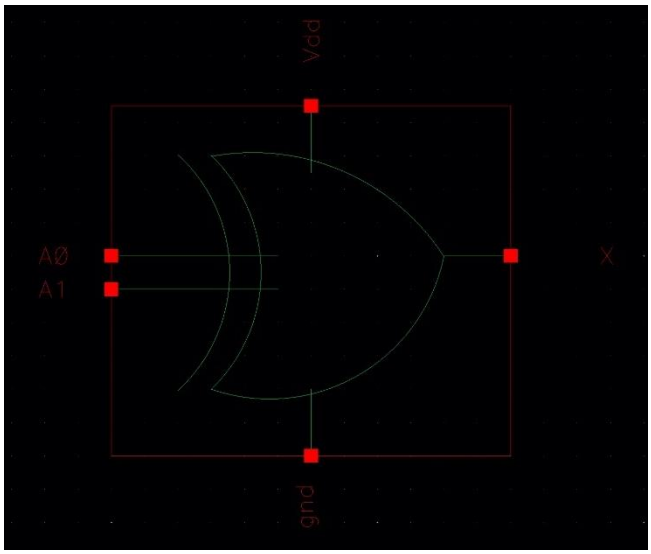

Fig.12: Symbol (XOR)

Part F: (100 words) Find a research paper (Conference papers or journal articles): Include Authors, Title, Publication year and name of the journal/conference

Topic: Roadmap for Semiconductor Industry & VLSI Trends

The paper "Semiconductor Industry: Present & Future" focuses on how the semiconductor industry is growing in the fields of AI, high-speed computing, neuromorphic computing, IoT, mobile devices, and automobiles. It illustrates the ongoing transaction from FinFET to nanosheet, optimization of power, area, and increasing the speed. As mobile, automotive, and sensor technologies advance towards greater efficiency and intelligence, advanced packaging, 3D stacking, and chip-to-chip interconnects make it possible for powerful HPC and AI systems. In the new area of VLSI, semiconductor size will be in the micro scale, will be faster, and will be more compact. In conclusion, semiconductors are about to enter a new "golden era," driving economic expansion and digital transformation as they approach a trillion-dollar global market by 2030.

Reference:

K. Zhang, "1.1 Semiconductor Industry: Present & Future," 2024 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 2024, pp. 10-15, doi: 10.1109/ISSCC49657.2024.10454358.

Appendix A: NOR GATE

1. Rise Time & Fall Time of NOR gate

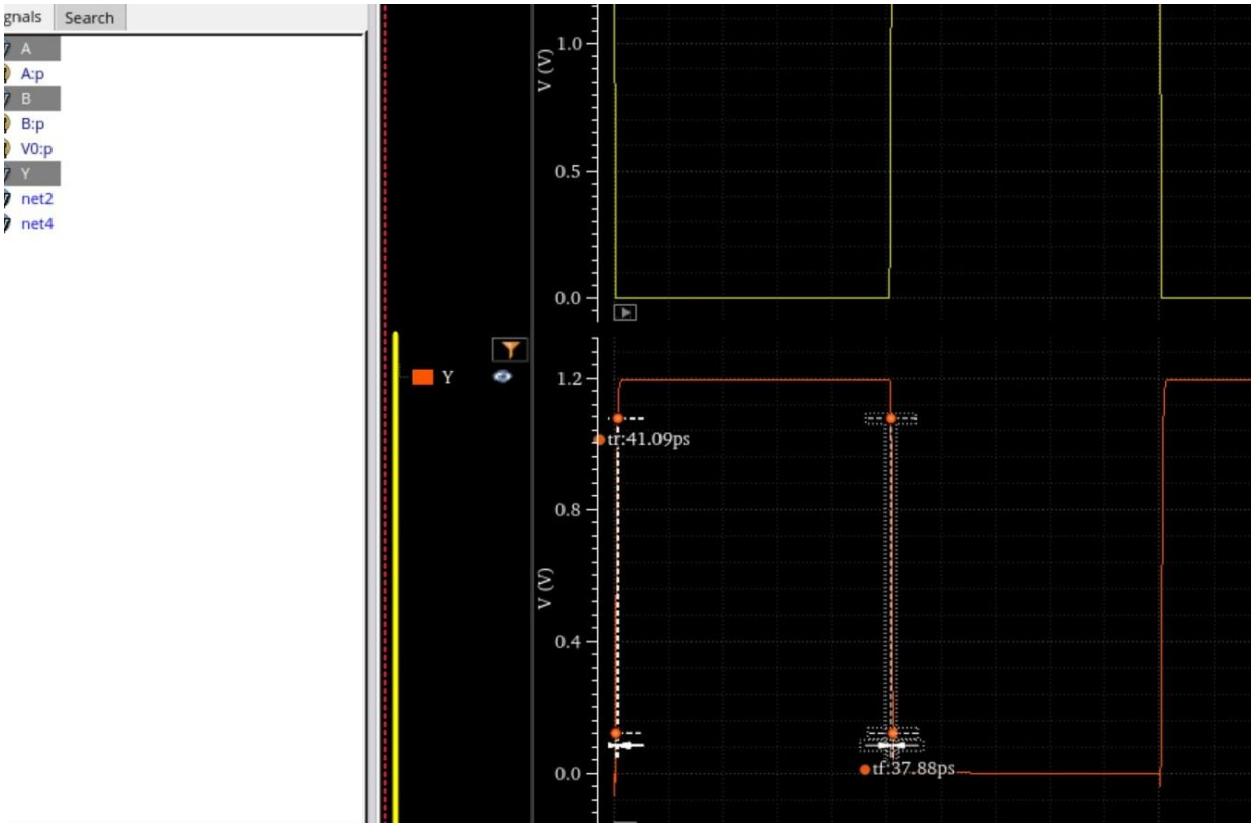

Fig.13: Rise time and Fall time (NOR)

2. Propagation Delay NOR Gate

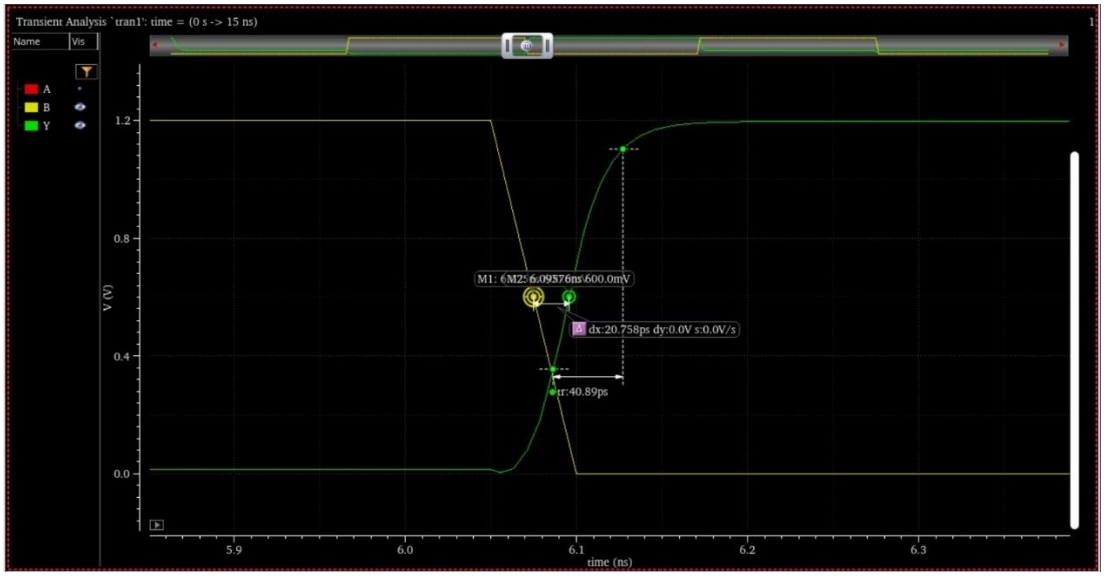

Fig.14: Propagation Delay (NOR)

3. Total Area of NOR Gate

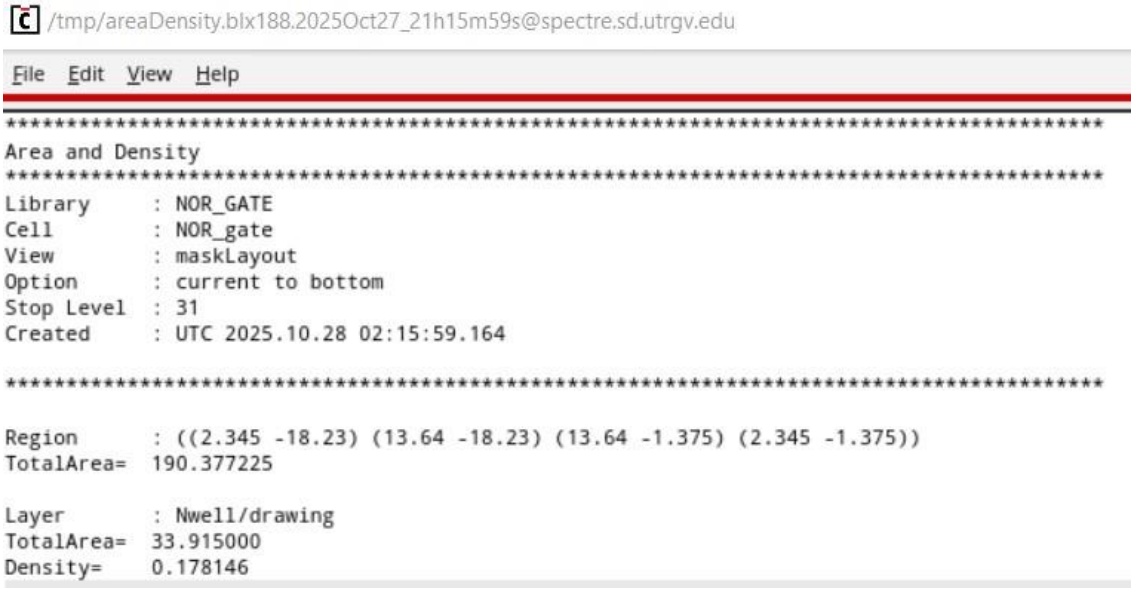

Fig.15: Area (NOR)

4. DRC Check of NOR Gate Layout

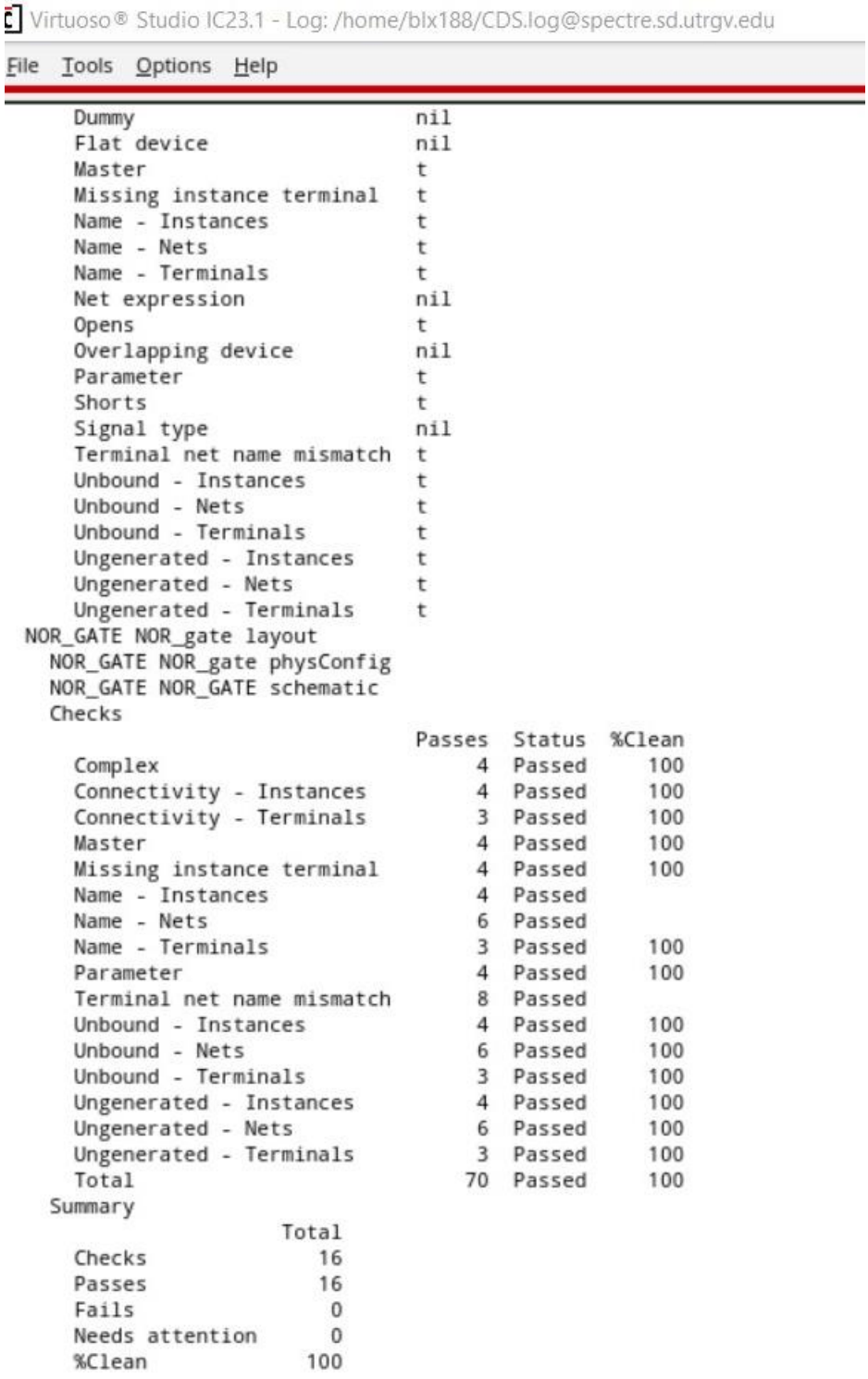

Fig.16: DRC Check of NOR Gate Layout

Appendix B: NAND GATE

1. Rise Time & Fall Time of the NAND gate

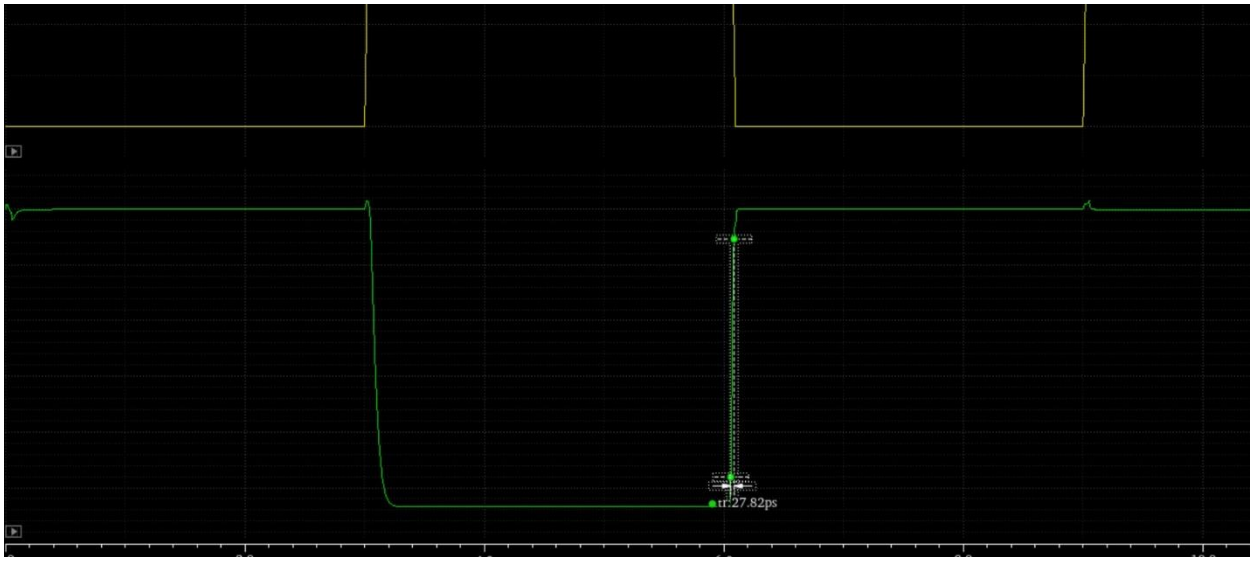

Fig.17: Rise Time

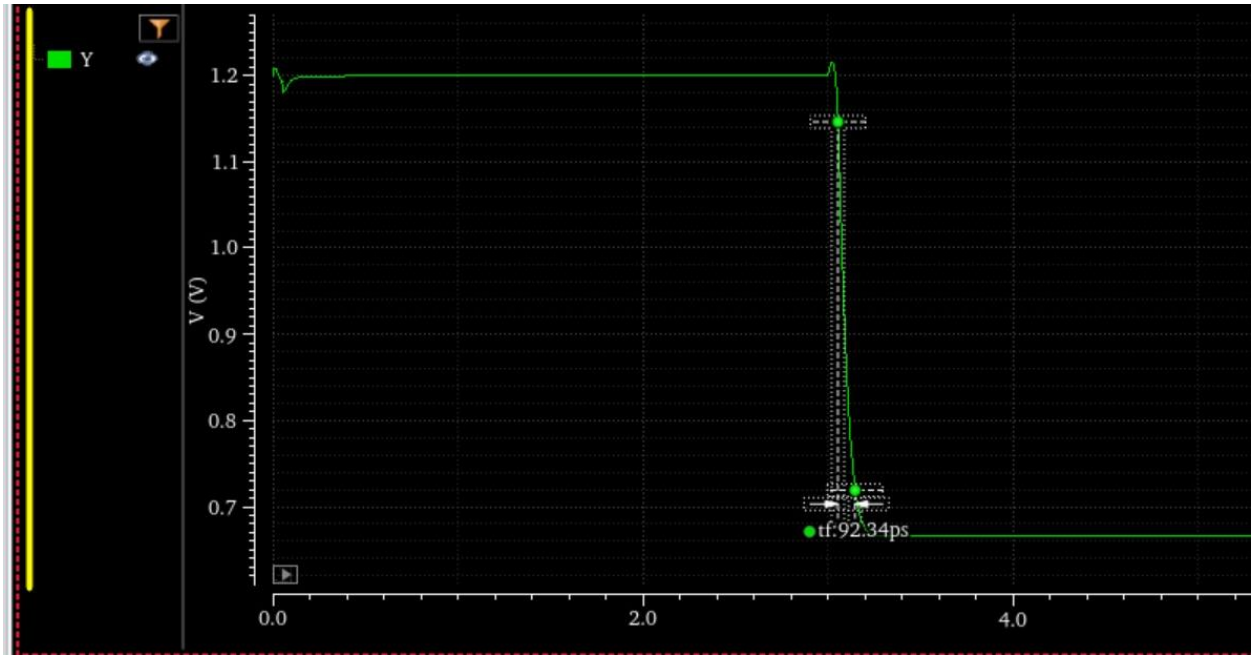

Fig.18: Fall Time

2. Propagation Delay NAND Gate

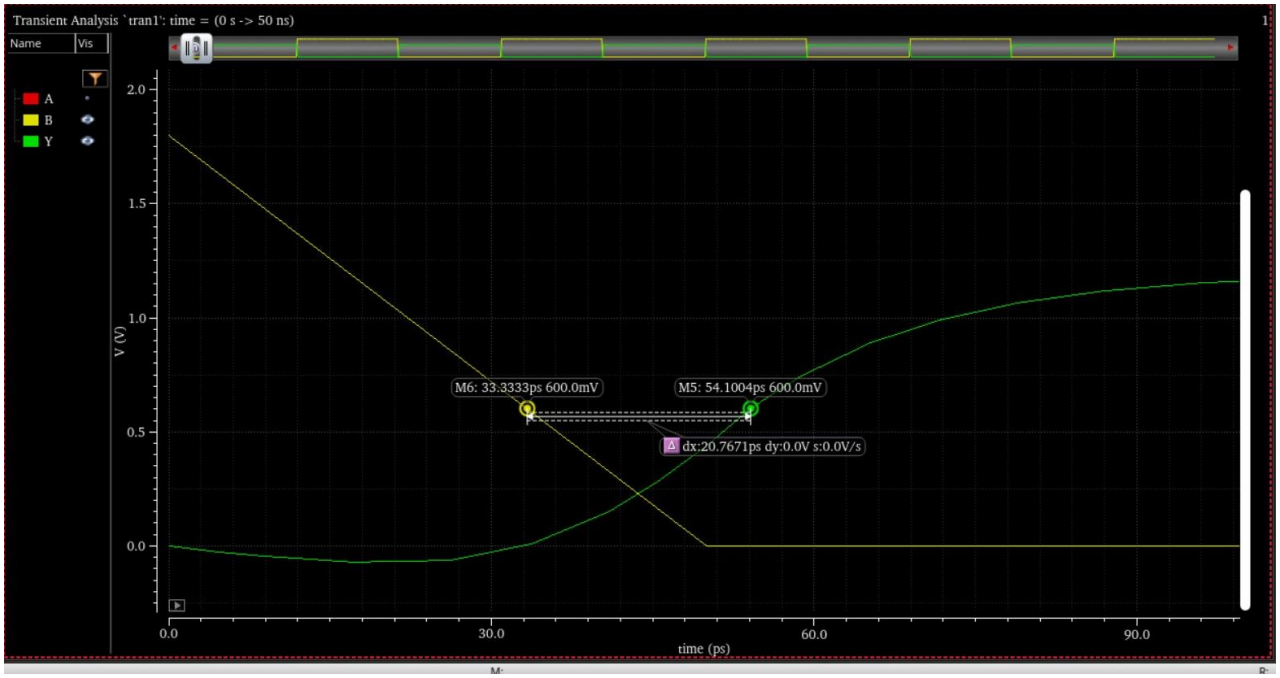

Fig.19: Propagation Delay NAND Gate

3. Total Area of NAND Gate

/tmp/areaDensity.blx188.2025Oct27_22h38m38s@spectre.sd.utrgv.edu

File Edit View Help

```
**********************************************************************************************
Area and Density
**********************************************************************************************
Library      : NAND
Cell         : NAND_Gate
View         : maskLayout
Option       : current to bottom
Stop Level   : 31
Created      : UTC 2025.10.28 03:38:38.984

**********************************************************************************************

Region       : ((-0.67 -18.35) (9.18 -18.35) (9.18 -1.475) (-0.67 -1.475))
TotalArea=   166.218750

Layer        : Nwell/drawing
TotalArea=   33.915000
Density=     0.204038
```

Fig.20: Area (NAND gate)

4. DRC of NAND Gate Layout

Virtuoso® Studio IC23.1 - Log: /home/blx188/CDS.log@spectre.sd.utrgv.edu

File Tools Options Help

```
    Dummy                        nil
    Flat device                  nil
    Master                       t
    Missing instance terminal    t
    Name - Instances             t
    Name - Nets                  t
    Name - Terminals             t
    Net expression               nil
    Opens                        t
    Overlapping device           nil
    Parameter                    t
    Shorts                       t
    Signal type                  nil
    Terminal net name mismatch   t
    Unbound - Instances          t
    Unbound - Nets               t
    Unbound - Terminals          t
    Ungenerated - Instances      t
    Ungenerated - Nets           t
    Ungenerated - Terminals      t
NAND NAND_Gate layout
  NAND NAND_Gate physConfig
  NAND NAND_Gate schematic
  Checks
                               Passes  Status  %Clean
    Complex                         4  Passed     100
    Connectivity - Instances        4  Passed     100
    Connectivity - Terminals        3  Passed     100
    Master                          4  Passed     100
    Missing instance terminal       4  Passed     100
    Name - Instances                4  Passed
    Name - Nets                     6  Passed
    Name - Terminals                3  Passed     100
    Parameter                       4  Passed     100
    Terminal net name mismatch      8  Passed
    Unbound - Instances             4  Passed     100
    Unbound - Nets                  6  Passed     100
    Unbound - Terminals             3  Passed     100
    Ungenerated - Instances         4  Passed     100
    Ungenerated - Nets              6  Passed     100
    Ungenerated - Terminals         3  Passed     100
    Total                          70  Passed     100
  Summary
                    Total
    Checks             16
    Passes             16
    Fails               0
    Needs attention     0
    %Clean            100
```

Fig.21: DRC Check of NAND Gate Layout

Appendix C: XOR GATE

1. Rise Time & Fall Time of the XOR gate

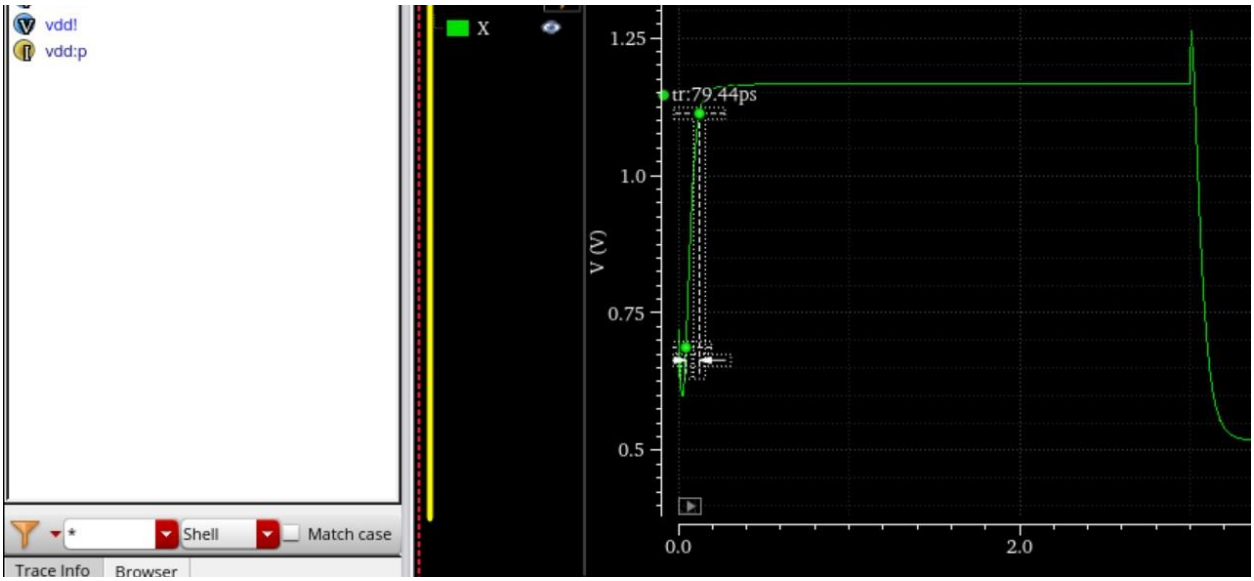

Fig.22: Rise Time

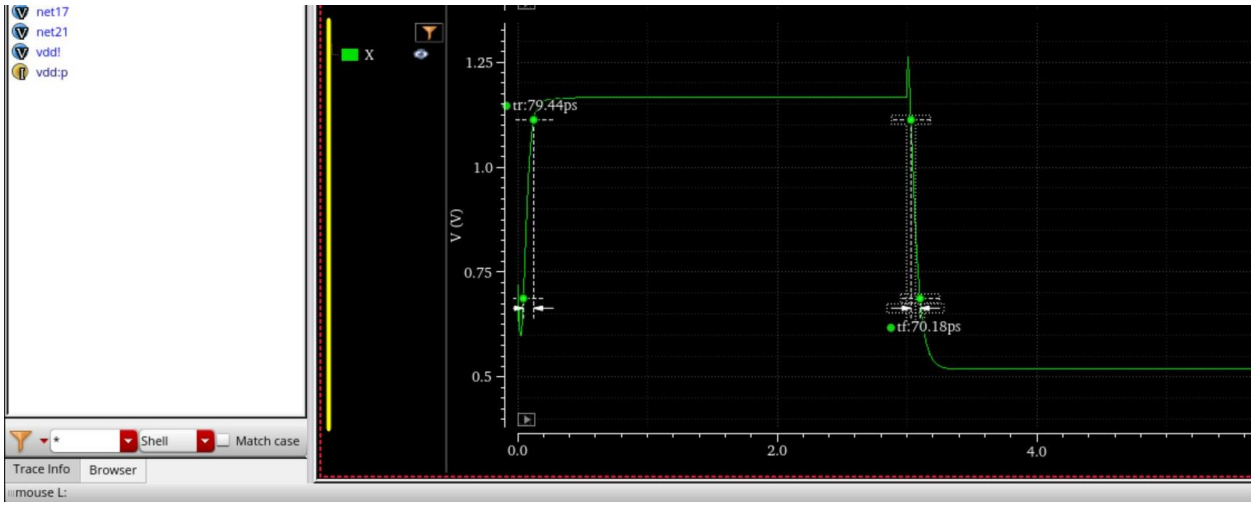

Fig.23: Fall Time

2. Propagation Delay NAND Gate

Fig.24: Propagation Delay

3. Area of XOR gate

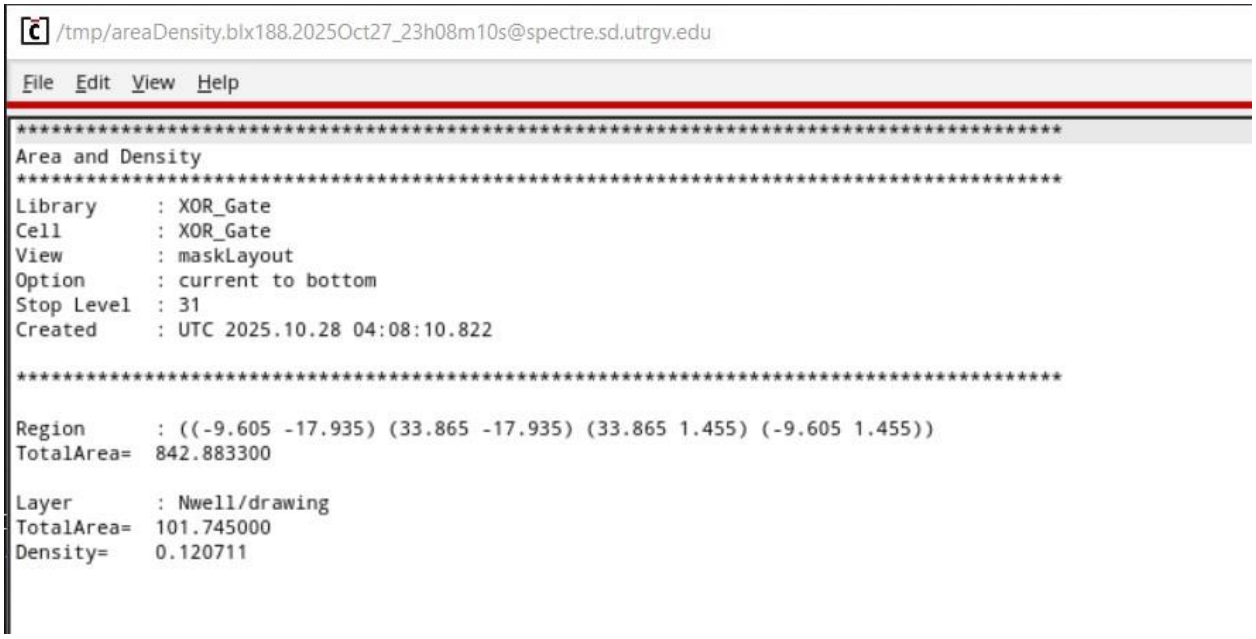

Fig.25: Area of XOR gate

4. DRC of XOR Gate Layout

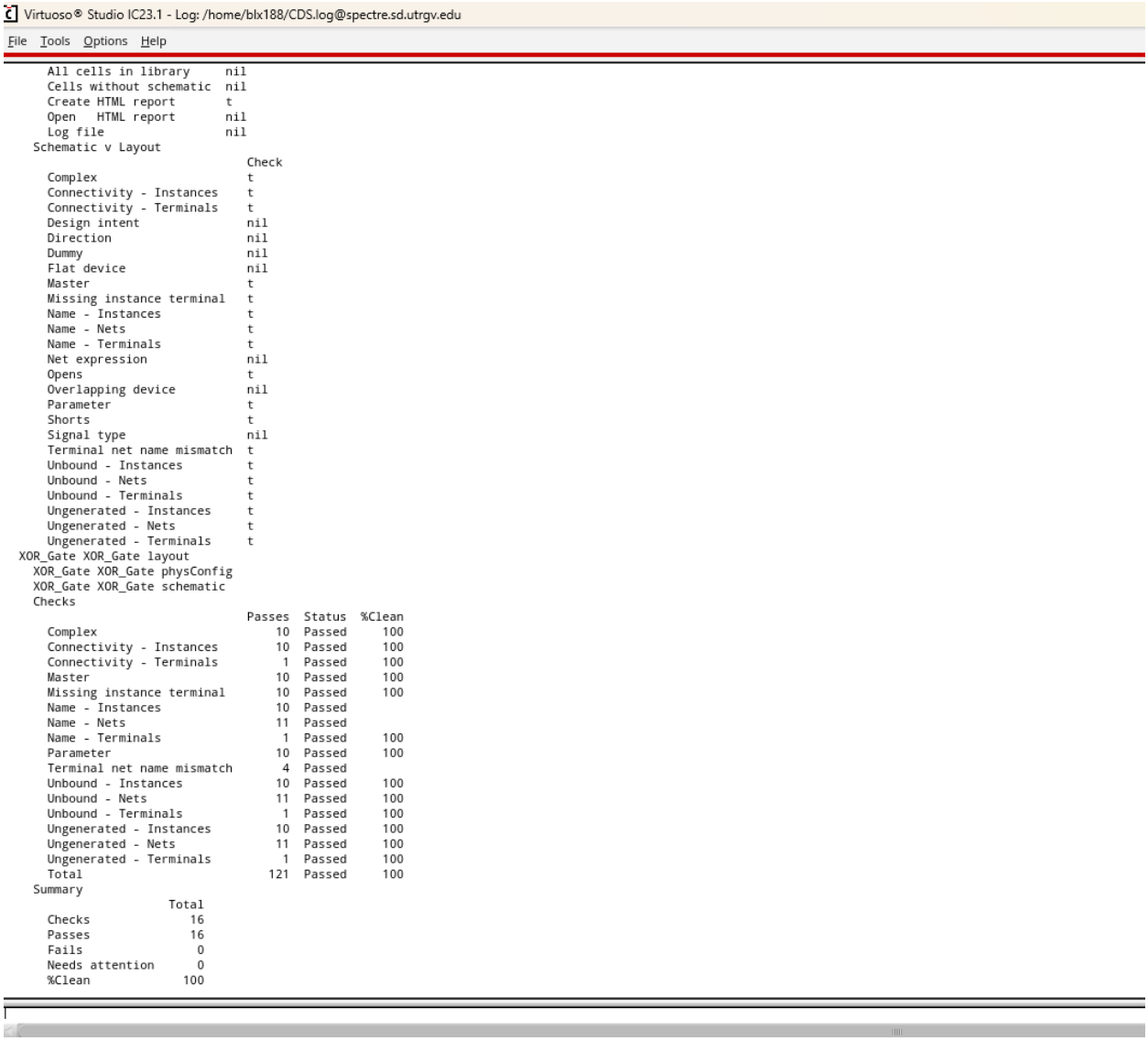

Fig.26: DRC of XOR Gate Layout