Convolutional Encoder/Viterbi Decoder

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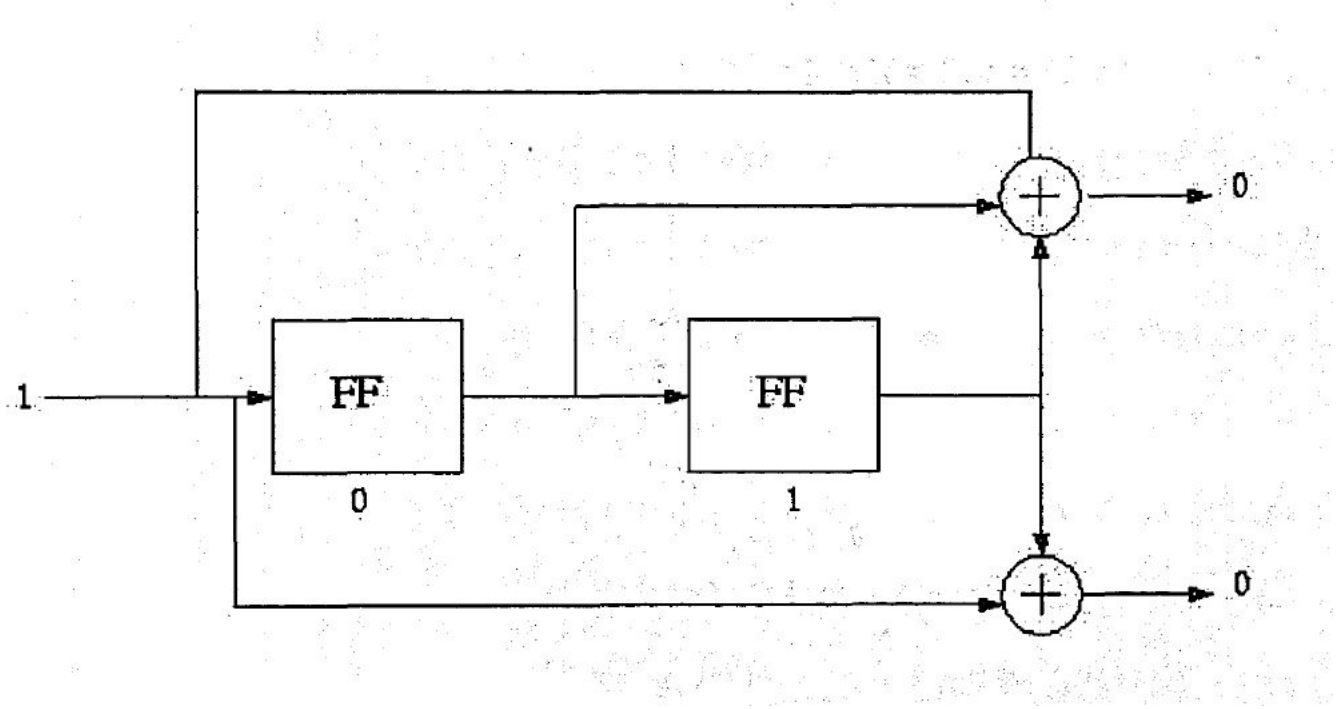
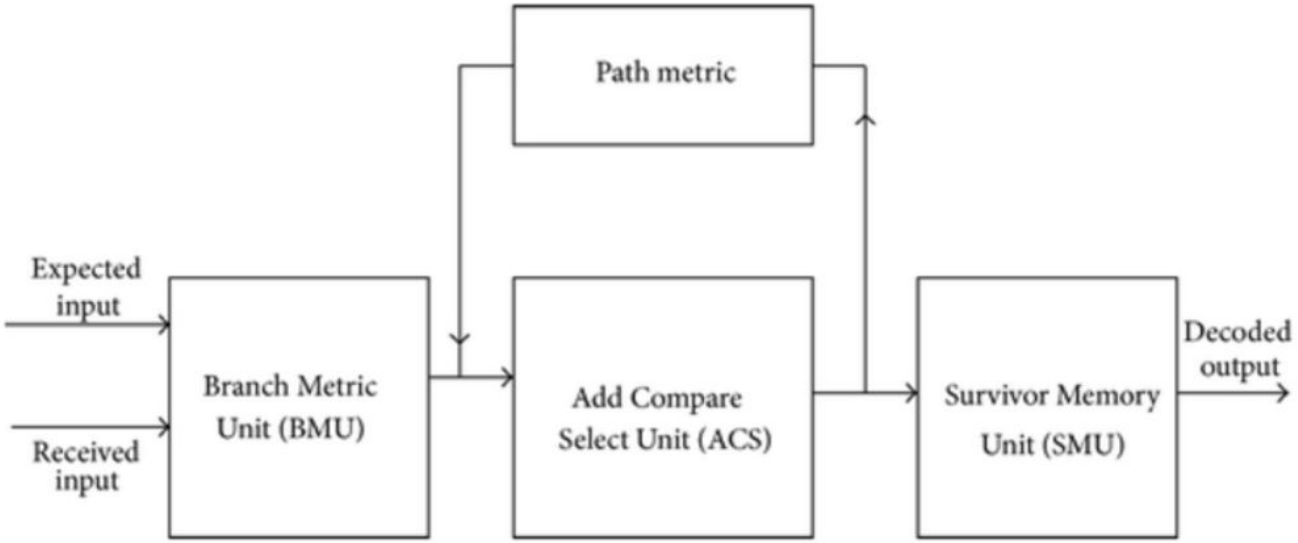
Introduction

- **Background:**
- Convolutional code error-correcting code used to overcome data corruption in digital communication channels.
- Viterbi Algorithm there are only a finite number of possible states of the encoder, and that given two consecutive states we can predict the input bit(s) that would have caused that state transition.
- **Problem Statement:** Design and implement Convolutional Encoder/Veterbi Decoder .

Convolutional Encoder:



Viterbi Decoder:



- **Branch Metric Unit (BMU):** Calculates the branch metrics for every stage.
- **Add Compare Select (ACS):** Calculates the path metrics of all the states in a stage. The number of ACS units depends on the constraint length
- **Survivor Memory Unit (SMU):** used to store the path history of all the surviving paths and is finally used to retrieve the original input sequence.

Approach to solution

- **Implementation of convolutional encoder/viterbi decoder as HW/SW co-design**

- HW/SW division
- HW/SW parallel synthesis
- HW/SW parallel simulation

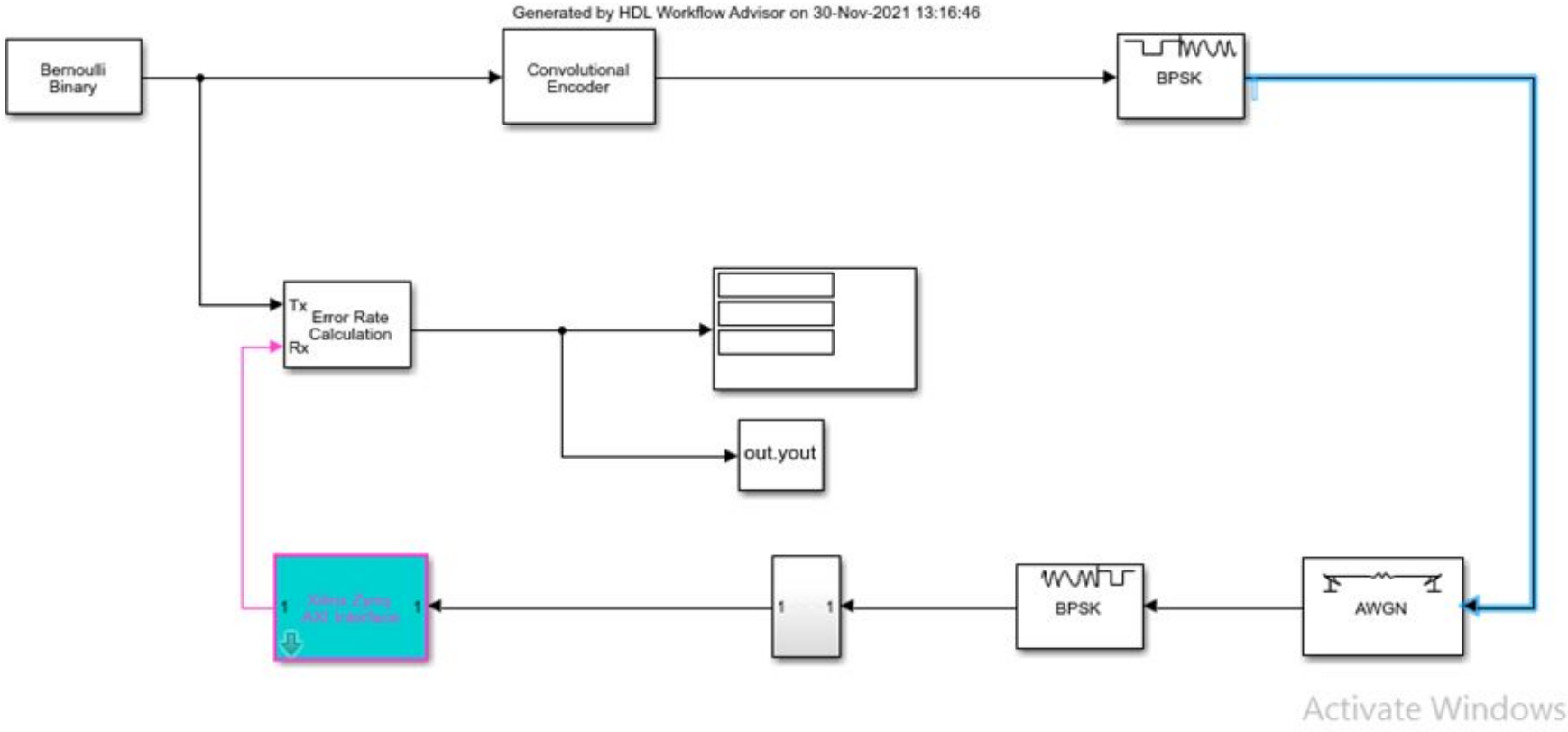
- **Tools used:** MATLAB simulink and vivado

HW/SW Partitioning

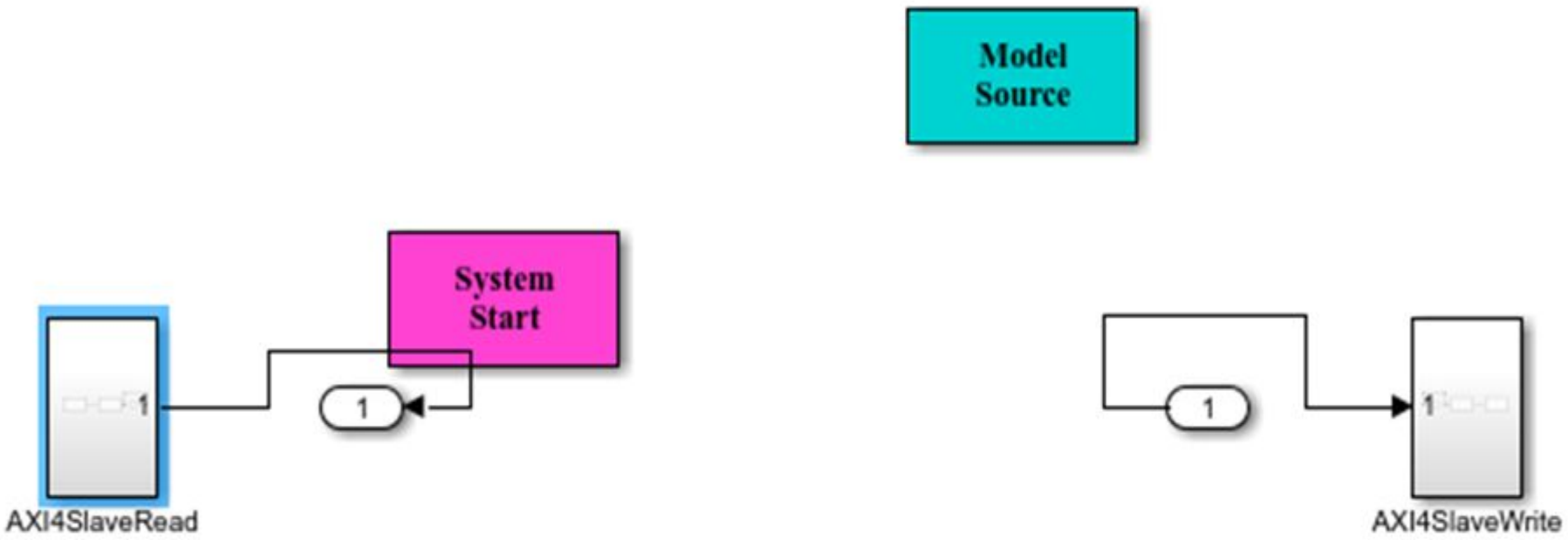
- **Hardware**: tasks with low complexity and high speed.
- **Software**: tasks with high complexity and low speed.

- **Viterbi decoder**:
- **Hardware blocks**: BMU, SMU and PMU
- **Software blocks**: Add-compare-select unit

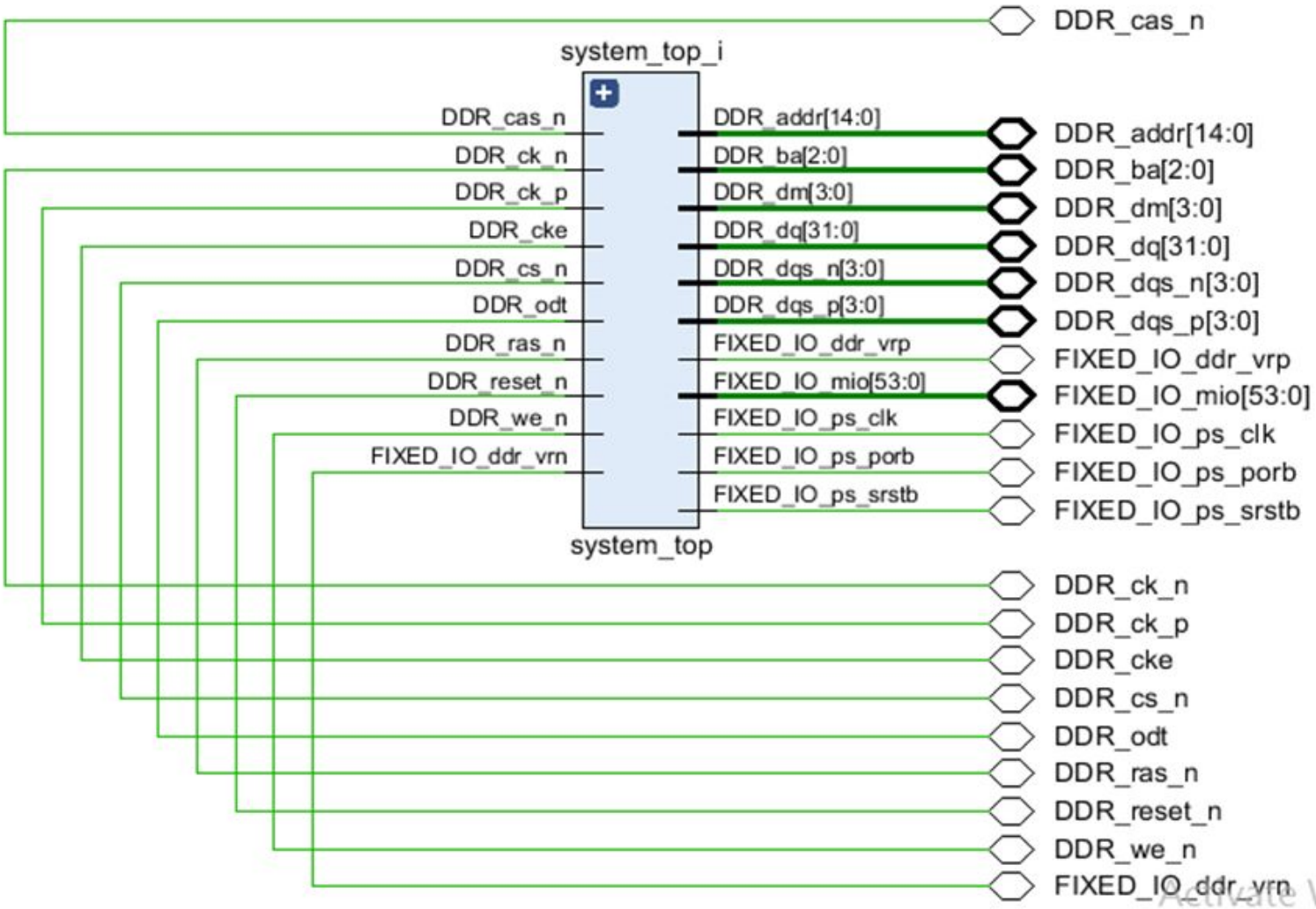
HDL Generated Model



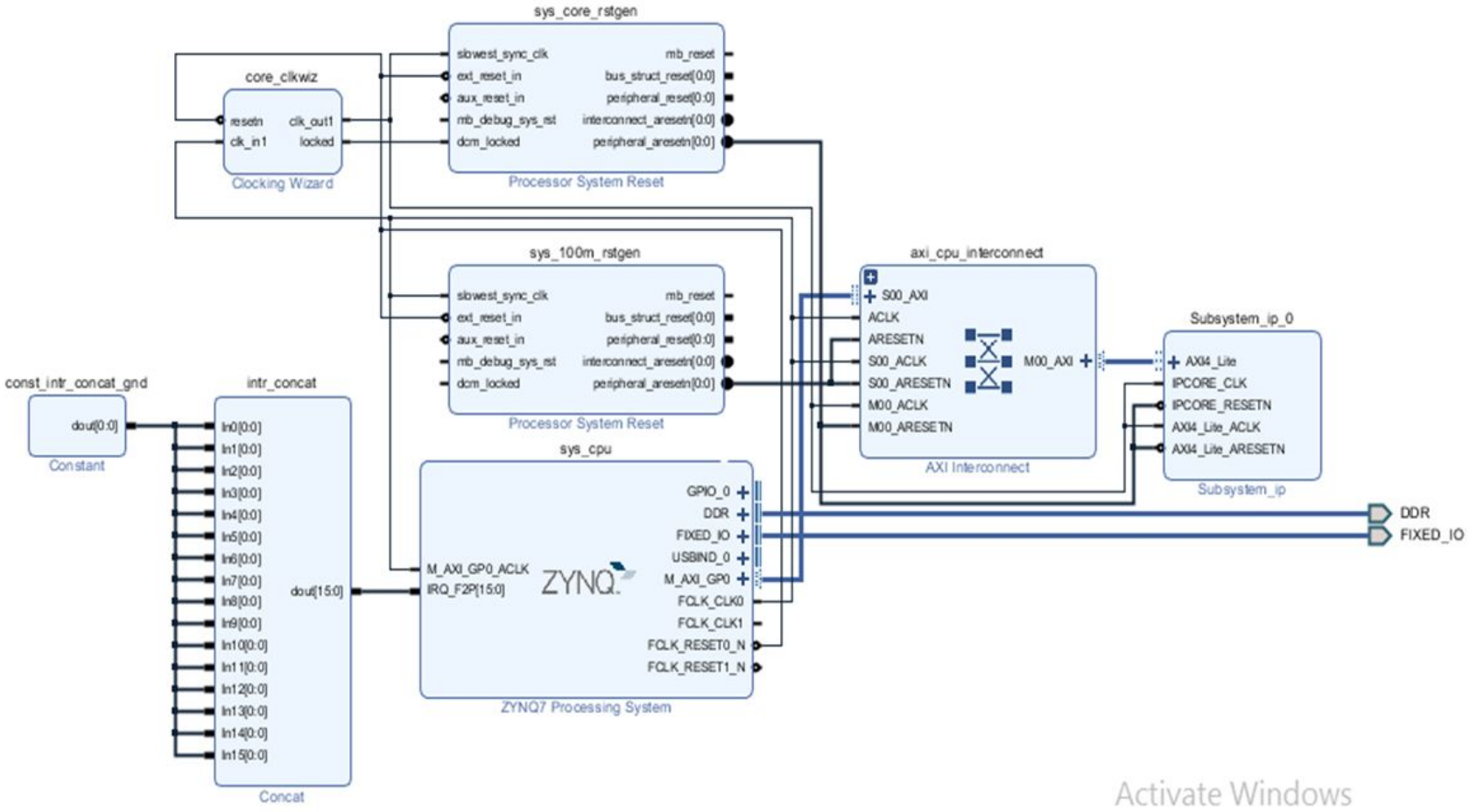
Elaboration of Subsystem



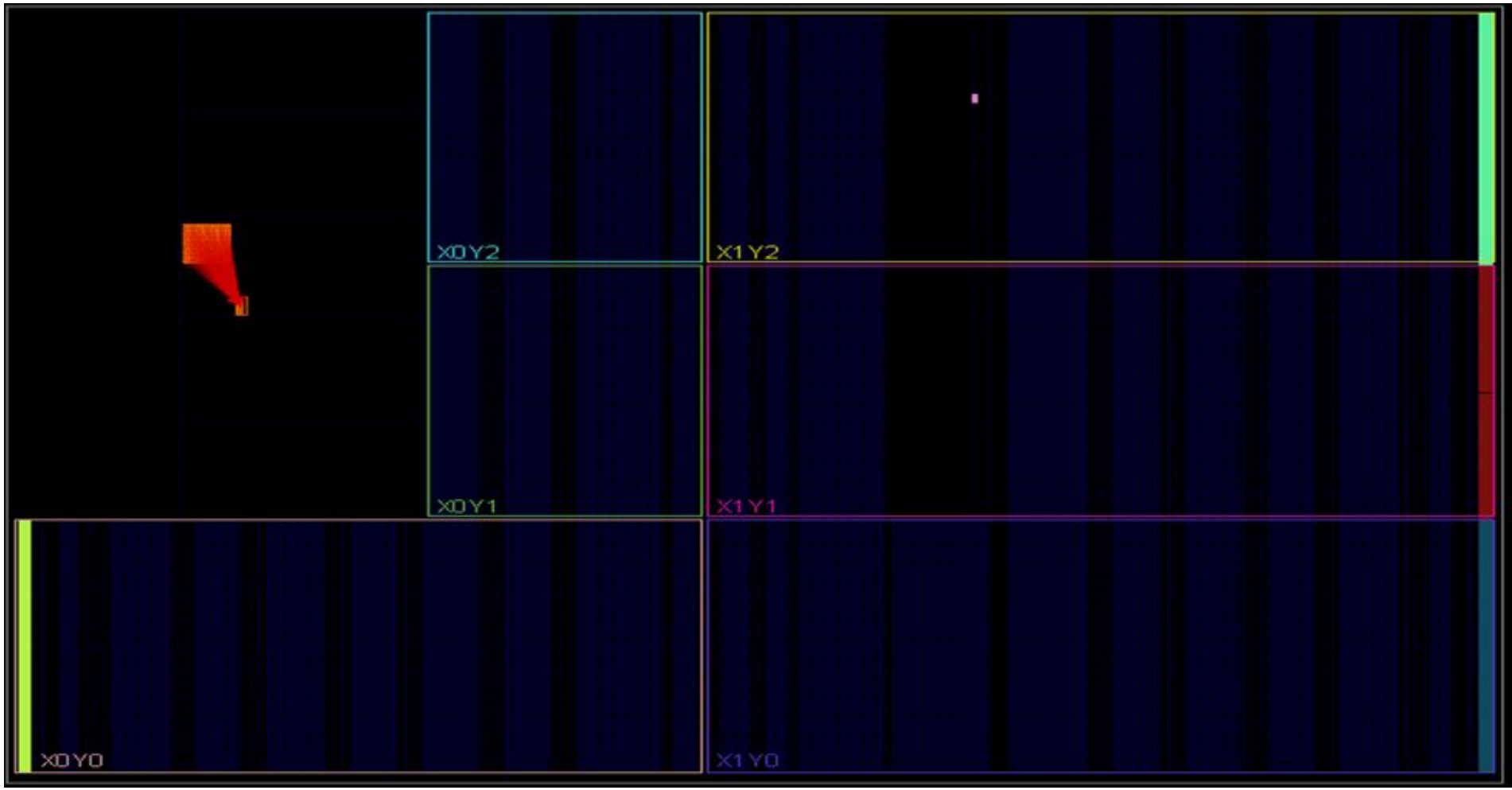
RTL of Viterbi Decoder



Synthesized Model



Mapping on FPGA



Utilization Report

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1. Slice Logic

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	3743	0	53200	7.04
LUT as Logic	3436	0	53200	6.46
LUT as Memory	307	0	17400	1.76
LUT as Distributed RAM	176	0		
LUT as Shift Register	131	0		
Slice Registers	6492	0	106400	6.10
Register as Flip Flop	6492	0	106400	6.10
Register as Latch	0	0	106400	0.00
F7 Muxes	209	0	26600	0.79
F8 Muxes	104	0	13300	0.78

Conclusion

- Viterbi Decoder plays a significant role in Communication Systems.
- HDL of Viterbi Decoder has been implemented as a IP core and integrated in Simulink Model.
- Hardware Software Codesign speed up the design process and reduce error in design.
- Fabrication rate increases.

Thank You