# Convolutional Encoder/Viterbi Decoder

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# Hardware Software Co-Dsn (EEE G626)


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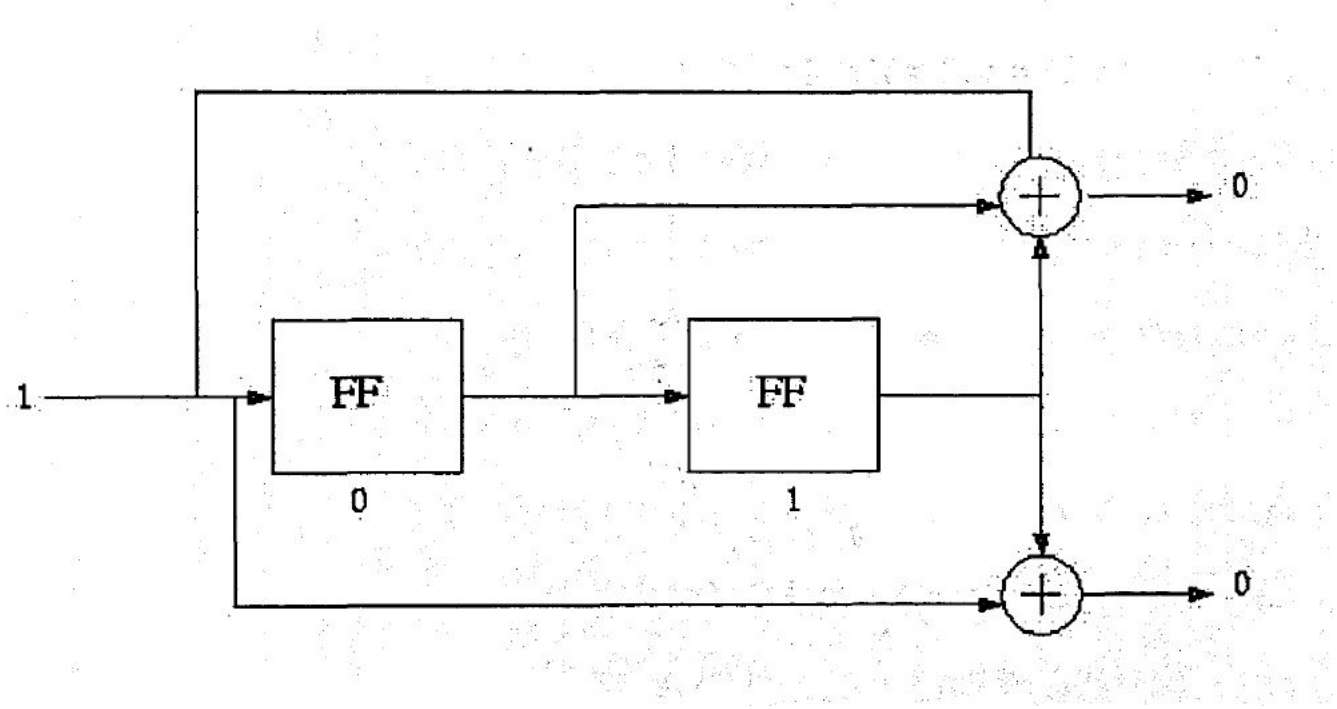
# Introduction



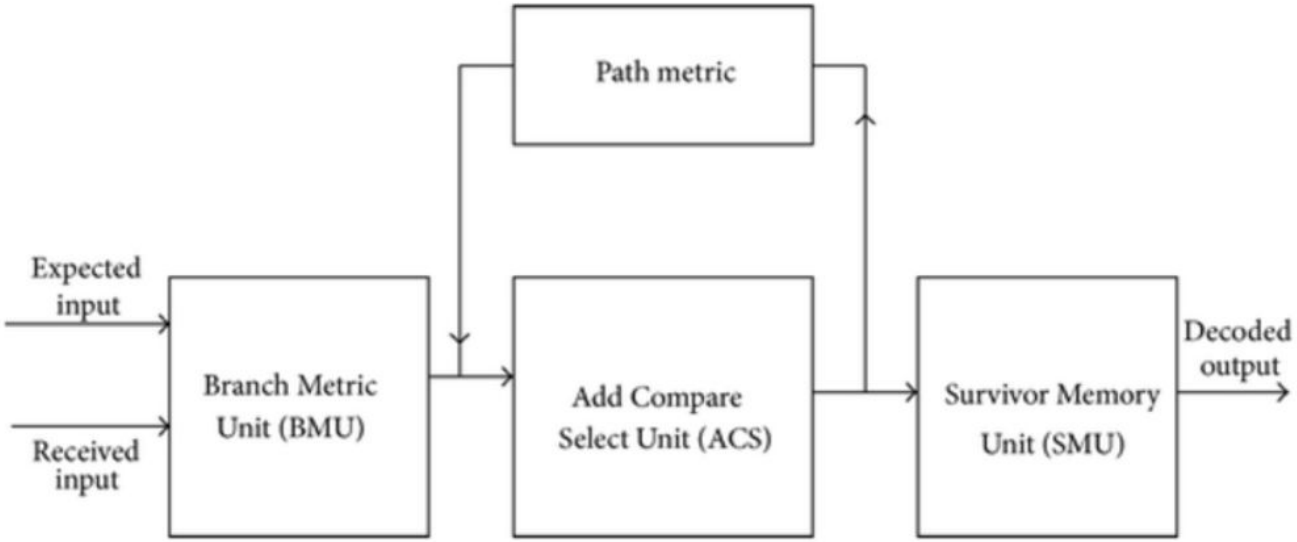
- **Background:**
- Convolutional code  error-correcting code used to overcome data corruption in digital communication channels.
- Viterbi Algorithm  there are only a finite number of possible states of the encoder, and that given two consecutive states we can predict the input bit(s) that would have caused that state transition.
- **Problem Statement:** Design and implement Convolutional Encoder/Veterbi Decoder .

# Convolutional Encoder:



# Viterbi Decoder:






- **Branch Metric Unit (BMU):** Calculates the branch metrics for every stage.
- **Add Compare Select (ACS):** Calculates the path metrics of all the states in a stage. The number of ACS units depends on the constraint length
- **Survivor Memory Unit (SMU):** used to store the path history of all the surviving paths and is finally used to retrieve the original input sequence.

encoder/viterbi decoder as

## Approach to solution

HW/SW co-design

HW/SW division

HW/SW parallel synthesis

HW/SW parallel simulation

Tools used: MATLAB simulink and vivado

## HW/SW Partitioning

Hardware: tasks with low complexity and high speed

Software: tasks with high complexity and low speed.

Viterbi decoder:

Hardware blocks: BMU, SMU and PMU

Software blocks:

Add-compare-select unit

# HW/SW Co Verification



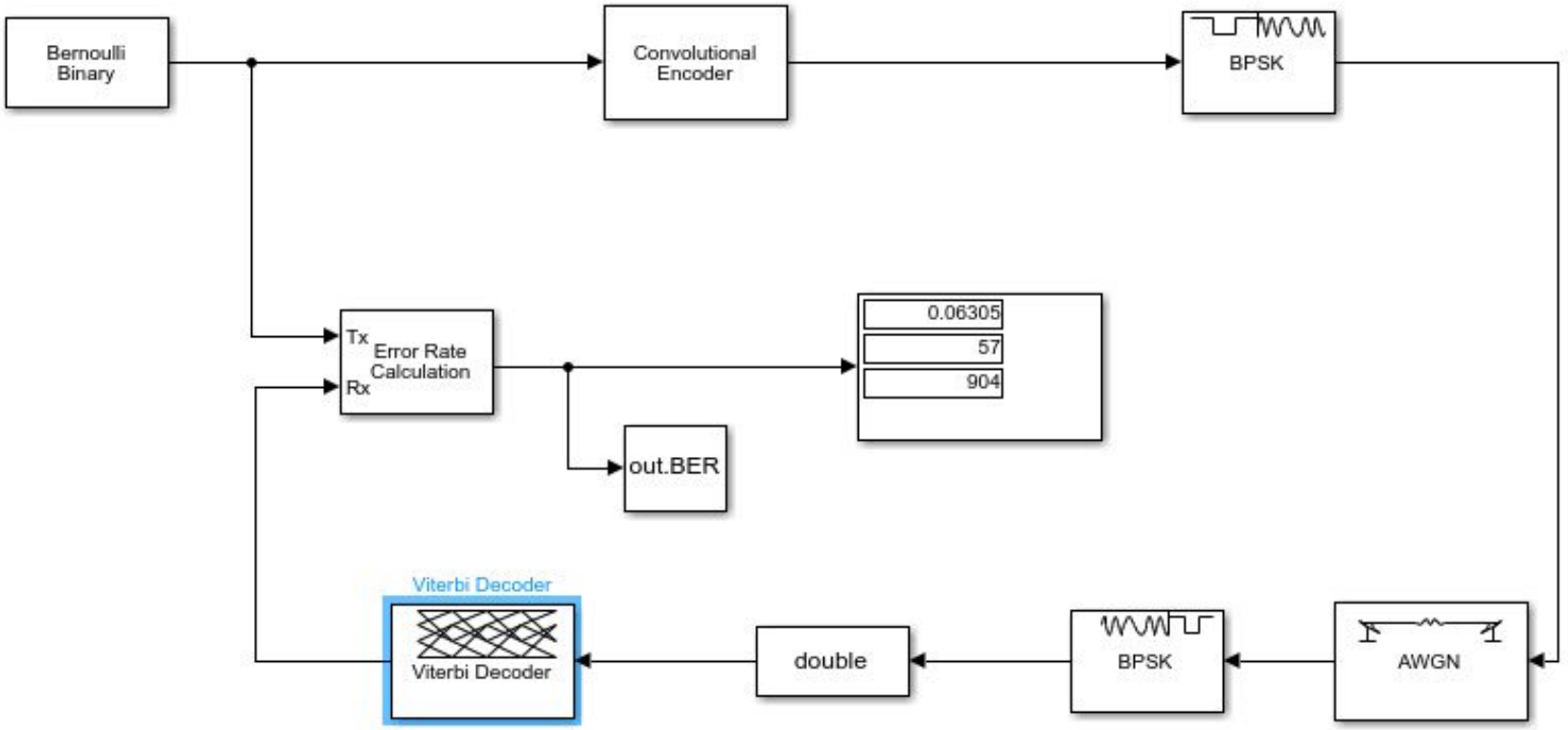
## System platform

Hardware: FPGA  accelerator

Software: Embed OS – ARM

Interfacing component: AMBA

# Software Testing



# Near Future work



Encode Viterbi decoder into HDL model

Integrating HDL and Embedded system and compare results with software tested error rate

# Thank You