Multi-rate DAG Scheduling Considering Communication Contention for NoC-based Embedded Many-core Processor

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Problem statement

Problem definition:

To identify a specific multi-rate DAG scheduling algorithm and implement the same in Multi Processor environment for Autonomous Cars

Assumptions:

Task Sets

Tools used:

Cheddar Simulator

MCRTSim

RTSim

SimSo

Description

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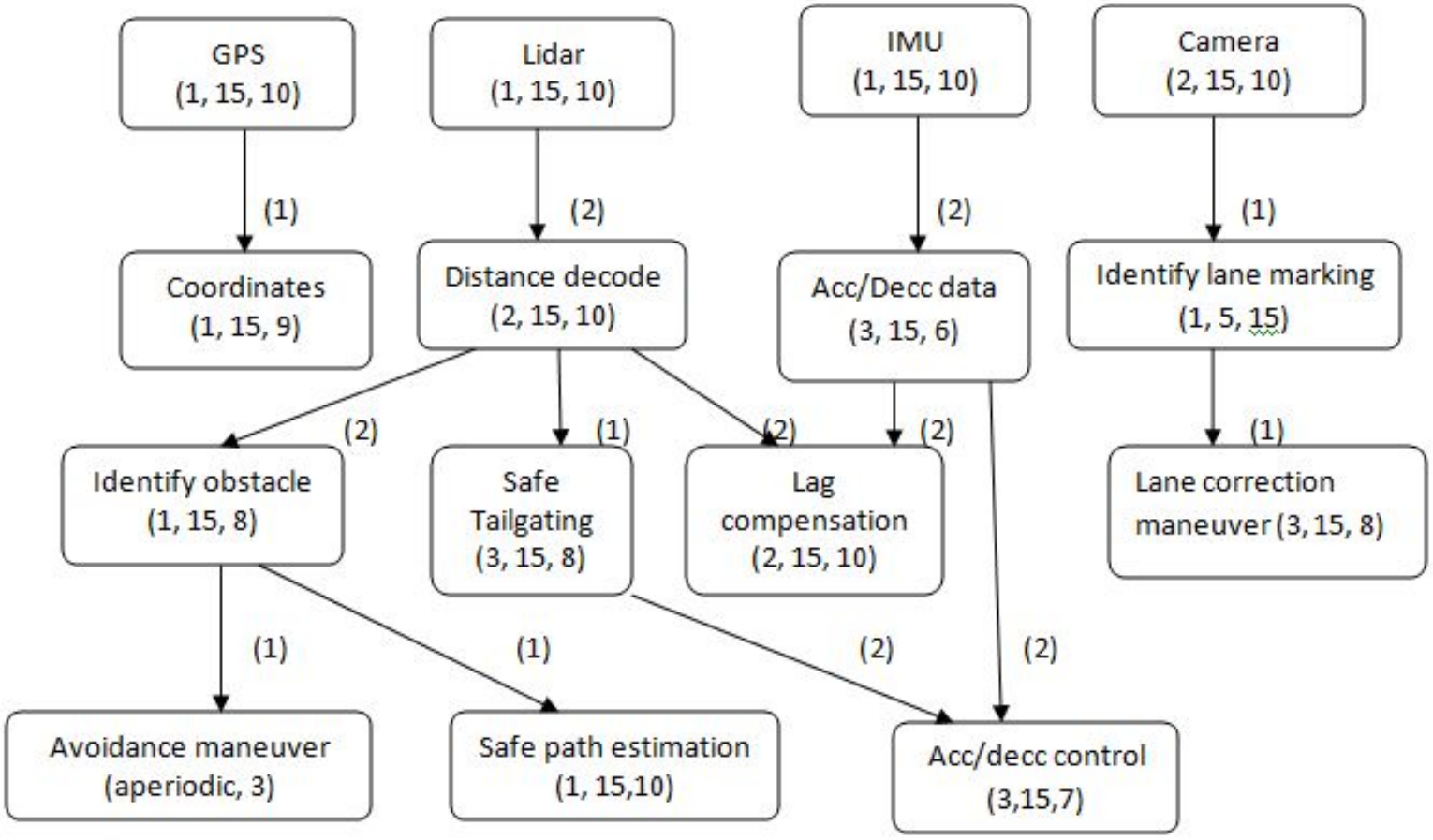
Directed Acyclic Graph for the tasks

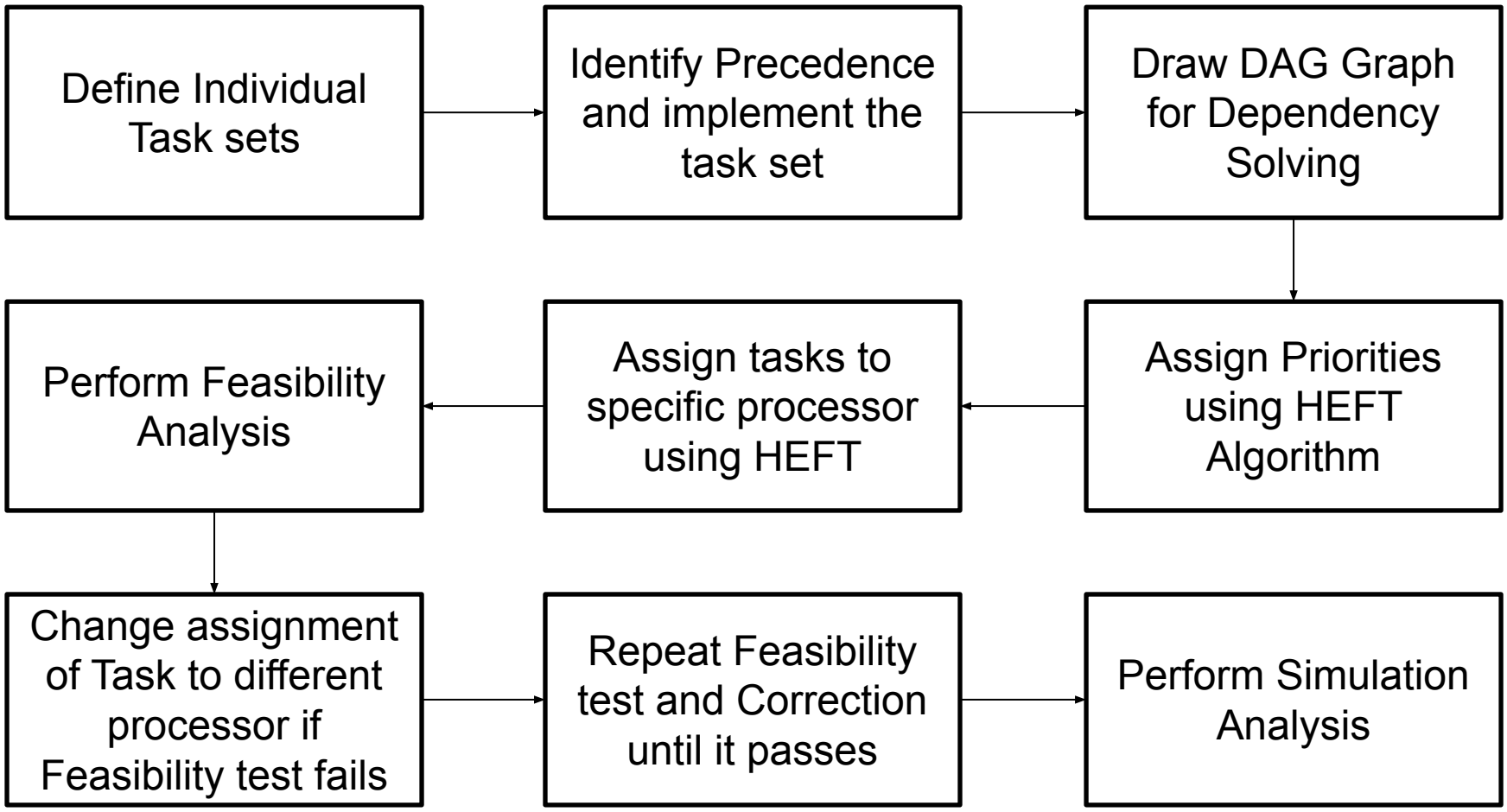


Description

- **Algorithm proposed:**
  - Dependency Graph using DAG
  - HEFT Scheduling for Multi Processor System
  - DMA Scheduling for Independent Processors

- **Expected Outcome**
  - Makespan reduced without deadline missing
  - Communication Contention free scheduling

Methodology



Methodology:

- **Novelty**
- HEFT algorithm has been used for task allocation
- Loading imbalance problem is met by incorporating utilisation balancing algorithm without violating the rules of heuristic HEFT.
- Three different architectures has been used to compare the results.

Implementation

- Three different pathways
  - 16x16 MPPA Implementation
  - 2x2 Implementation
  - 3x3 Implementation
  - 4x4 Implementation

Experimental Results

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Processor	Tasks assigned		Utilisation factor (ei/di)	Deadline missed if any	
	Tasks	Messages			
P1	Acc/dcc data, IMU	Acc/dcc data	0.85	none	Makespan = 480ms
P2	Lag compensation	Distance decode data	0.45	none	
P3	Lidar, Distance decode	-	0.3	none	
P4	Safe tailgating	Distance decode data	0.54	none	
P5	Acc/dcc control	Safe tailgate data	0.678	none	
P6	Identify Obstacle	Distance decode data	0.52	none	
P7	Safe path estimation	Identify obstacle	0.24	none	
P8	GPS, GPS coordinates	-	0.21	none	
P9	Camera, Lane marking, Lane correction	-	0.775	none	

Experimental Results

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Processor	Tasks assigned		Utilisation factor (ei/di)	Deadline missed if any	
	Tasks	Messages			
P1	Lidar, Lag compensation	Distance decode	0.55	none	**Makespan = 720ms**
P2	Distance decode, safe path estimation	Identify obstacle	0.84	none	
P3	IMU, Lane correction	-	0.475	none	
P4	-	Acc/dcc control, safe tailgating	1.25	none	
P5	Acc/dcc data, GPS coordinates	GPS coordinates	1.5	none	
P6	Identify Obstacle	Distance decode data	0.52	none	
P7	Safe tailgating	Distance decode	0.54	none	
P8	Acc/dcc control, Camera, GPS	-	0.72	none	
P9	Identify Lane marking,	Camera, Lane marking data	0.65	none	

Experimental Results

Type	2x2	3x3	3x3 Modified	4x4
Processor Utilization (Period)	0.69	0.3070	0.1940	0.17499
Processor Utilization (Deadline)	1.76	0.5070	0.7820	0.44318
Deadlines missed	12	0	0	0
Total Context Switches	-	1383	544	171
Total Pre-emptions	-	172	48	9
Makespan	116640	480	720	135

References

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