19L021-LOW POWER VLSI DESIGN

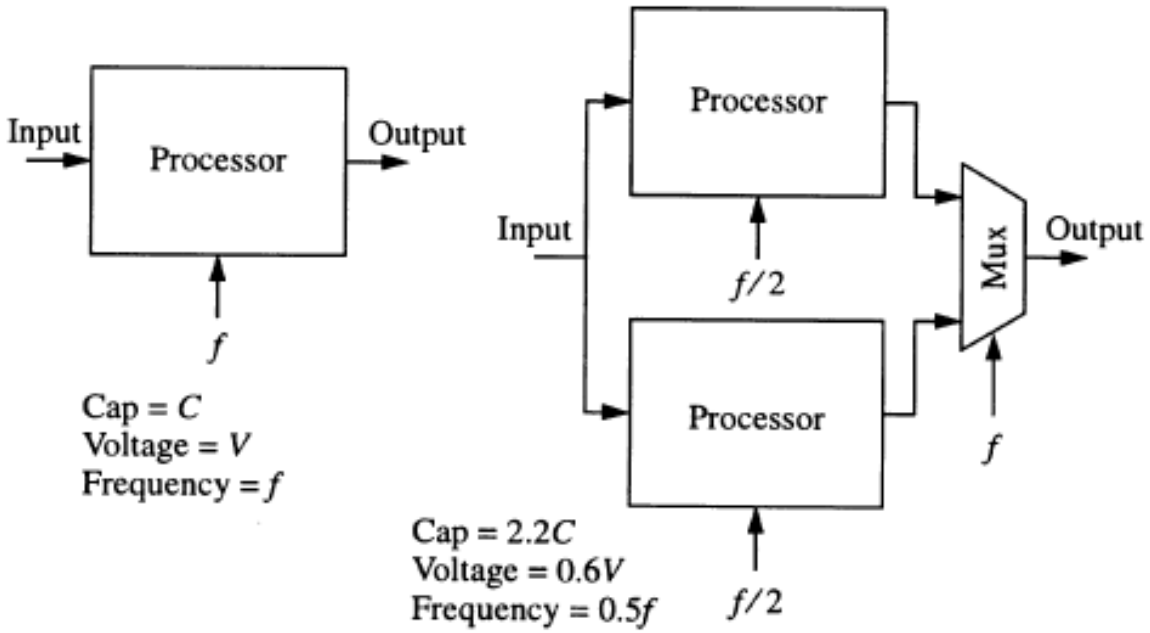
TOPIC:PARALLEL ARCHITECTURE WITH VOLTAGE REDUCTION

NEED FOR PARALLEL ARCHITECTURE

- To improve the computation throughput of high performance digital system
- Compared to a uniprocessing system, parallelism effectively increases the throughput of a system
- Since operating frequency and throughput is proportional, it *lowers* the operating frequency while maintaining the same system throughput.
- Parallelism essentially trades area off for a lower operating frequency or higher throughput
- the frequency requirement of the system is reduced, thus allowing the system designer to choose a lower operating voltage.

PARALLEL MECHANISM

- To decrease the power consumption,we go for parallelism where frequency can be reduced ,allowing the designer to choose the operating voltage.
- In parallel mechanism the processor is divided into two parts,with a reduced supply frequency f/2.



DISADVANTAGES

- Due to the use of multiplexer at the transmitter side,a demultiplexer is required at the receiver side,due to which the capacitance requirement increases
- The overall area of the system will increase ,to overcome this pipelining can be done

EFFECT IN OVERALL POWER DISSIPATION

- Normal power dissipation of unidirectional processor is given by,

$$P_{uni} = CV^2f$$

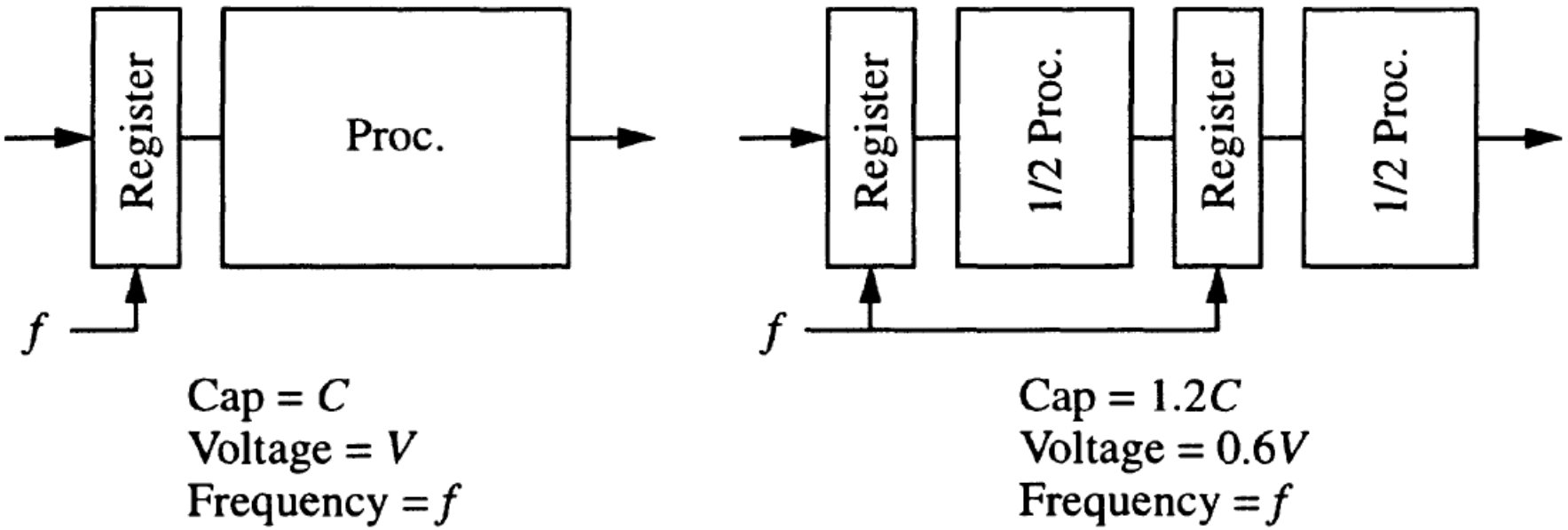
- Power dissipation after parallel processing:

$$P_{par} = (2.2C)\,(0.6V)^2\,(0.5f) = 0.396\,P_{uni}$$

- 60% of the power is saved,only 40 % of previous power isutilized
- Capacitance >twice the original capacitance

PIPELINING

- It is nothing but parallel processing without using double units



- Single frequency f is provided
- The operating voltage is reduced
- Overall supply voltage is reduced
- The capacitance is only 20% of the original capacitance
- Area overhead is also reduced
- The power dissipation is given by,

which is less when compare to parallel processing

$$P_{pip} = (1.2C)(0.6V)^2 f = 0.432\,P_{uni}$$

The generalized dynamic power dissipation is given by,

$$P_{par} = (nC)\left(\frac{V}{n}\right)^2\left(\frac{f}{n}\right) = \frac{P_{uni}}{n^2}$$

$$P_{pip} = C\left(\frac{V}{n}\right)^2 f = \frac{P_{uni}}{n^2}$$

where n is the parallelism factor

APPLICATIONS

- The general principle of parallelism is applicable to any digital systems, this low power technique is more appropriate for special purpose architecture digital signal
- Duplicating or pipelining data operators in such systems are easier compared to general purpose processors with complicated control structures.