FPGA IMPLEMENTATION OF DIGITAL FM MODEM(MODULATOR AND DEMODULATOR)

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Abstract— In this paper an FPGA implementation of a high performance programmable digital FM modem has been done for targeting towards the Software Defined Radio (SDR) application. The proposed design consists of the reprogrammable, area optimized and low-power features. The modulator and demodulator contain a compressed direct digital synthesizer (DDS) for generating the carrier frequency with spurious free dynamic range of more than 70 dB. The demodulator has been implemented based on the digital phase locked loop (DPLL) technique. The same DDS has been used for demodulating the modulated signal. The proposed FM modem has been implemented and tested using Virtex2Pro University board as a target device. Implementation of the FM modem can run maximum 103 MHz, by taking less than 8k gate equivalent in the XC2VP-30 FPGA device.

WHY FPGA FOR MODEM?

FPGA is…..

- **Reprogrammable**
- **Area optimized**
- **Having low-power features.**

Why Digital FM modulation over Analog modulation

- Traditionally analog FM modulation was used to perform the audio broadcasting. But the difficulties arise in analog FM modulation scheme due to the uses of the voltage controlled oscillator (VCO).
- Audio or voice clarity is the main concern in any audio broadcasting standards.
- Using the VCO it is very difficult to obtain a good clarity in the FM modulated or demodulated signal as VCO suffers from the lack of linearity over the desired frequency range.
- Therefore the digital implementation of FM modulation scheme has evolved to replace the traditional analog counterpart.
- the sudden departure from its linearity property of the VCO degrades the overall system performance. Hence, Digital PLL's provide the best possible solution to overcome some of the bottlenecks of analog PLL's

What is an SDR SYSTEM?

- A software-defined radio (SDR) system is a radio communication system which uses software for the modulation and demodulation of radio signals. An SDR performs significant amounts of signal processing in a general purpose computer, or a reconfigurable piece of digital electronics. The goal of this design is to produce a radio that can receive and transmit a new form of radio protocol just by running new software.

ROLE OF FPGA IN SDR SYSTEM

Digital implementation of FM demodulators in software often does not meet the demanding requirements of such communication system. An alternative solution is to implement it in FPGA, due to

- its flexibility
- modularity in nature
- A reduced area,
- Low power,

So,a high speed linear digital FM demodulator using the All Digital Phase Locked Loop (ADPLL) technique has been implemented towards the development of a SDR system

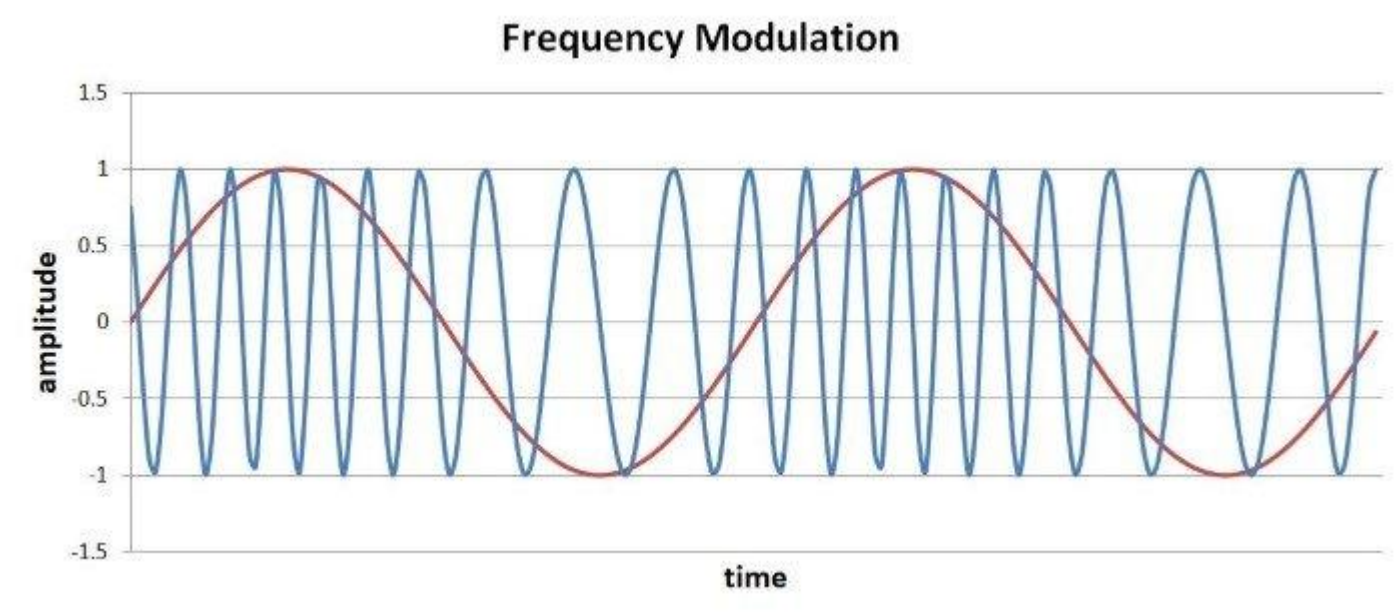
FM MODULATION AND DEMODULATION

FM MODULATION

FM MODULATION

- FM is a type of angle modulation where instantaneous frequency of the carrier signal varies linearly with the baseband modulated signal m(t)

$$S_{FM}(t) = A_c \cos\left[2\pi F_c t + 2\pi K_f \int_0^t m(n)dn\right]$$



BLOCKS IN FM MODULATION

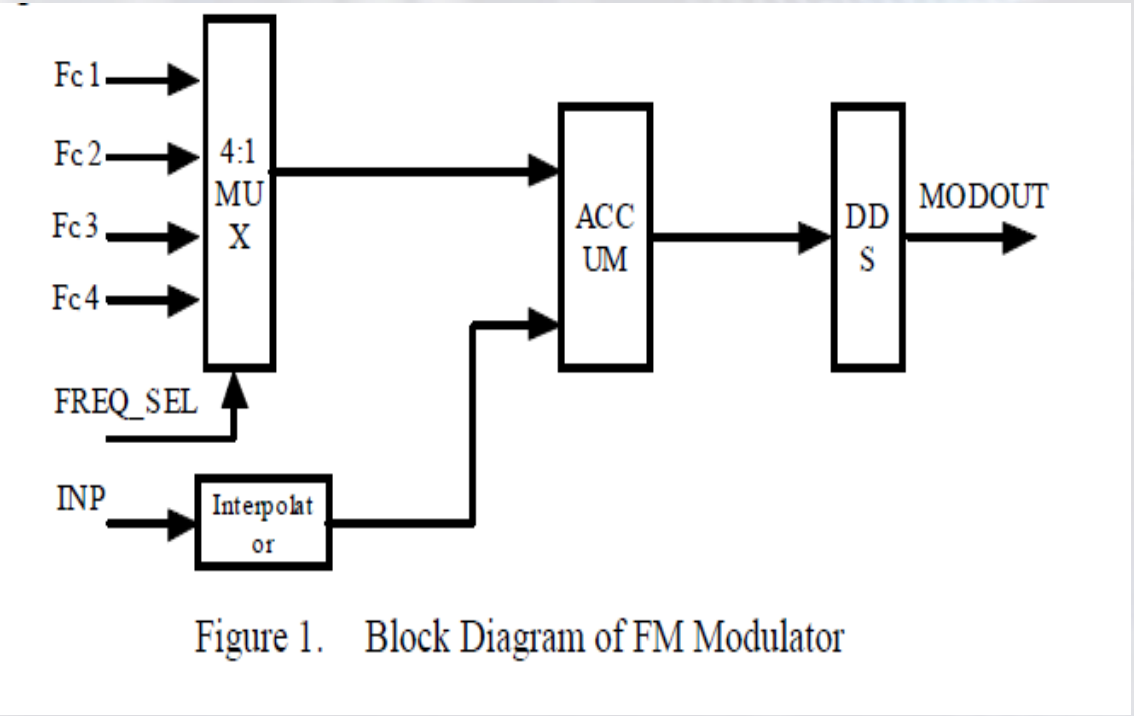
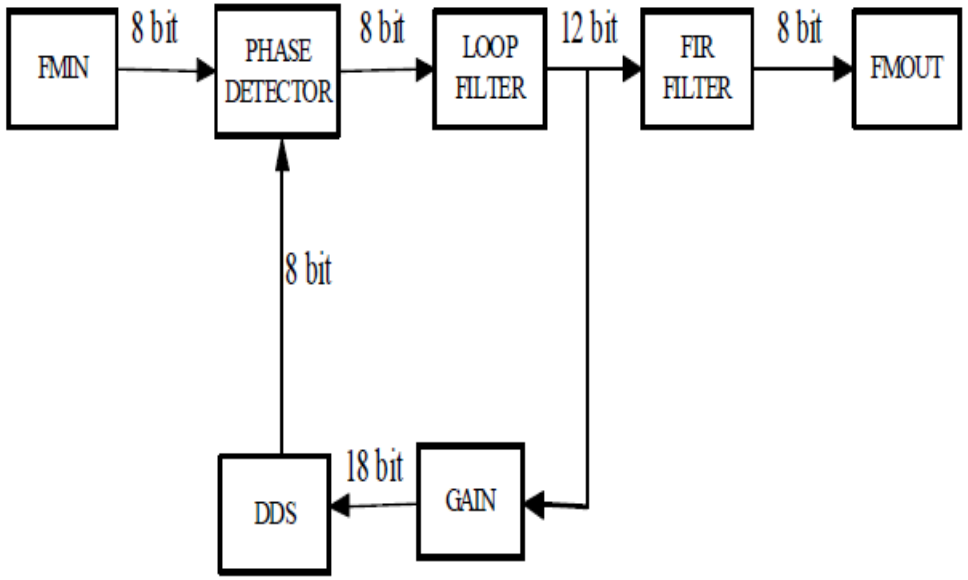


Figure 1. Block Diagram of FM Modulator

The FM modulator consists of a multiplexer, an accumulator and a DDS block. The multiplexer block has been used for generating different carrier frequency. The accumulator block accumulates the instantaneous frequency of the input message signal along with the carrier frequency and generates the corresponding phase w.r.t. input frequency. And finally DDS block take this phase as an input and generates the FM modulated signal.

FM DEMODULATION

BLOCKS IN FM DEMODULATION



$$V_i(t)=\sin(\omega_i t+\theta_i(t))$$

Feedback loop mechanism of the PLL will force DDS to generate sinusoidal signal V0(t)

$$V_0(t)=\cos(\omega_i t+\theta_0(t))$$

Multiplying the above equation using trigonometric identities,we get….

$$=\frac{K_d}{2}\left[\sin(2\omega_i t+\theta_i(t)+\theta_0(t))+\sin(\theta_i(t)-\theta_0(t))\right]$$

DIGITAL PLL AS DEMODULATOR

- The single most important point to realize while designing the PLL is that it is a feedback system and, hence,it is characterized mathematically by the same equations that are applied to other, more conventional feedback control system.The transfer function of the system is

$$\frac{Y(s)}{X(s)} = -\frac{-s^2 + s}{1.9375s^2 + 0.06161s + 0.00089}$$

- The second order DPLL system improves the performance of the loop in terms of speed and locking range as compare with the first order DPLL system. As a result of that the DPLL system used here is a second order system

PHASE DETECTOR

- The phase detector’s operation is to detect the phase error between the incoming frequency modulated signal from the ADC and the output frequency generated from the DDS.This operation needs one register and one multiplier module.The modified Booth Encoded Wallace-tree multiplier architecture is used to implement the multiplier module.

BOOTH-ENCODED WALLACE TREE MULTIPLIER

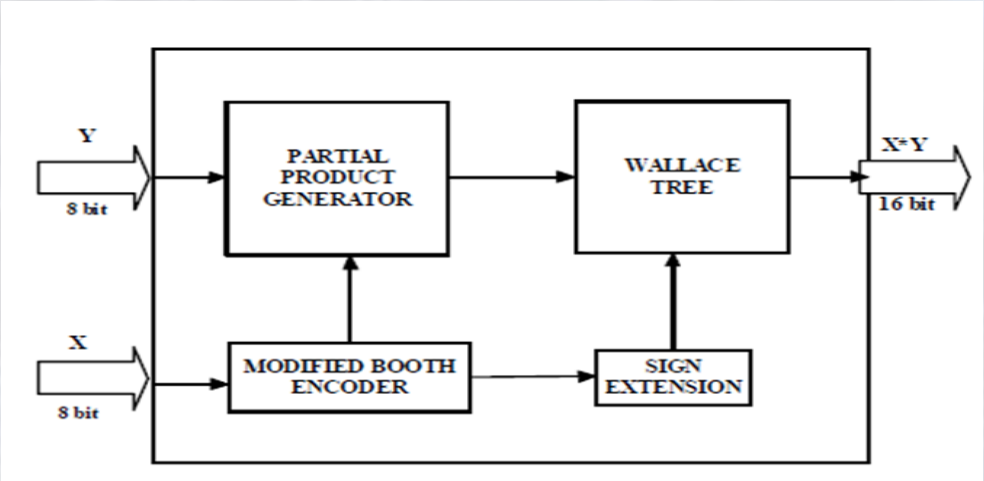


TABLE 1: Truth table of modified booth encoder.

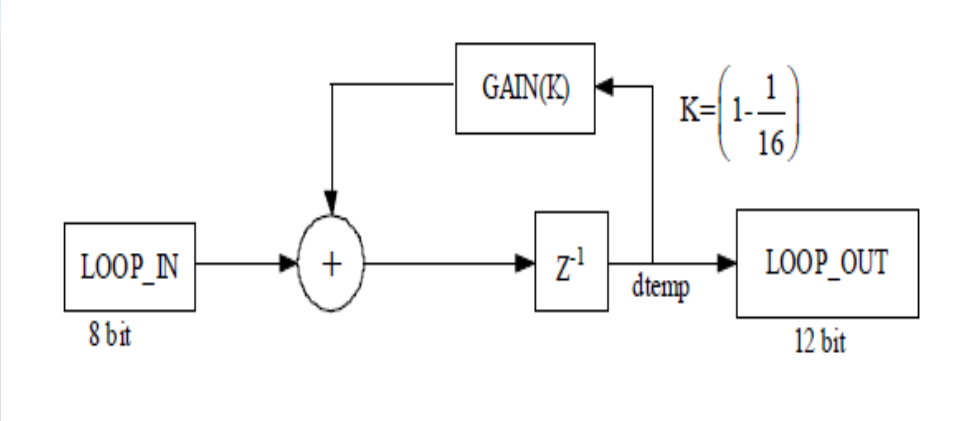
Y_{i+1}	Y_i	Y_{i-1}	Value	$X1\_b$	$X2\_b$	Neg	Z
0	0	0	0	1	0	0	1
0	0	1	1	0	1	0	1
0	1	0	1	0	1	0	0
0	1	1	2	1	0	0	0
1	0	0	−2	1	0	1	0
1	0	1	−1	0	1	1	0
1	1	0	−1	0	1	1	1
1	1	1	0	1	0	1	1

LOOP FILTER

- Loop filter, which is just a low pass filter by its characteristics, is used to remove the high frequency components in . It does the addition with the output signal from the phase detector and the register output multiplied by the coefficient

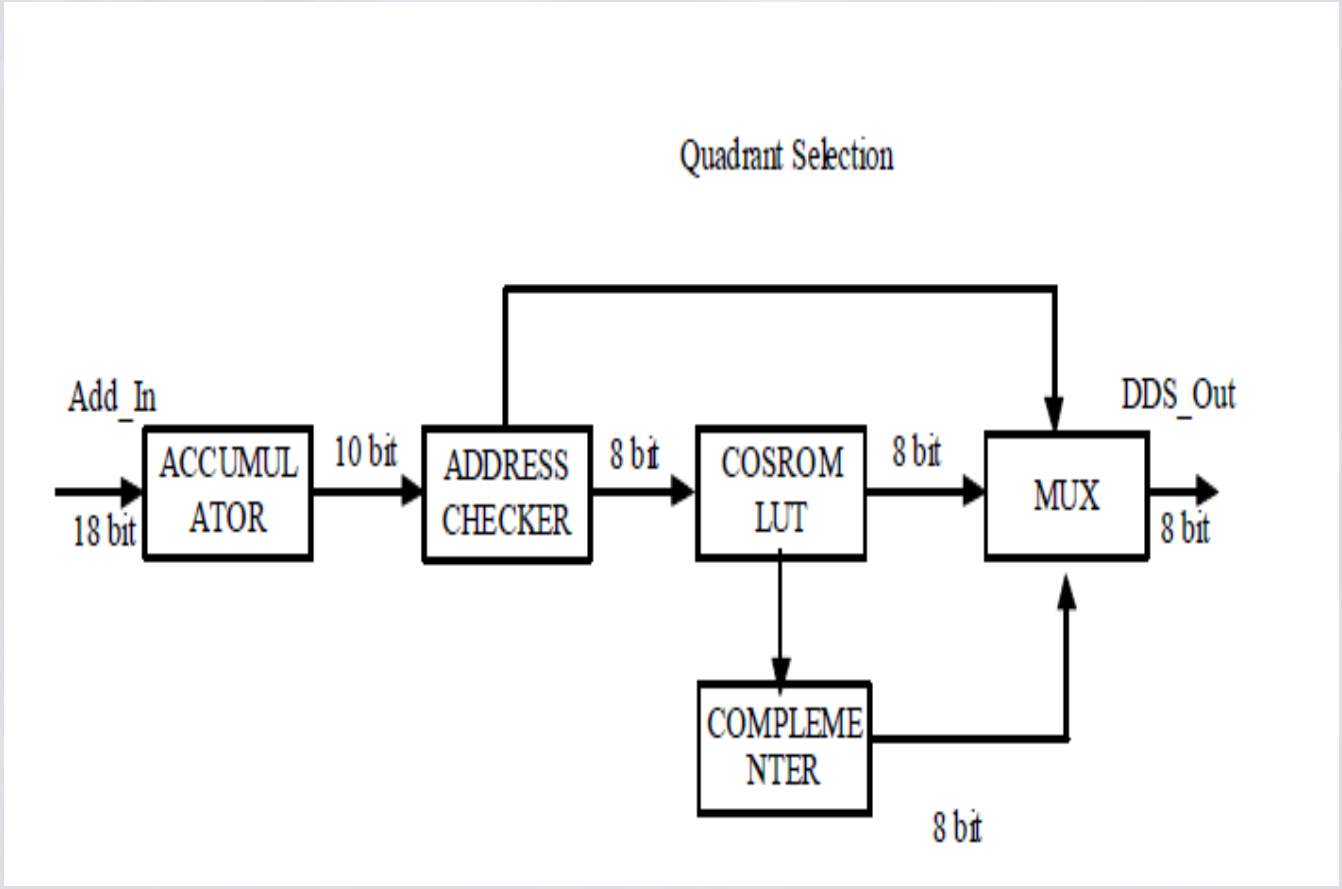
$$\alpha = (1 - 1/16) = 15/16 = .09375$$

- The intermediate signal has been chosen in such a way that the multiplication operation can be implemented by just 4 bit right shift instead of a multiplier



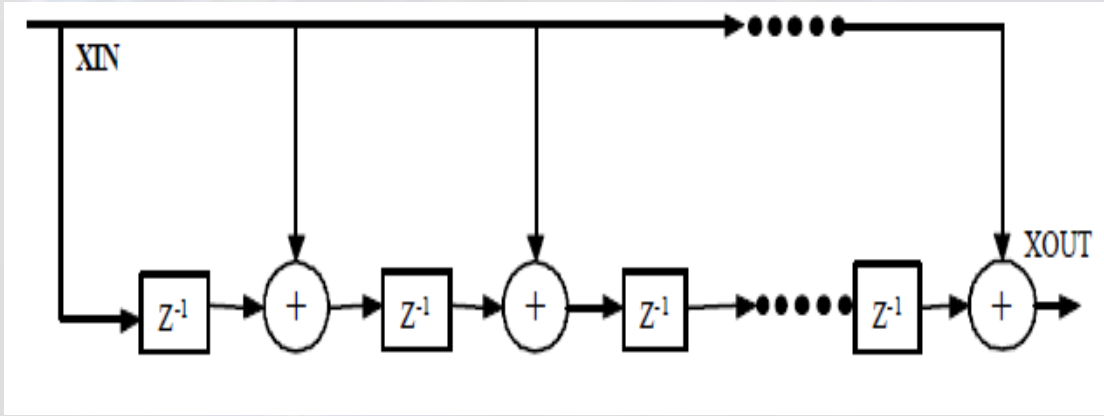
DIRECT DIGITAL SYNTHESIZER

- DDS will take the corrective error voltage, $V_d(t)$ and then shift its output frequency from its free running value to the input signal frequency w*i* and thus keep the DPLL in lock.
- The input phase will be just accumulated in the accumulator



FIR FILTER(FINITE IMPULSE RESPONSE FILTER)

- At the last stage of the receiver, low pass Finite Impulse Response (FIR) filter is used to perform the signal shaping. Here 16 tap transposed FIR filter architecture is used, as shown in Figure, This filter is essentially an average filter since its output is equal to the average value of its input over the last n-tap samples where n is the number of tap used. As in direct form digital FIR filter the total propagation delay of the circuit became more due to the addition of the 16 data samples, here transposed FIR filter architecture is chosen. Here the coefficients are the same 1/16, and in reality 1/16 can be implemented by just 4 bit right shift operation. Hence no multiplier is required.



HARDWARE IMPLEMENTATION

SYNTHESIS RESULTS

- Xilinx ISE 9.2i is used for synthesis and implementation of the circuit. Xilinx XCV2vp30-7FF896 device has been used as the target device for FPGA implementation and XST has been used as a synthesis tool and XPower has been used for the power calculation. The power is being calculated by simulation based switching activities of the all the signals.

TABLE I. TIMING, AREA & POWER RESULTS FOR 2VP30-7FF896

	AREA				TIMING (MHz)	POWER (mW)
	Slices	FFs	LUTs	Gates		
FM Modulator	34	9	54	582	144	124.92
FM Demodulator	336	447	479	7,774	105.5	129.27

FPGA RESOURCE USAGE COMPARISON RESULT

Xilinx 3S200FT256-4	Time		Area		
	Delay (ns)	Frequency (MHz)	Slices	Slice FFs	LUTs
PLL(optimized) [7]	9.725	102.828	491	548	721
Sigma Delta Arch.[9]	2427 out of 3071 slices in Xilinx Virtex2 XC2V500 device				
Proposed Implementation	12.453	80.30	353	448	486
	349 out of 3072 slices in Xilinx Virtex2 XC2V500 device				

AREA UTILIZATION COMPARISON WITH OTHER FM DEMODULATOR IMPLEMENTATION [5-6]

Without Optimization /No of Gate		With Optimization /No of Gate	
Proposed Design	Existing Architecture	Proposed Design	Existing Architecture
Phase Detector: 389	Phase Detector: 422	Phase Detector: 413	Phase Detector: 616
Loop Filter: 202	Loop Filter: 200	Loop Filter: 277	Loop Filter: 297
FIR: 3213	FIR: 2367	FIR: 3696	FIR: 3511
DDS: 684	DDS: 1534	DDS: 828	DDS: 1833
Total FM: 4920	Total FM: 10545	Total FM: 6052	Total FM: 14314

By optimizing the basic components of the FM receiver, the reduction of the hardware usage and improvement in the performance has been done

TIMING ANALYSIS COMPARISON WITH OTHER FM RECEIVER IMPLEMENTATION [5-6]

Without Optimization		With Optimization	
Proposed Design	Pervious Architecture	Proposed Design	Previous Architecture
Operating Frequency (clock) 149.4 MHz	Operating Frequency (clock) 143.7 MHz	Operating Frequency (clock) 158.1 MHz	Operating Frequency (clock) 155.8MHz

CONCLUSION

The proposed VLSI implementation of high performance digital phase locked loop based FM receiver has been designed so that it can meet the constraint for the application in

- personal wireless communication
- very high frequency signal processing field.

The proposed design takes only 108.67mW power for running in the 100 MHz frequency. The circuit requires only 7.8K gates for implementation and it can operate at maximum frequency of 105 MHz.

Thank you