وَمَا أُوتِيتُمْ مِنَ الْعِلْمِ إِلَّا قَلِيلًا

Ain Shams University – Faculty of Engineering – ECE Dept. – Integrated Circuits Lab.
Dr. Hesham Omran

Analog/Mixed-Signal Simulation and Modeling
Lab 04
Analog Design Automation

Objectives

1. Learn how to systematically design analog circuits using the gm/ID design methodology and precomputed LUTs.
2. Create a knowledge-based synthesis script that automates OTA design using LUTs.
3. Design OTAs using ADT Device Xplore and gm/ID design charts.

Instructions

1. Use MATLAB or Octave to write your codes.
2. Use LTSpice for design entry and simulation. You may use Notepad++ to write your netlist (it has SPICE highlight mode). Do NOT use a schematic entry GUI.
3. Download Murmann's gm/ID Starter Kit (https://web.stanford.edu/~murmann/gmid).
   - Read the documentation and the help of the lookup function.
   - Use the 180 nm SPICE model and the LUTs included in Murmann's gm/ID starter kit.
   - You may need to edit the code if you will use Octave.
4. Download ADT:
   - Go to https://adt.master-micro.com
   - Register using your university or corporate email address. If you are a student or fresh grad, select academia as your organization type. If you don't have a university or corporate email address then register as unemployed and include your LinkedIn profile URL, but your account may take some time to get reviewed and approved.
   - Read ADT readme file. Visit ADT website again and generate a free personal license.
   - **Use the LTspice example LUTs included in ADT. Do NOT generate new LUTs.**
5. Watch the following playlist:
   https://youtube.com/playlist?list=PLMSBalys69ywdpmcih1yP4hboBLY4-iCr
6. Watch Lecture 14 in the Analog IC Design (1) Course:
   https://youtube.com/playlist?list=PLMSBalys69yzp1vrmnYAmpRFiptbuGuaj
7. **Optional:** Read the following paper:
   https://www.sciencedirect.com/science/article/pii/S0026269217307905.

Part 1

Index	Deliverable
1.	Using ADT Device Xplore, plot the following design charts vs gm/ID for both PMOS and NMOS. Set VDS = VDD/3 and L = 0.18u,0.5u:0.5u:2u 1) gm/gds 2) ID/W 3) gm/Cgg (use advanced Y expression) 4) VGS

2.	Use ADT Device Xplore to find ID and VGS of an NMOS that has gm/ID = 10, gm/gds = 50, VDS = VDD/3, VSB = 0, and W = 5u.
3.	Complete the script "lookup_test.m" to repeat the previous problem. Compare the results in a table.
4.	Use ADT Device Xplore to design an **NMOS-input 5T-OTA** with the following specs: • AVDC = 34 dB, GBW = 100 MHz, CL = 500 fF Assume VDD = 1.8V. Ignore the body effect and the OTA self-loading. Make any reasonable assumptions whenever necessary and clearly explain your assumptions. You can make the following reasonable assumptions: • gm/ID = 15 for the input pair and gm/ID = 10 for the load and the tail bias **(why is this reasonable?)**. • ro of the load is five times ro of the input pair **(why is this reasonable?)**. • L = 1um for the tail bias **(why is this reasonable?)**. Report the design charts you used and use cursors to clearly show your design points.
5.	Complete the function "designOTA.m". This is a function that automates the design of an NMOS-input 5T-OTA using Murmann's gm/ID starter kit. The function takes a single structure (SPEC) as input. SPEC has the following fields: DC gain (AVDC), gain-bandwidth product (GBW), and load capacitance (CL). The function returns a single structure OTA that contains the bias current and the sizing (W and L) of the OTA transistors. Report your MATLAB function.
6.	Complete the script "designOTA_test.m". This is a script that calls your synthesis function and prints the output clearly in the command window. Use the script "designOTA_test.m" to design the OTA you designed using ADT Device Xplore. Use the same assumptions you used in the previous part. Report your script. Report the output of the command window. Compare the results to the results obtained by ADT Device Xplore.
7.	Complete the netlist "ota_tb.cir" to simulate your synthesized OTA. Simulate the differential gain vs frequency (annotate DC gain and GBW) and compare the simulator output with the required specifications. Report your netlist, the simulation results, and the comparison table. Comment on the results.

Part 2

Index	Deliverable
1.	Use ADT Device Xplore to redesign the previous OTA while taking into account the OTA self-loading (optional: you can also consider the body effect). Report the design charts you used and use cursors to clearly show your design points. Compare the results to the results obtained in Part 1.
2.	Copy your "designOTA.m" script to a new one "designOTA2" and edit it to take into account the new requirements. Use the same assumptions you used in the previous part. Use the script "designOTA_test.m" to re-design the OTA. Report the output of the command window. Compare the results to the results obtained in Part 1. Compare the results to the results obtained by ADT Device Xplore.
3.	Write a netlist for the synthesized OTA. Simulate the differential gain vs frequency (annotate DC gain and GBW) and compare the simulator output with the required specifications. Report your netlists, the simulation results, and the comparison table. Comment on the results.

Thanks to all who contributed to these labs. If you find any errors or have suggestions concerning these labs, please contact Hesham.omran@eng.asu.edu.eg.