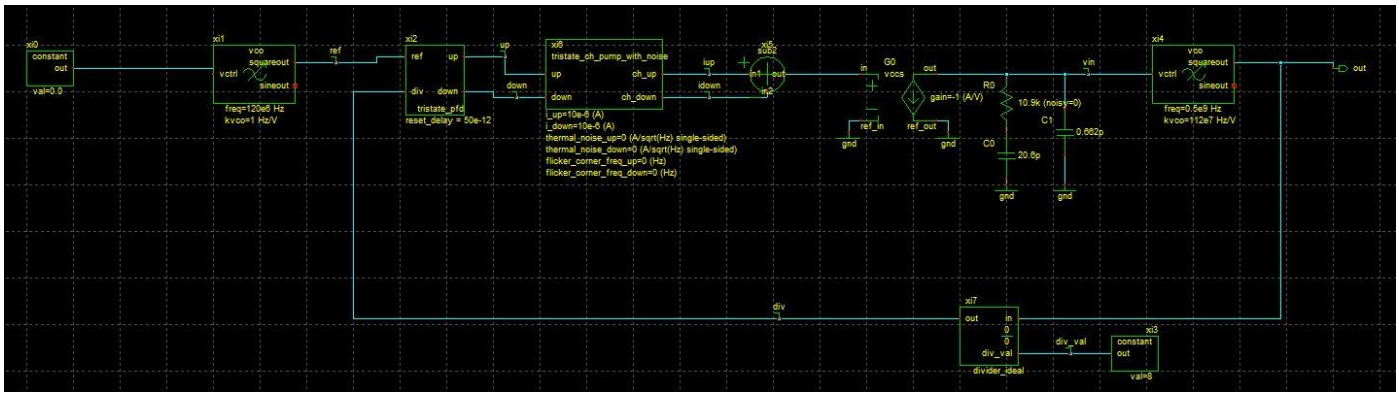
Lab 06: PLL System-Level Design and Simulation

Part (1)

(1)



(2)

Kvco = 1.12 GHz/V

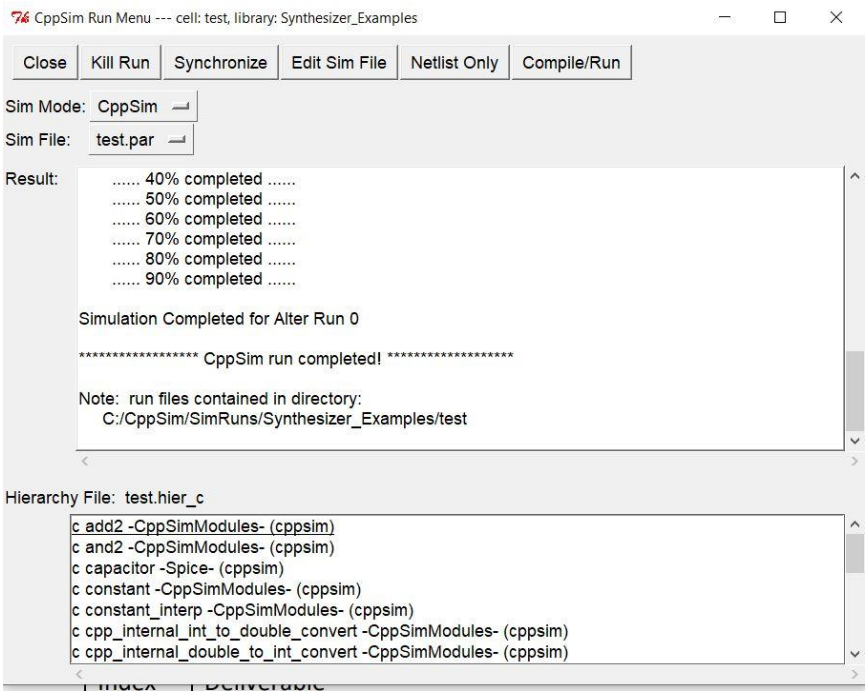
(3)

Fout = Fo + Kvco*Vin

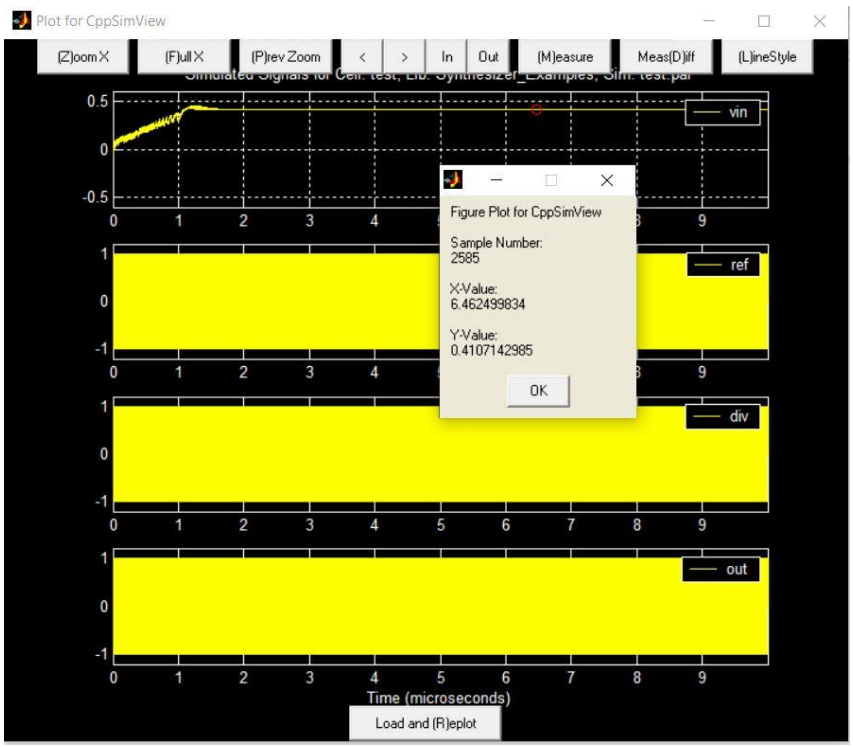
960M = 500M + Kvco*Vin

Vin = (960M - 500M)/(1.12G) = **0.4107142857 V**

(4)



(5)

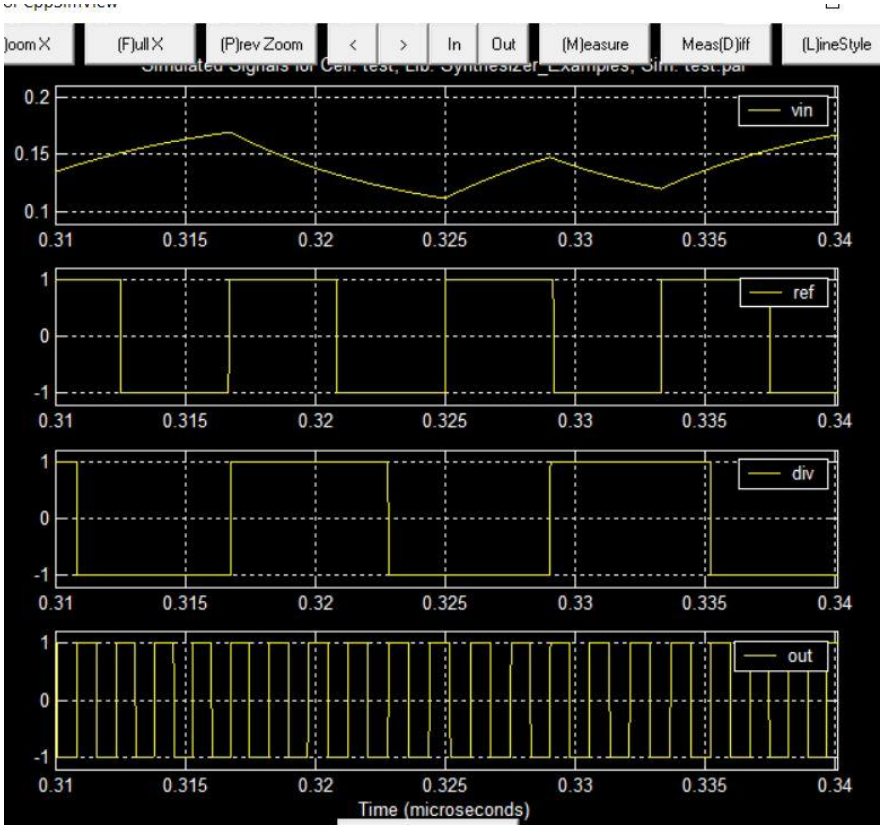


(6)

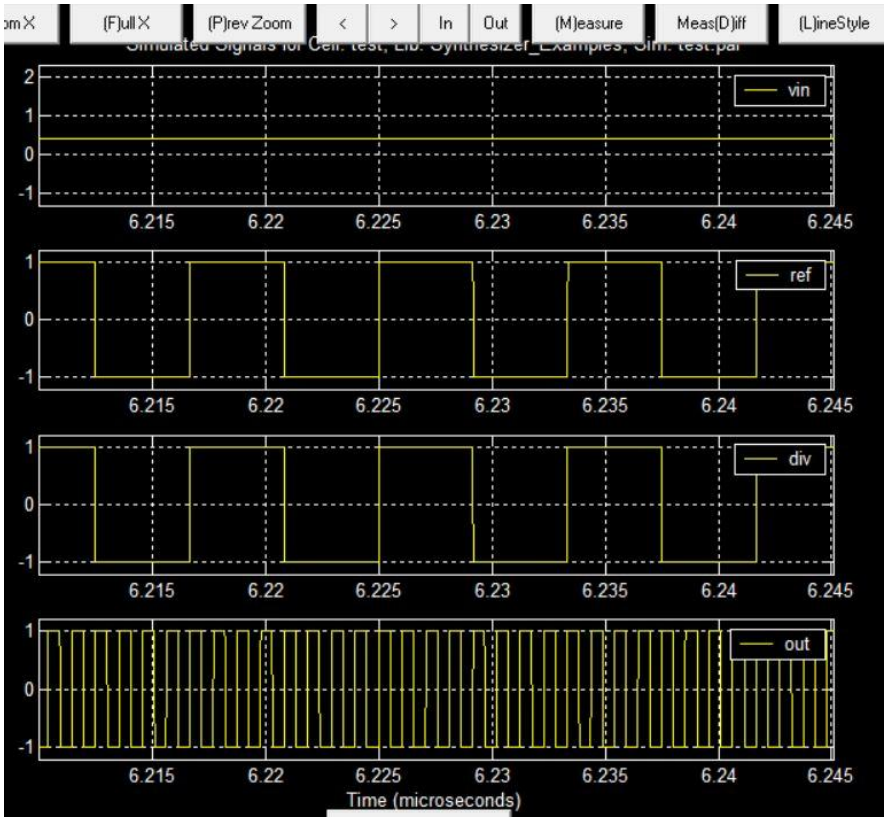
	Analytical	**Simulation**
vin value (V)	0.4107142857	0.4107142985

Both the analytical and simulated values are the same.

(7) Before lock:

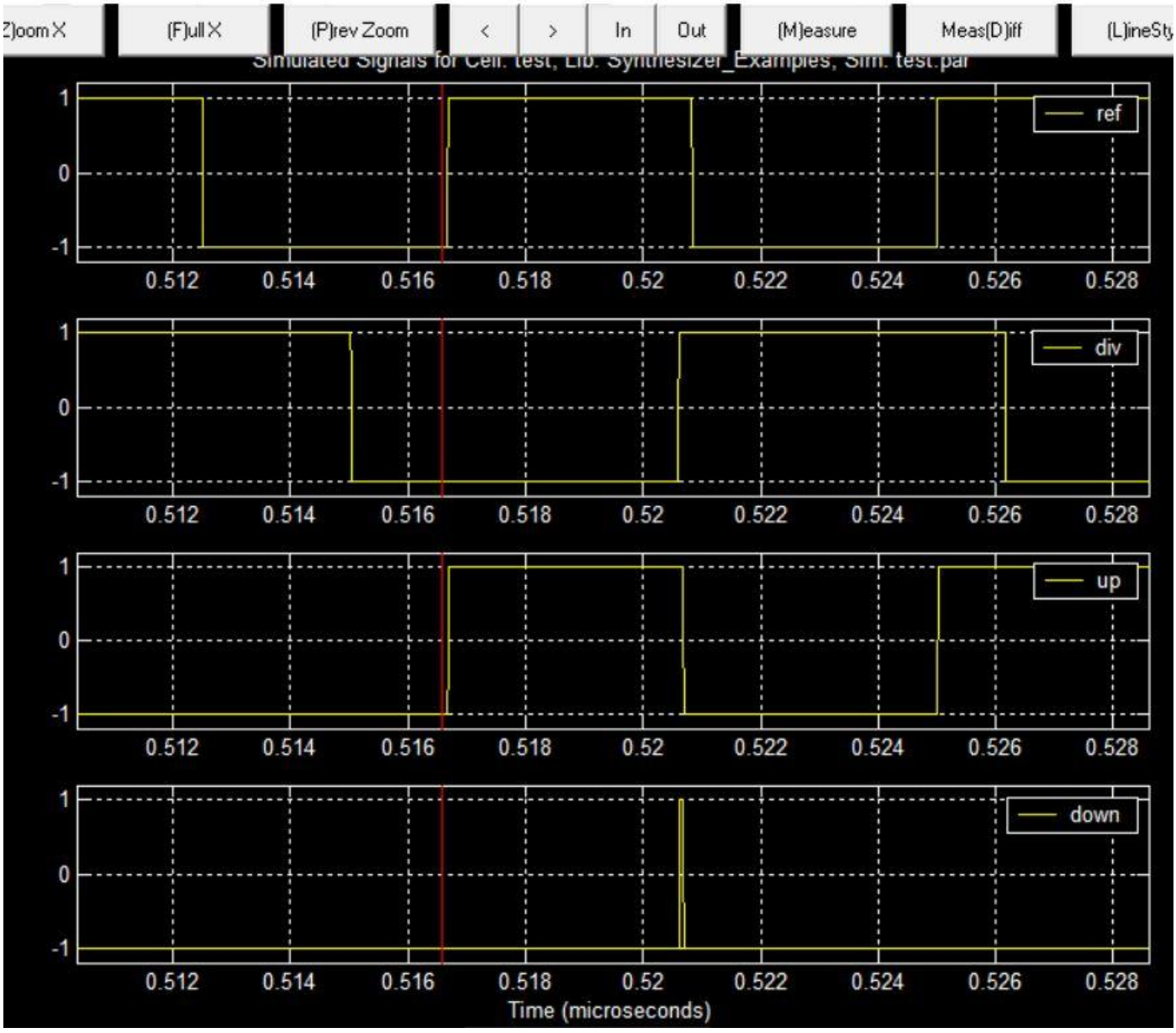


(8) After lock:



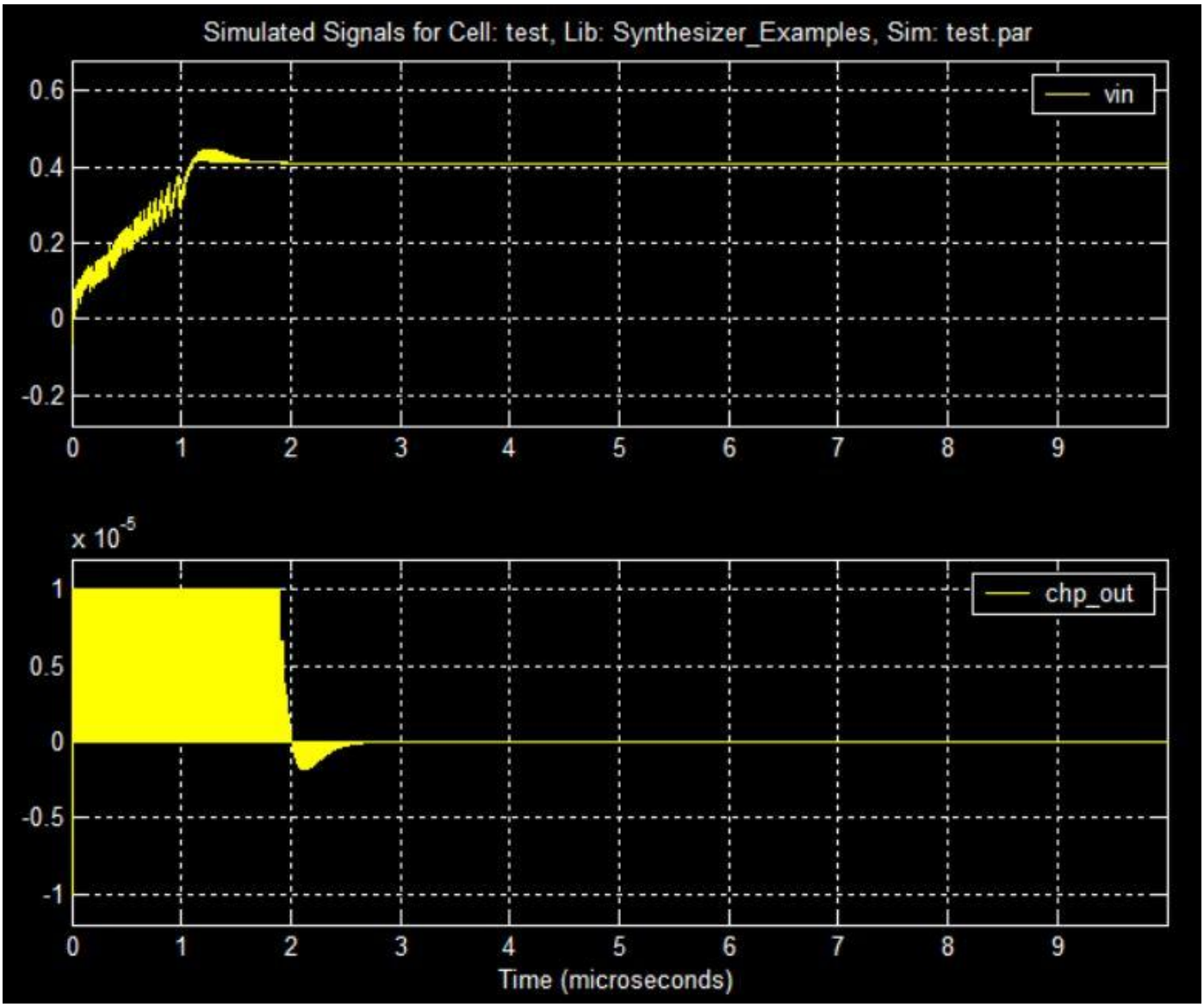
Part (2)

(1)



As shown in the figure, at the positive edge of "ref", "up" is asserted until there is a positive edge for "div", then "down" is also asserted, and after the reset delay, both are deasserted.

(2)


Simulated Signals for Cell: test, Lib: Synthesizer_Examples, Sim: test.par
vin
0.6
0.4
0.2
0
-0.2
0
1
2
3
4
5
6
7
8
9
x 10^-5
chp_out
1
0.5
0
-0.5
-1
0
1
2
3
4
5
6
7
8
9
Time (microseconds)