Lab 03

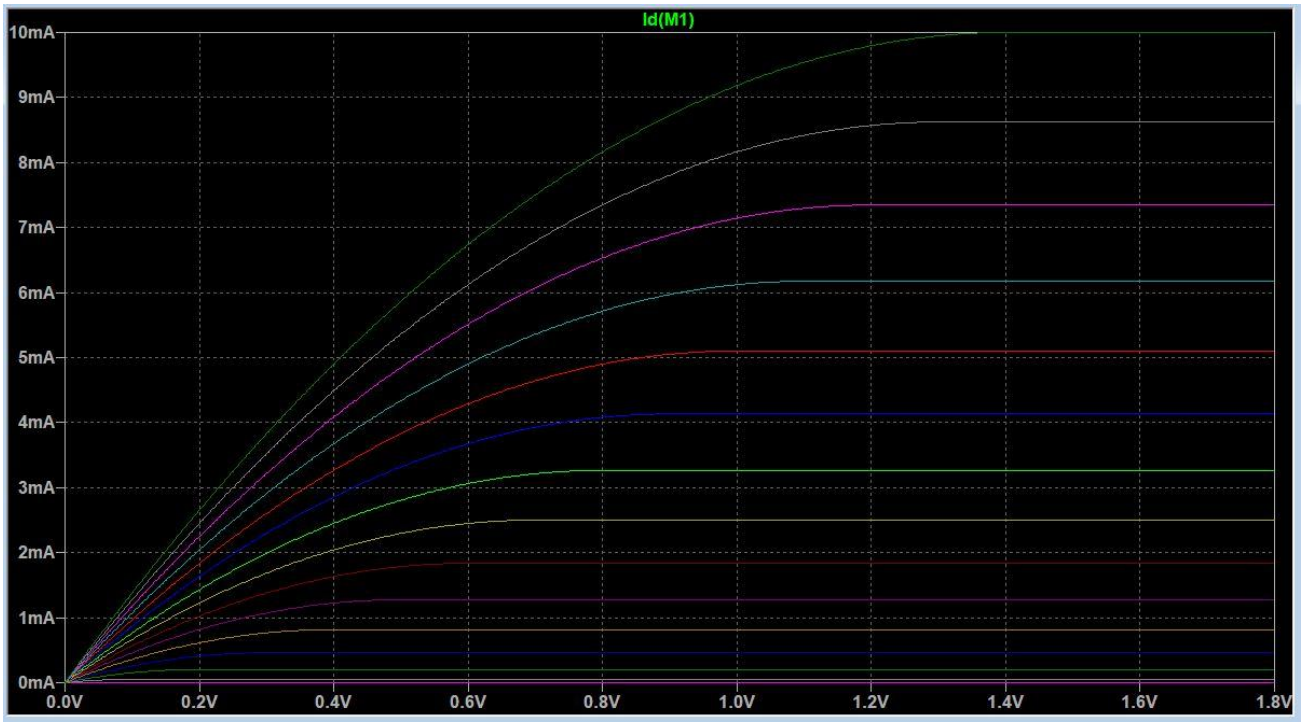
Part (1)

my_nmos.lib

```
*---------------------------------*
* Part 1.1
.model nmos_part1_1 NMOS [LEVEL=1 Kp=183.67346u Vto=0.4]

*---------------------------------*

* Part1.2
* add a line here (same as Part 1.1 except for one more parameter)
* Don't forget to change the model name to nmos_part1_2
.model nmos_part1_2 NMOS [LEVEL=1 Kp=183.67346u Vto=0.4 Lambda=0.1]
*---------------------------------*

* Part 1.3
*.add a line here (same as Part 1.2 except for one more parameter)
.model nmos_part1_3 NMOS [LEVEL=3 Kp=183.67346u Vto=0.4 Lambda=0.1 Vmax=4.28e5]
*---------------------------------*

* Part 1.6
* add a line here (same as Part 1.3 but you have to add CJ and CJSW. Take care of the units)
.model nmos_part1_6 NMOS [LEVEL=3 Kp=183.67346u Vto=0.4 Lambda=0.1 Vmax=4.28e5 Cjsw=0.1n Cj=1m]
*---------------------------------*
```

1. ### nmos_tb.cir

```
NMOS testbench

* add a line here to include the model library
.LIB my_nmos.lib
** Circuit Description **

VGS 1 0 DC 1.8V
* add a line here (VDS source)
VDS 2 0 DC 1.8V
* add a line here (MOSFET instantiation)
M1 2 1 0 0 nmos_part1_1 L=180n W=10u

** Analysis Requests **
* add a line here to do the nested DC sweep
.DC VDS 0V 1.8V 1mV VGS 0V 1.8V 100mV
.Plot DC I(VDS) V(1)
.END
```

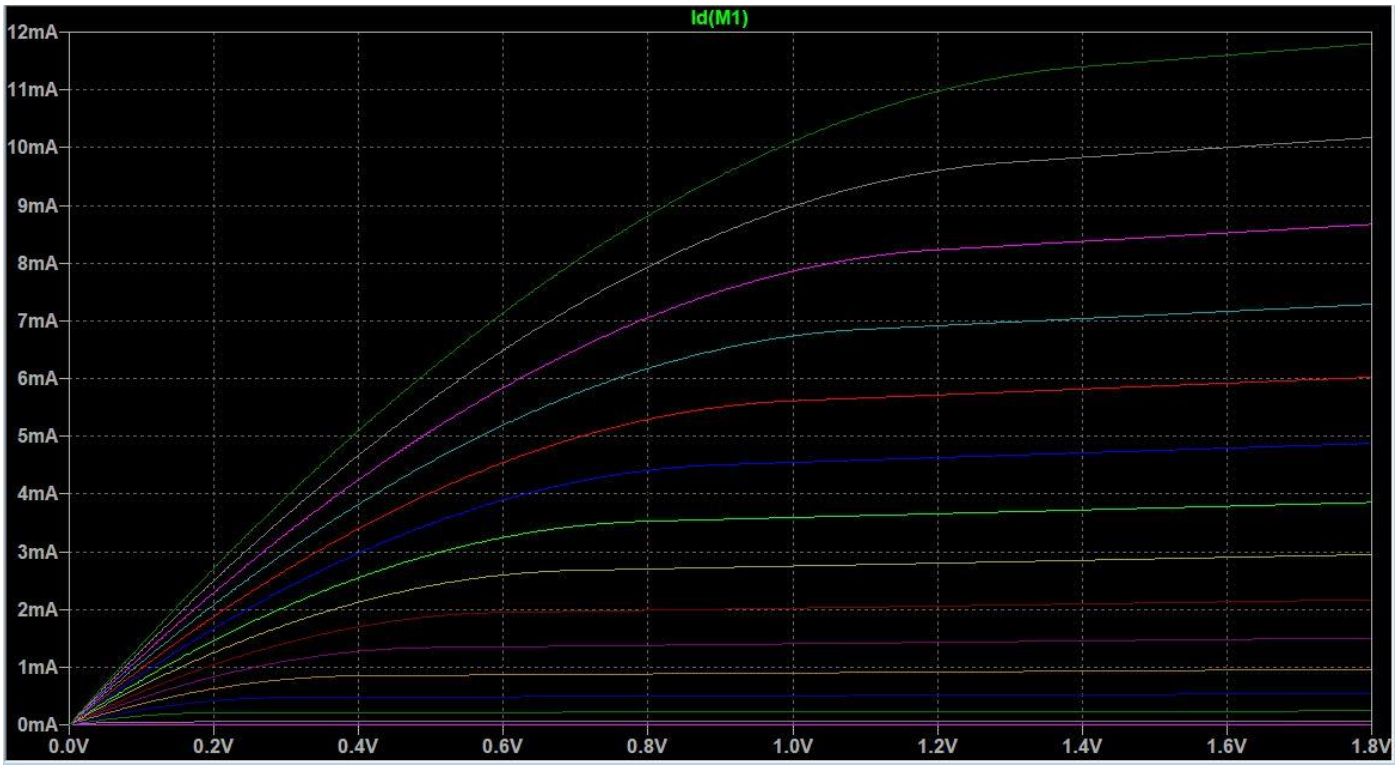



```
Instance "m1": Length shorter than recommended for a level 1 MOSFET.
```

The warning is about the 180nm MOSFET that suffers from short-channel effects not included in the models of LEVEL 1.

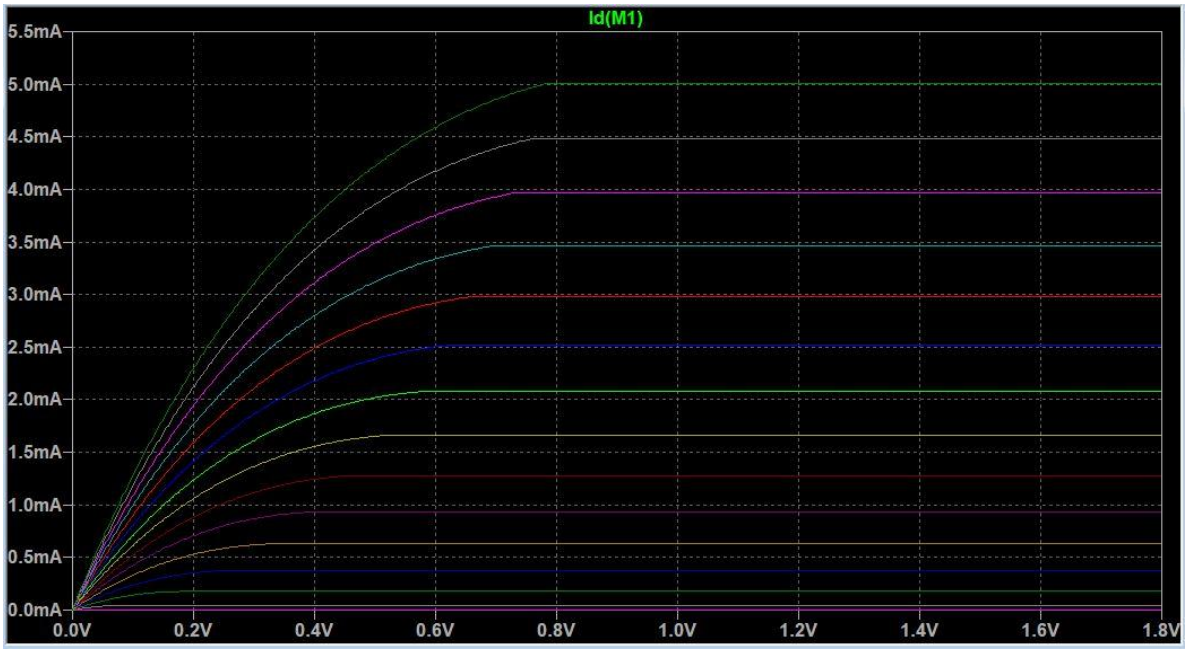
2.

```
NMOS testbench

* add a line here to include the model library
.LIB my_nmos.lib
** Circuit Description **

VGS 1 0 DC 1.8V
* add a line here (VDS source)
VDS 2 0 DC 1.8V
* add a line here (MOSFET instantiation)
M1 2 1 0 0 nmos_part1_2 L=180n W=10u

** Analysis Requests **
* add a line here to do the nested DC sweep
.DC VDS 0V 1.8V 1mV VGS 0V 1.8V 100mV
.Plot DC I(VDS) V(1)
.END
```



3.

```
NMOS testbench

* add a line here to include the model library
.LIB my_nmos.lib
** Circuit Description **

VGS 1 0 DC 1.8V
* add a line here (VDS source)
VDS 2 0 DC 1.8V
* add a line here (MOSFET instantiation)
M1 2 1 0 0 nmos_part1_3 L=180n W=10u

** Analysis Requests **
* add a line here to do the nested DC sweep
.DC VDS 0V 1.8V 1mV VGS 0V 1.8V 100mV
.Plot DC I(VDS) V(1)
.END
```



4.

the polarity of vt0 should be negative.

my_pmos.lib

my_pmos.lib

```
.model pmos_part1_1 PMOS [LEVEL=1 Kp=91.83673u Vto=-0.4 Lambda=0.1]
.model pmos_part1_2 PMOS [LEVEL=1 Kp=91.83673u Vto=-0.4 Lambda=0.1 Cjsw=0.1n
```

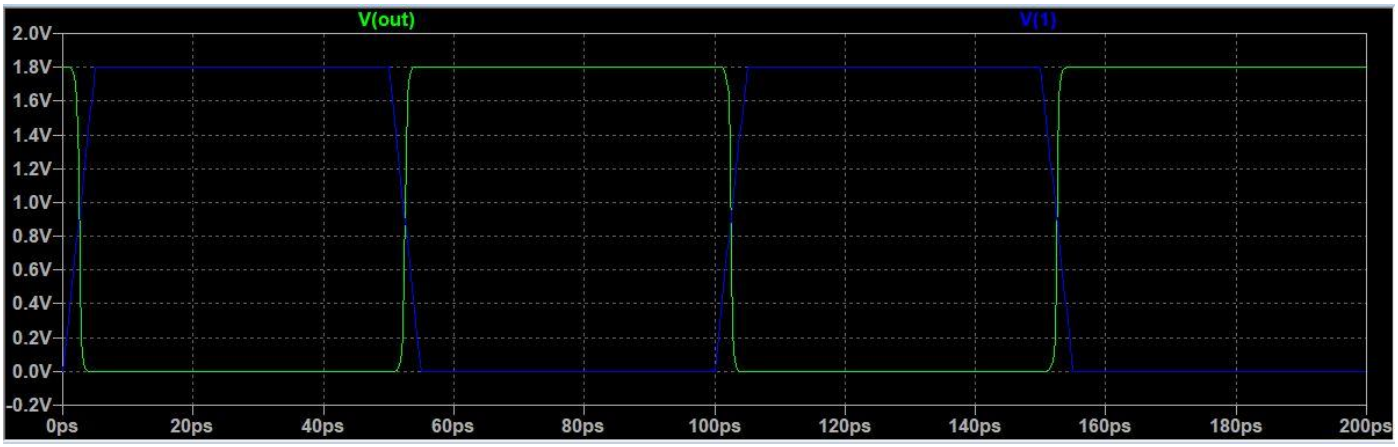
cmos_inv_dc.cir

```
CMOS inverter DC sweep

** Circuit Description **
* power supply
*add a line here
Vsupply VDD 0 1.8V
* input
VIN 1 0 DC 0V
* circuit

*add two lines here (NMOS and PMOS instantiation)
M1 OUT 1 0 0 nmos_part1_2 L=180n W=10u
M2 OUT 1 VDD VDD pmos_part1_1 L=180n W=20u
*add a line here include the model file
.LIB my_nmos.lib
.LIB my_pmos.lib
** Analysis Requests **
.DC VIN 0 1.8 0.05

** Outputs Requests **
*.PROBE

.END
```

5.

```
CMOS inverter tran analysis

* add a line here include the model file
.LIB my_nmos.lib
.LIB my_pmos.lib
** Circuit Description **

VDD 2 0 DC 1.8V

* add a line here (pulse source)
Vpulse 1 0 PULSE(0 1.8 0 5p 5p 45p 100p)
* add two lines here (NMOS and PMOS instantiation )
M1 OUT 1 0 0 nmos_part1_2 L=180n W=10u
M2 OUT 1 2 2 pmos_part1_1 L=180n W=20u
*M1 OUT 1 0 0 nmos_part1_6 L=180n W=10u AD=4.5p AS=4.5p PD=20.9u PS=20.9u
*M2 OUT 1 2 2 pmos_part1_2 L=180n W=20u AD=4.5p AS=4.5p PD=20.9u PS=20.9u
** Analysis Requests **
*add a line here (use transient analysis for two periods)
.TRAN 1p 200p
.MEAS TRAN delay TRIG when V(1)=0.9 cross=1 TARG when V(OUT)=0.9 cross=1
.END
```

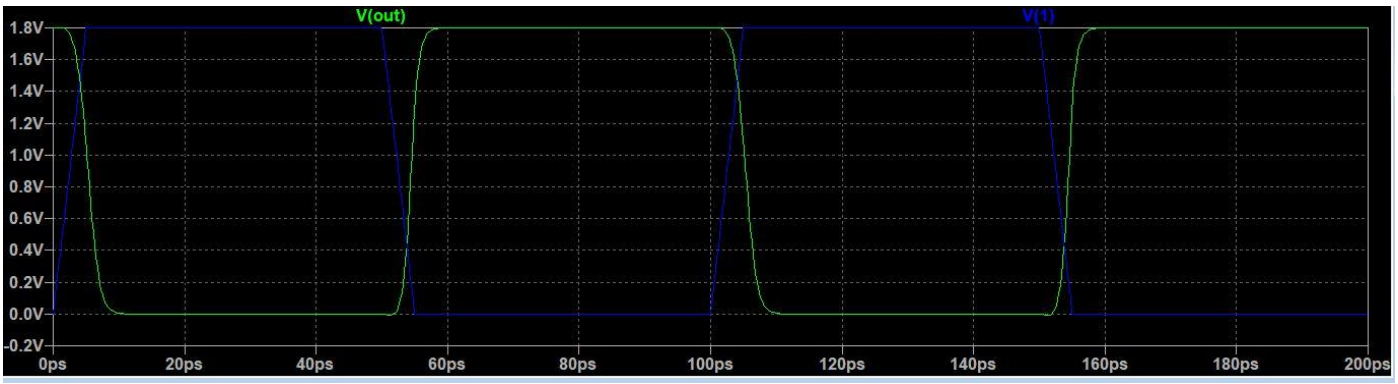
```
delay=1.4684e-015 FROM 2.5e-012 TO 2.50147e-012
```



6.

```
CMOS inverter tran analysis

* add a line here include the model file
.LIB my_nmos.lib
.LIB my_pmos.lib
** Circuit Description **

VDD 2 0 DC 1.8V

* add a line here (pulse source)
Vpulse 1 0 PULSE(0 1.8 0 5p 5p 45p 100p)
* add two lines here (NMOS and PMOS instantiation )
*M1 OUT 1 0 0 nmos_part1_2 L=180n W=10u
*M2 OUT 1 2 2 pmos_part1_1 L=180n W=20u
M1 OUT 1 0 0 nmos_part1_6 L=180n W=10u AD=4.5p AS=4.5p PD=20.9u PS=20.9u
M2 OUT 1 2 2 pmos_part1_2 L=180n W=20u AD=4.5p AS=4.5p PD=20.9u PS=20.9u
** Analysis Requests **
*add a line here (use transient analysis for two periods)
.TRAN 1p 200p
.MEAS TRAN delay TRIG when V(1)=0.9 cross=1 TARG when V(OUT)=0.9 cross=1
.END
```

```
delay=2.83618e-012 FROM 2.5e-012 TO 5.33618e-012
```

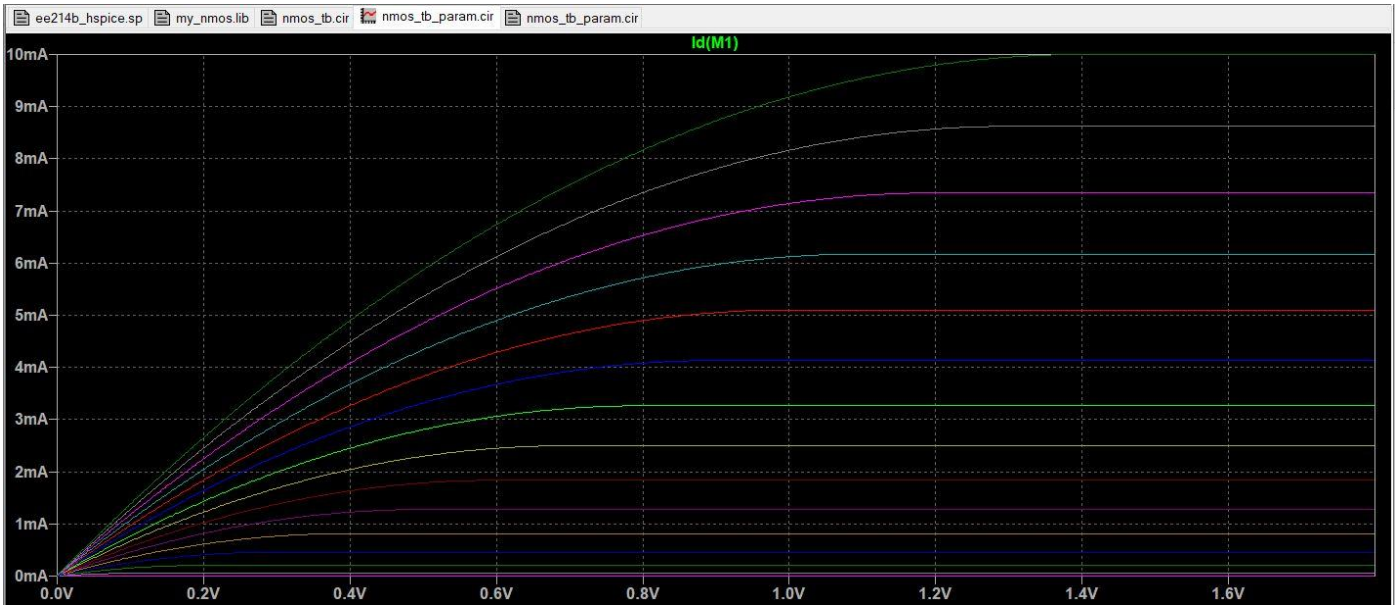


Comment: When the parasitic capacitances are included, the delay increases.

Part (2)

1.

```
* add a line here to include the model library
.LIB my_nmos.lib
** Circuit Description **

VGS 1 0 DC 1.8V
* add a line here (VDS source)
VDS 2 0 DC 1.8V
* add a line here (MOSFET instantiation)
M1 2 1 0 0 nmos_part1_1 L=180n W=10u

** Analysis Requests **
*.DC VDS 0V 1.8V 1mV VGS 0V 1.8V 100mV
.OP
.STEP VDS 0V 1.8V 1mV VGS 0V 1.8V 100mV
.Plot DC I(VDS) V(1)
.END
```



The simulation time of the parametric sweep is much longer than the nested DC sweep.

Time of parametric sweep,

```
Total elapsed time: 221.811 seconds.
```

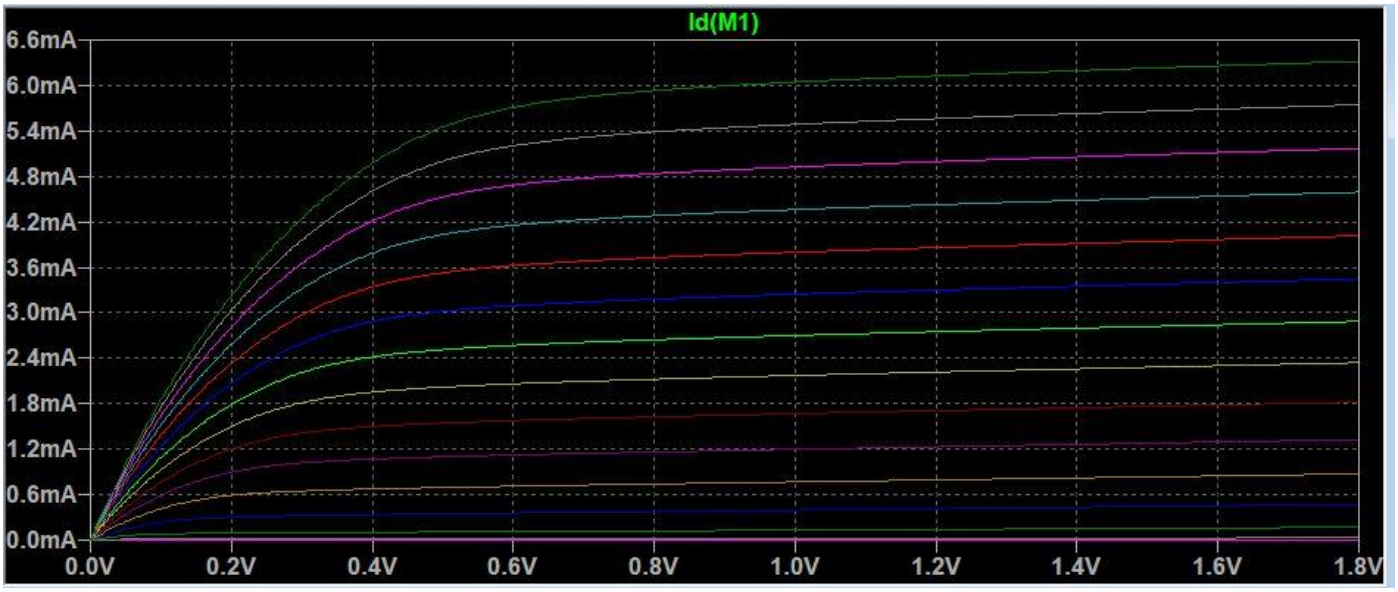
Time of nested DC,

```
Total elapsed time: 1.446 seconds.
```

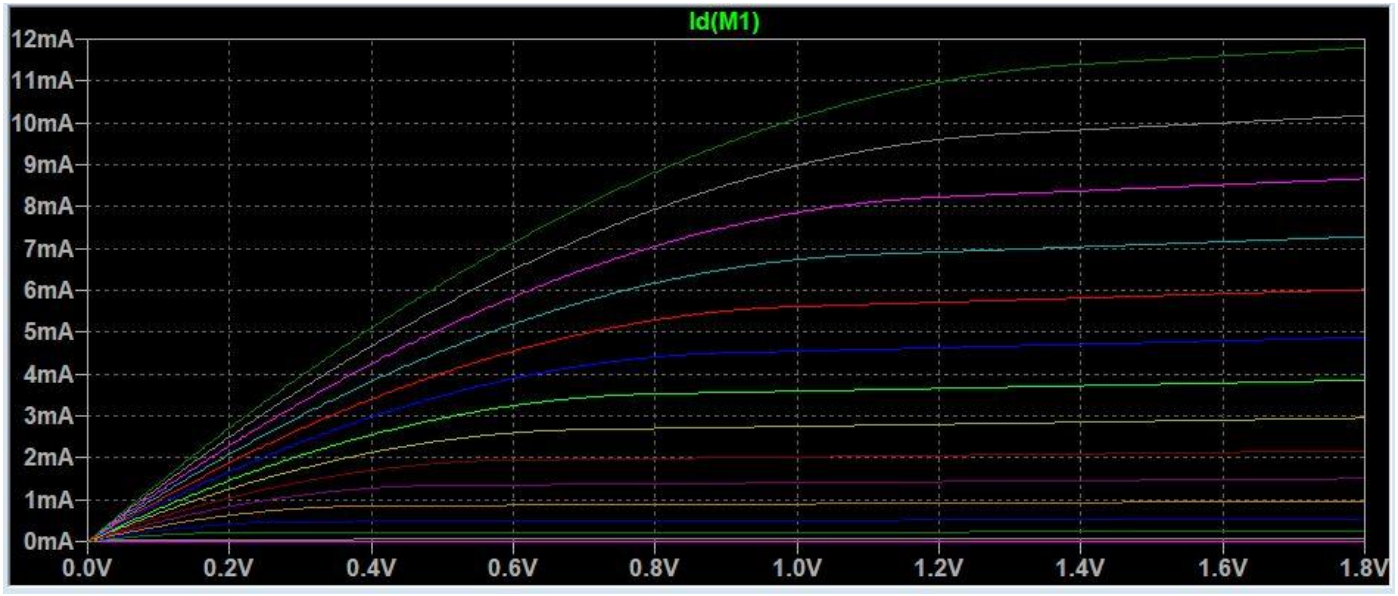
2.

- Level 49 in HSPICE is an HSPICE-enhanced version of BSIM3v3.
- To set the level parameter appropriately in LTspice, BSIM3v3.3.0 is level 8.

BSIM3v3.3.0



My level 1 model

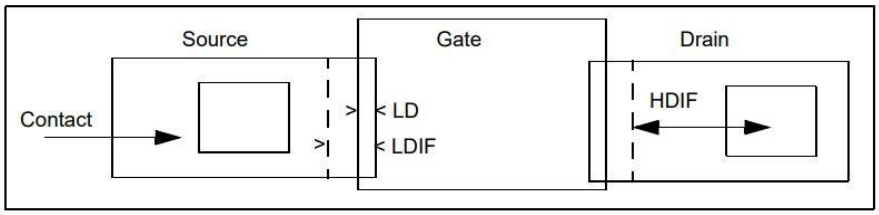


The current in BSIM3v3.3.0 is less than the current in my level 1 model as the saturation happens earlier due to velocity saturation in BSIM3v3.3.0.

3.

```
Circuit: NMOS testbench

Ignoring BSIM parameter ACM
Ignoring BSIM parameter HDIF
Ignoring BSIM parameter XL
Ignoring BSIM parameter XW
```

- **ACM (Area Calculation Method)**: controls the geometry of the source and drain diffusions, and selects the modeling of the bulk-to-source and bulk-to-drain diodes of the MOSFET model. The diode model includes the diffusion resistance, capacitance, and DC currents to the substrate.
    - If ACM=0, the pn bulk junctions of the MOSFET are modeled in the SPICE style.
    - The ACM=1 diode model is the original ASPEC model.
    - The ACM=2 model parameter specifies the improved diode model, which is based on a model similar to the ASPEC MOSFET diode model.
    - The ACM=3 diode model is a further improvement that deals with capacitances of shared sources and drains, and gate edge source/drain-to bulk periphery capacitance.
- **HDIF**: Length of heavily-doped diffusion, from contact to lightly-doped region (ACM=2, 3 only).



  If AD, AS, PD, and PS values are not specified, they are calculated using HDIF.
- **XL**: Length bias accounts for the masking and etching effects.
- **XW**: Width bias accounts for the masking and etching effects.

Geometry Effect

$$W_{eff} = W + XW$$
$$L_{eff} = L + XL$$

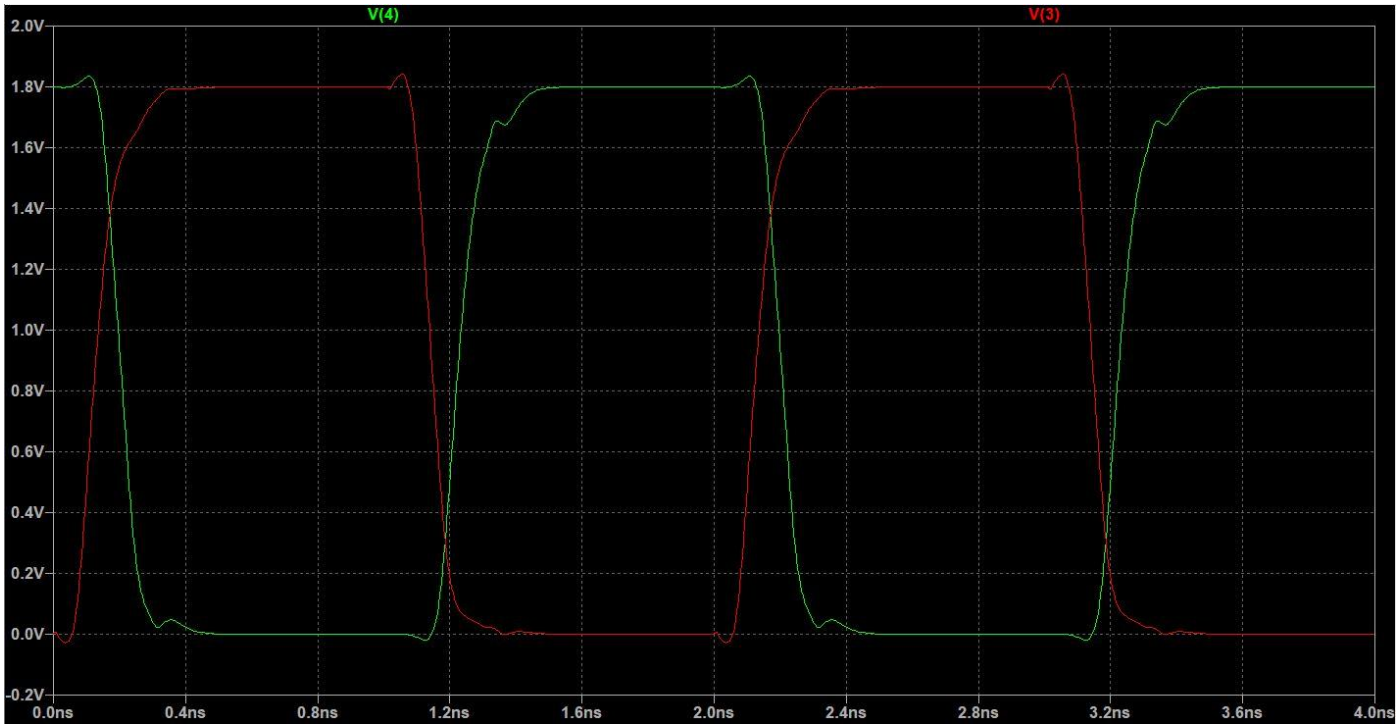
The values of these parameters in the model file:

- ACM = 3 → meaning: properly model MOS diodes of stacked devices (shared source/drains) and source/drain periphery capacitance along the gate edge.
- hdif = 0.32e-6 → the length of the heavily-doped diffusion, from contact to lightly-doped region, is 320 nm.
- XL = 0 → Difference between the physical (on the wafer) and the drawn reference channel length is zero (i.e., this effect is not included in the calculations).
- XW = -1E-8 → Difference between the physical (on the wafer) and the drawn S/D active width is 10 nm.

These parameters are used for calculating the parasitic capacitances, so ignoring them will erroneously result in smaller delay values in the simulation.

4.

```
CMOS inverter transient analysis

.INC ee214b_hspice.sp

** Inverter Subcircuit **
.SUBCKT inverter 1 2 3 PARAMS: MULT=1
* Connections:   | | |
*             input | |
*                 VDD |
*                output
m1 3 1 0 0 nch L=180n W=10u M={MULT}
m2 3 1 2 2 pch L=180n W=20u M={MULT}
.ENDS inverter

** Circuit Description **
* power supply
V_VDD VDD 0 DC 1.8
* input
V_VIN 1 0 PULSE (0 1.8 0 10p 10p 1n 2n)
* inverters FO4
X_I1 1 VDD 2 inverter PARAMS: MULT={4**0} ; shape input
X_I2 2 VDD 3 inverter PARAMS: MULT={4**1} ; shape input
X_I3 3 VDD 4 inverter PARAMS: MULT={4**2} ; circuit under test
X_I4 4 VDD 5 inverter PARAMS: MULT={4**3} ; load output
X_I5 5 VDD 6 inverter PARAMS: MULT={4**4} ; load output

** Analysis Requests **
.TRAN 5p 4n

** Outputs Requests **
.PROBE
.MEAS TRAN FO4_delay TRIG when V(3)=0.9 cross=1 TARG when V(4)=0.9 cross=1
.END
```



5.

```
fo4_delay=7.43586e-011 FROM 1.28066e-010 TO 2.02424e-010
```

(74.3586 ps)/(0.5*180 nm) = 0.82621
for 65nm technology,
FO4 delay = (0.82621)*(0.5*65 nm) = 26.85 ps