Modeling of 90 nm NMOS and PMOS FETs

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***Abstract*— metal-oxide-semiconductor field-effect transistor is an important device in electronics. In this paper, we are modeling the device. This model shows the characteristics of the device and how it operates. Over the years, the device is scaled down to get more functionalities per chip. The scaled-down device deviates from the long-channel MOSFET, so to predict its behavior, we will add some modifications to the long-channel MOSFET model.**

Keywords—Long-channel MOSFET, short-channel MOSFET, Characteristics, Modifications

I. INTRODUCTION

A central device in VLSI circuits is the metal-oxide-semiconductor field-effect transistor (MOSFET). It has a major importance in microprocessors and semiconductor memories. Driven by the desire of increasing the number of components per chip, the MOSFET devices have been scaled down since the beginning of the era of integrated circuits in 1959 [1], but, according to Neamen in [2], to ensure the reliability of the scaled-down devices is the same, we rely on constant-field scaling principle which proposes scaling the device dimensions and voltages while keeping the electric field constant; this corresponds to changes in the other parameters of the device as shown in table I and fig. 1.

TABLE I. PRINCIPLE OF CONSTANT-FI ELD SCALING

Scaled parameters	***Scaling factor (k > 1)***
L, t_{ox}, W, r_j	1/k
N_a, N_d	k
Voltages	1/k

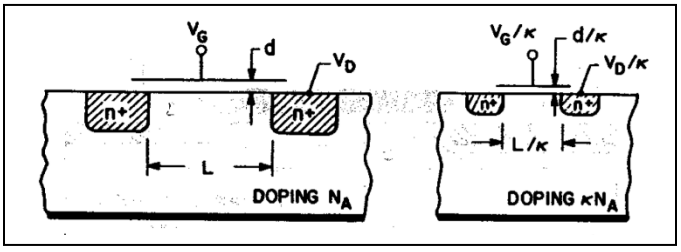

Fig. 1. Scaled-Down Device. Source: Sze [1].

Through this scaling down trend, we have developed a classification based on the length of the channel; we started with the long-channel MOSFET where the length of the channel is much longer than the sum of the source and drain depletion layer widths, then as the scaling down continued, more complicated phenomena started to appear and the operations deviated from our model, but the long-channel MOSFET still serves as the foundation to understand the short-channel MOSFET [1]. In this paper, we are going to study the I-V characteristics of the long-channel MOSFET, then examine the modifications to predict the characteristics of the short-channel MOSFET. The modifications are the following:

- Channel length modulation (CLM):

  Which proposes that the I_d current in the saturation region is not a constant with V_{DS} as the effective length channel is reduced due to the lateral extension of the depletion region at the drain.

- Mobility variation:

  The mobility is not a constant due to the surface scattering affected by the gate voltage and the mobility degradation by approaching the saturation velocity limit [2].

- Velocity saturation:

  By increasing the electric field, the mobility decreases and the carrier velocity saturates. As the length of channel decreases, the device starts to reach the saturation velocity before it reaches the pinch-off voltage [2].

- Threshold voltage (V_{th}) variation:

  When the length of the channel is reduced, the space charge region of the source and drain notably extend into the active channel region causing the threshold voltage variation [2].

All the plots in this paper are generated using MATLAB R2018b.

II. DESIGN PARAMETERS

A. N-channel MOSFET device

The device parameters of the N-channel MOSFET are shown in table II.

TABLE II. DESIGN PARAMETERS

Parameter	***Value (unit)***
T	$300\ K$
n_i	$1.5 * 10^{10}\ cm^{-3}$
L	$90 * 10^{-7} cm$
W	$5L$
t_{ox}	$2 * 10^{-7} cm\ of\ SiO_2 material$

Parameter	Value (unit)
e	$1.6 * 10^{-19}\ C$
Q_{ox}	$313 * 5 * 10^{8} * e\ \ cm^{-2}$
r_j	$60 * 10^{-7} cm$
$junction\ doping$	$2 * 313 * 5 * 10^{17} cm^{-3}$
$Junction\ area$	$4LW\ cm^2 (top - view\ area)$
t_{gate}	$200 * 10^{-7}\ cm$
$Gate\ doping$	$2 * 313 * 5 * 10^{17}\ cm^{-3}$ $of\ n^+\ polysilicon$
N_a	$(3 + 10) * 10^{17} cm^{-3}$
μ_n	$280\ \ cm^2/V - s$

Using these parameters to calculate the threshold voltage as follows:

$$C_{ox} = \frac{(3.9)(8.85*10^{-14})}{t_{ox}}\ F/cm^2,$$

$$\varphi_{fp} = (0.0259) \ln\left(\frac{N_a}{n_i}\right)\ \ V,$$

$$Q_{maxDepletion} = \sqrt{4e * 11.7 * 8.85 * 10^{-14} * N_a \varphi_{fp}}\ \ C/cm^2,$$

$$\varphi_{ms} = -(\frac{1.1}{2} + \varphi_{fp})\ \ \ V,$$

$$\boldsymbol{V_{Threshold} = \frac{Q_{maxDepletion}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}} + \varphi_{ms} + 2\varphi_{fp} = 0.2789\ V,}$$

B. P-channel MOSFET device

The device parameters of the P-channel MOSFET are shown in table III.

TABLE III. DESIGN PARAMETERS

Parameter	Value (unit)
T	$300\ K$
n_i	$1.5 * 10^{10}\ cm^{-3}$
L	$90 * 10^{-7} cm$
W	$10L$
t_{ox}	$2 * 10^{-7} cm\ of\ SiO_2 material$
e	$1.6 * 10^{-19}\ C$
Q_{ox}	$313 * 5 * 10^{8} * e\ \ cm^{-2}$
r_j	$60 * 10^{-7} cm$
$junction\ doping$	$2 * 313 * 5 * 10^{17} cm^{-3}$
$Junction\ area$	$4LW\ cm^2 (top - view\ area)$
t_{gate}	$200 * 10^{-7}\ cm$
$Gate\ doping$	$2 * 313 * 5 * 10^{17}\ cm^{-3}$ $of\ P^+\ polysilicon$
N_d	$(3 + 10) * 10^{17} cm^{-3}$
μ_p	$131\ \ cm^2/V - s$

Using these parameters to calculate the threshold voltage as follows:

$$C_{ox} = \frac{(3.9)(8.85*10^{-14})}{t_{ox}}\ F/cm^2,$$

$$\varphi_{fn} = (0.0259) \ln\left(\frac{N_d}{n_i}\right)\ \ V,$$

$$Q_{maxDepletion} = \sqrt{4e * 11.7 * 8.85 * 10^{-14} * N_d \varphi_{fn}}\ \ C/cm^2,$$

$$\varphi_{ms} = (\frac{1.1}{2} + \varphi_{fn})\ \ \ V,$$

$$\boldsymbol{V_{Threshold} = -\frac{Q_{maxDepletion}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}} + \varphi_{ms} - 2\varphi_{fp} = -0.3079\ V,}$$

III. LONG-CHANNEL MOSFET

We will start by the case where we have a long-channel MOSFET, and, also, we will set a comparison between the plots of P- and N-channel MOSFET.

A. V_{DS} vs I_{DS}

The $V_{DS} vs\ I_{DS}$ curve has two regions:

1. Linear region where

$$I_{DS} = \frac{W\mu_n C_{ox}}{2L}[2(V_{GS} - V_T)V_{DS} - V_{DS}^2]\ ,$$
$$0 \le V_{DS} \le\ V_{GS} - V_T$$

2. Saturation region where

$$I_{DS} = \frac{W\mu_n C_{ox}}{2L}(V_{GS} - V_T)^2\ , \qquad V_{DS} >\ V_{GS} - V_T$$

We plotted for $V_{GS} = 1\ and\ 1.3$ having $V_{DS}(sat.) = 0.72,\ 1.02$, respectively. We find that as V_{GS} increases, I_{DS} & $V_{DS}(sat.)$, also, increase as expected.

For N-channel MOSFET device, the curve behaves as shown in fig. 2.

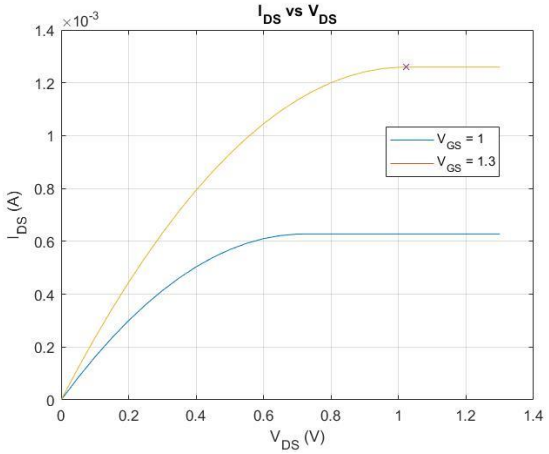

Fig. 2. $I_{DS}\ vs\ V_{DS}$.

We repeated the same analysis for P-channel MOSFET device, so we get plot shown in fig. 3.

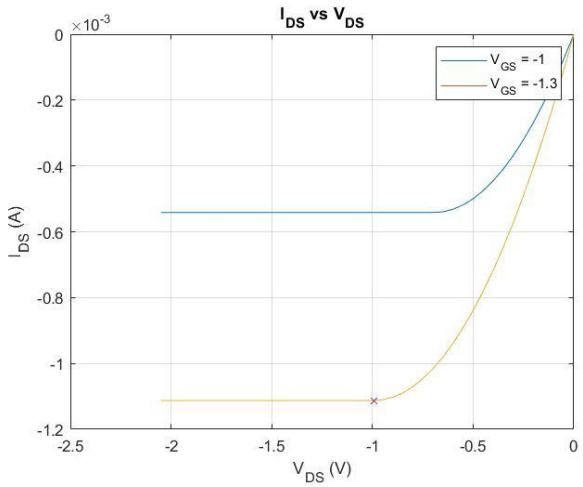

Fig. 3. I_{DS} *vs* V_{DS}.

B. V_{GS} *vs* I_{DS}

For N-channel MOSFET device,

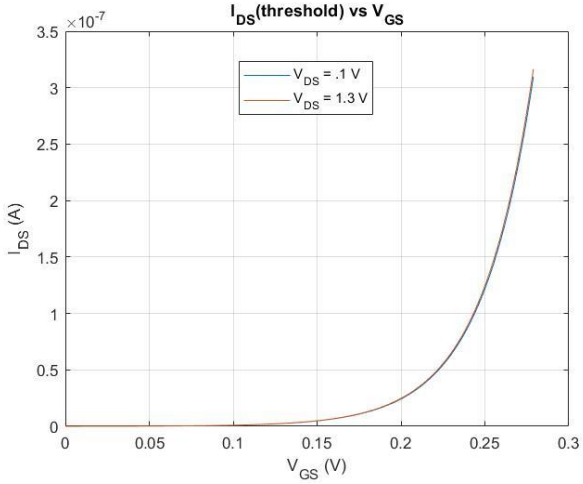

Fig. 4. $I_{DS}(subthreshold)$ *vs* V_{GS}.

The V_{GS}*vs* I_{DS} curve has three regions:

1. Subthreshold region where

$$I_{DS}(sub) = \mu_n C_{ox} \frac{W}{L}(m-1)\left(\frac{kT}{e}\right)^2 e^{\frac{V_{GS}-V_T}{m\frac{kT}{e}}}\left(1 - e^{-\frac{V_{DS}}{\frac{kT}{e}}}\right),$$

$0 \le V_{GS} < V_T$

and the curve of this region is plotted separately in fig. 4.

2. Saturation region where

$$I_{DS} = \frac{W\mu_n C_{ox}}{2L}(V_{GS} - V_T)^2\,, \qquad V_T \le V_{GS} < V_{DS} + V_T$$

3. linear region where

$$I_{DS} = \frac{W\mu_n C_{ox}}{2L}[2(V_{GS} - V_T)V_{DS} - V_{DS}^2]\,,\ V_{DS} + V_T \le V_{GS}$$

There sequence in the plot is the following: subthreshold region, saturation region then linear region. We note that as V_{DS} increases, I_{DS}, also, increases for the same V_{GS}. The plot of all the regions combined is shown in fig. 5.

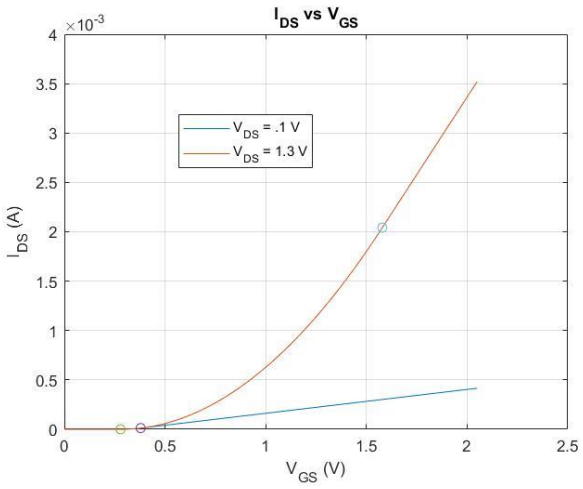

Fig. 5. I_{DS} *vs* V_{GS}.

For P-channel MOSFET device, we repeated the same analysis of the N-channel MOSFET, so we got fig. 6 & 7.

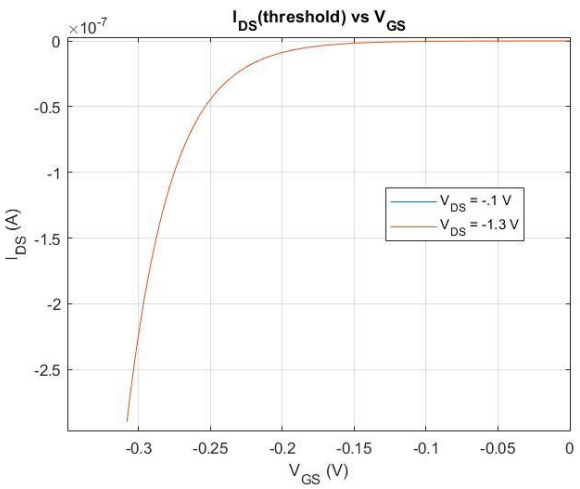

Fig. 6. I_{DS} *vs* V_{GS}.

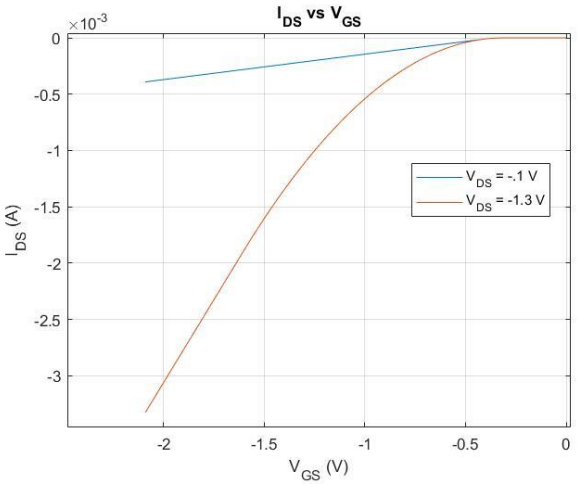

Fig. 7. I_{DS} *vs* V_{GS}.

C. V_{GS} vs G_m

The plot is divided into two regions:

1. Saturation region

$$G_m = \frac{W\mu_n C_{ox}}{L}(V_{GS} - V_T), \qquad V_T \le V_{GS} < V_{DS} + V_T$$

2. Linear region

$$G_m = \frac{W\mu_n C_{ox}}{L} V_{DS}, \quad V_{DS} + V_T \le V_{GS}$$

For N-channel MOSFET device, the curve behaves as shown in fig. 8.

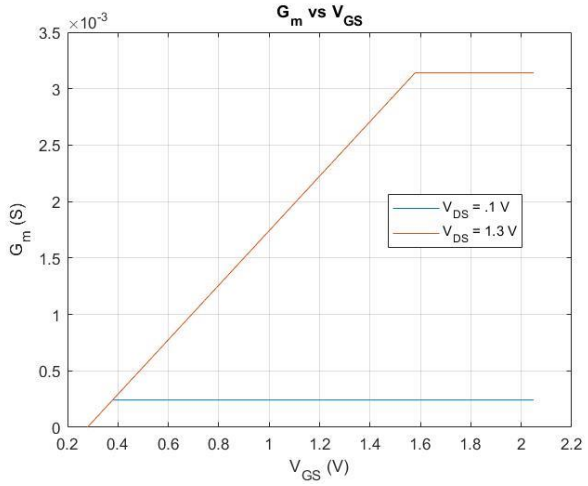

Fig. 8. G_m *vs* V_{GS}.

For P-channel MOSFET device, we repeated the same analysis of the N-channel MOSFET, so we got fig. 9.

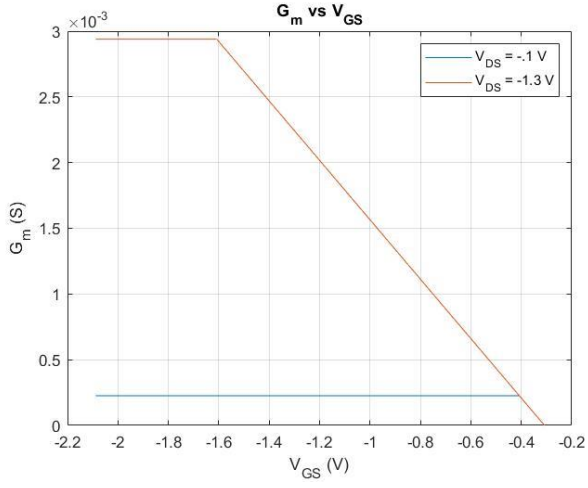

Fig. 9. G_m *vs* V_{GS}.

D. V_{GS} vs g_d

The plot is divided into two regions:

1. Saturation region

$$g_d = 0, \qquad V_T \le V_{GS} < V_{DS} + V_T$$

2. Linear region

$$g_d = \frac{W\mu_n C_{ox}}{L}(V_{GS} - V_T - V_{DS}), \quad V_{DS} + V_T \le V_{GS}$$

For N-channel MOSFET device, the curve behaves as shown in fig. 10.

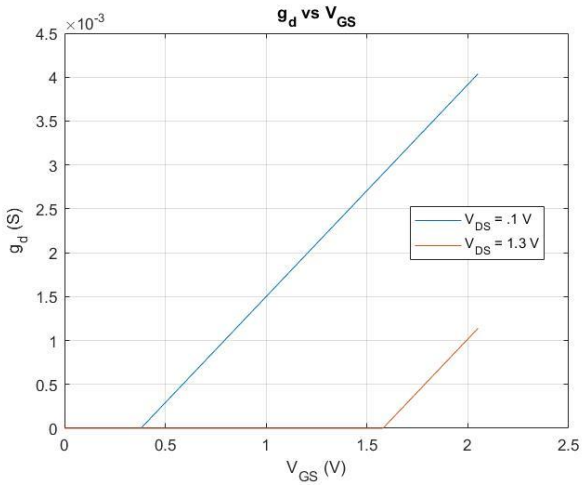

Fig. 10. g_d *vs* V_{GS}.

For P-channel MOSFET device, we repeated the same analysis of the N-channel MOSFET, so we got fig. 11.

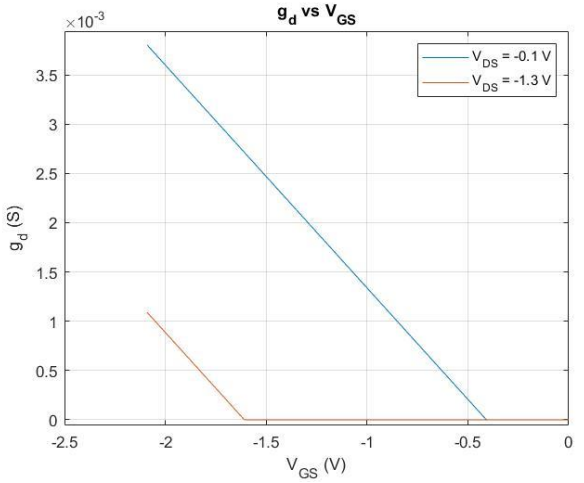

Fig. 11. g_d *vs* V_{GS}.

IV. SHORT-CHANNEL MOSFET

After examining the characteristics of the long-channel MOSFET, we will add the modifications discussed in the introduction to predict the behavior of N-short-channel MOSFET.

A. Channel length modulation (CLM)

To add the CLM, we have

$$\Delta L = \sqrt{\frac{2\epsilon_s}{eN_a}}\left[\sqrt{\varphi_{fp} + V_{DS}} - \sqrt{\varphi_{fp} + V_{DS}(sat.)}\right]$$

Then $I_{DS}(sat.)' = \left(\frac{L}{L-\Delta L}\right) I_{DS}(sat.)$, so we get the following plot:

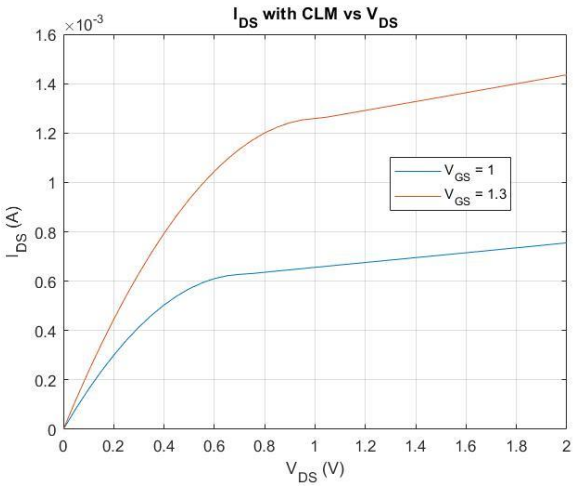

Fig. 12. I_{DS} *vs* V_{DS}.

We see from the plot that the current in the saturation region is not a constant, and it is increasing with V_{DS} due to the lateral extension of the depletion region at the drain.

B. Velocity saturation

In this case, we are dealing with a constant mobility in a certain region. After this region, the carriers reach the saturation velocity. As the behavior of the dotted line in fig. 13 shows from [3].

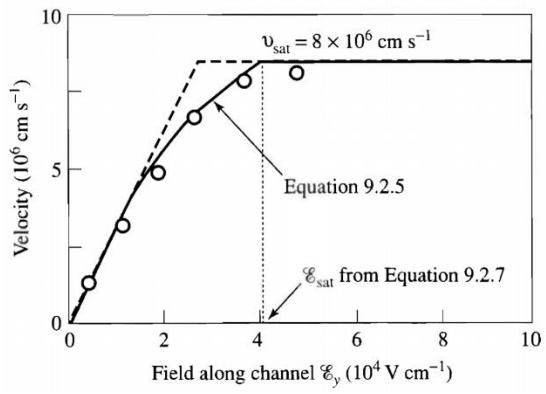

Fig. 13. *horizontal electric field vs velocity*.

The plot, as shown in fig. 14, is divided into two regions:
1. linear region where

$$I_{DS}(with\ velocity\ sat.) = \frac{I_{DS}(without\ velocity\ sat.)}{1+\frac{V_{DS}}{LE_c}}$$

Where $E_c = \frac{v_{sat}}{\mu}$.

2. the saturation region:

$I_{DS}(with\ velocity\ sat.)$ has an additional dependence on V_{DS} than the common $I_{DS}(without\ velocity\ sat.)$, so we need to start the derivation of $I_{DS}(with\ velocity\ sat.)$ in the saturation region from the beginning by taking the derivative of $I_{DS}(with\ velocity\ sat.)$ in the linear region, equating the result with zero, solving for $V_{DS}(sat.)$, then substituting this value in the equation of $I_{DS}(with\ velocity\ sat.)$ in the linear region to get $I_{DS}(sat.)$ as shown in the MATLAB code.

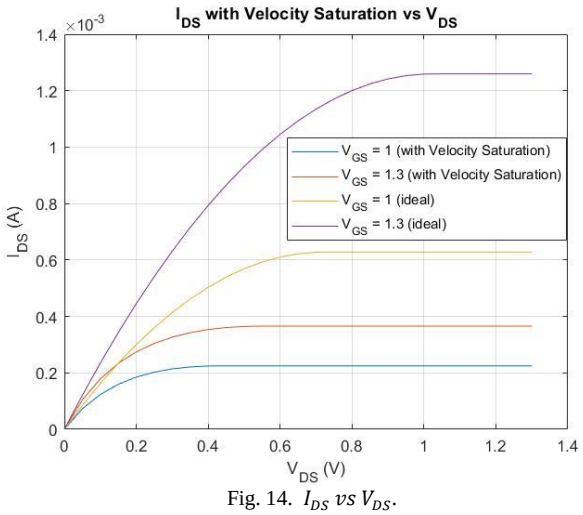

Fig. 14. I_{DS} *vs* V_{DS}.

Also noted in the plot that the velocity saturation modification results in a lower I_{DS} than the long-channel MOSFET current.

C. Mobility degradation

Here, we are just considering the effect of the mobility degradation and neglecting the velocity saturation effect as we are assuming that the carriers' velocity has no limit and modeling how the mobility value changes.

First, we add the effect of the surface scattering on the mobility as follows:

$$E_{eff} = \frac{1}{\epsilon_s}(|Q'_{SD}(max)| + \frac{1}{2}Q'_n)$$

Where $Q'_n = C_{ox}(V_{GS} - V_{th})$
The effective mobility is represented by

$$\mu_{eff} = \mu_0 \left(\frac{E_{eff}}{E_0}\right)^{-1/3}$$

Where μ_0 and E_0 are curve-fitting constants, so we use fig. 15 from [2] to determine our constants using one point (10^5,700) extracted using GetData Graph Digitizer sofware where we get the following:

$$\mu_{eff} = \left(\frac{700}{10^{-\frac{5}{3}}}\right) E_{eff}^{-\frac{1}{3}}$$

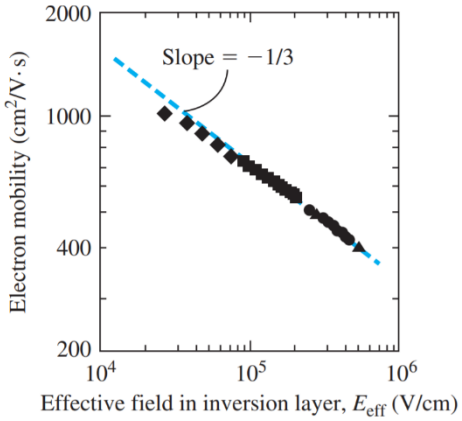

Fig. 15. *vertical electric field vs mobility*.

Secondly, we add the effect of the horizontal electric field on the mobility as follows:

$$\mu = \frac{\mu_{eff}}{\left[1 + \left(\frac{\mu_{eff} E_{horizontal}}{v_{sat}}\right)^2\right]^{1/2}}$$

Where $E_{horizontal} = \frac{V_{DS}}{L}$ and $v_{sat} = 10^7\ cm/s$

Then we plotted $I_{DS} vs\ V_{DS}$ which is divided into two regions:

1. Linear region where

$$I_{DS} = \frac{W \mu_n C_{ox}}{2L} [2(V_{GS} - V_T)V_{DS} - V_{DS}^2]$$

2. saturation region:

Due to the dependence of the mobility on V_{DS}, we followed the same treatment of the velocity saturation case.

As shown in fig. 16, we find that the mobility degradation results in a lower I_{DS} than the long-channel MOSFET current.

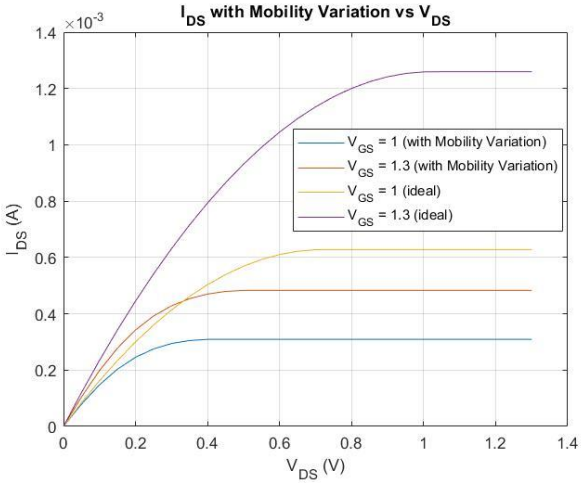

Fig. 16. I_{DS} *vs* V_{DS}.

D. Threshold voltage (V_{th}) variation

a) V_{th} dependence on L_{gate}:

As the MOSFET length decreases, the threshold voltage, also, decreases because larger fraction of the space charge regions of the source and drain is occupied in the channel region. The effect of this phenomana goes as follows:

$$\Delta V_{th} = -\frac{eN_a x_{dT}}{C_{ox}} [\frac{r_j}{L}(\sqrt{1 + \frac{2x_{dT}}{r_j}} - 1)]$$

$V_{th}(short\ channel) = V_{th}(long\ channel) + \Delta V_{th}$

Then by plotting the $V_{DS} vs\ I_{DS}$ curve in the linear region where

$$I_{DS} = \frac{W \mu_n C_{ox}}{2L} [2(V_{GS} - V_T)V_{DS} - V_{DS}^2],$$
$$0 \le V_{DS} \le V_{GS} - V_T$$

And in the saturation region where

$$I_{DS} = \frac{W \mu_n C_{ox}}{2L} (V_{GS} - V_T)^2, \qquad V_{DS} > V_{GS} - V_T$$

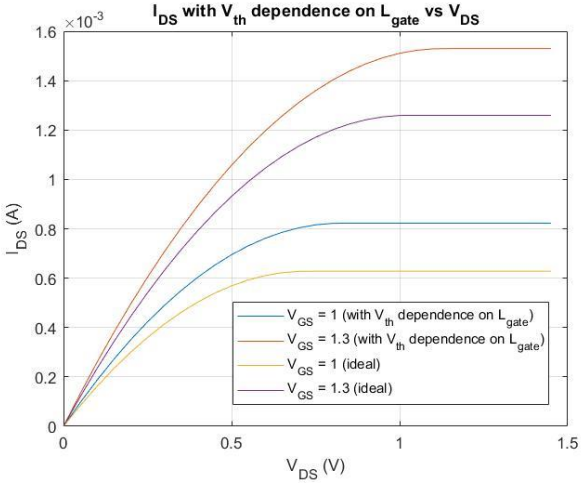

Fig. 17. I_{DS} *vs* V_{DS}.

From fig. 17, we see that the modified current of the short channel is higher than the long channel MOSFET corresponding to decreasing the value of the threshold voltage.

b) V_{th} dependence on V_{DS}:

Due to the charge of the junctions shared in the channel region as explained before, we find that increasing V_{DS} results in reducing the threshold voltage. This reduction could be modeled as follows:

$$\Delta V_{th} = [2(V_{bi} - 2\varphi_{fp}) + V_{DS}](e^{-\frac{L}{2l}} + e^{-\frac{L}{l}})$$

Where $V_{bi} = \frac{kT}{e} \ln\left(\frac{N_a N_d}{n_i^2}\right)$,

$l(\text{Device natural length}) = \sqrt{\frac{x_{dT} t_{ox} \epsilon_{si}}{\epsilon_{ox}}}$. [4]

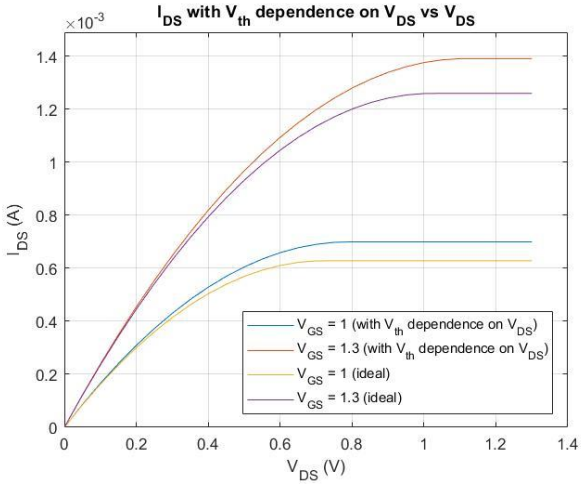

Fig. 18. I_{DS} *vs* V_{DS}.

Then after modifying the I_{DS} relation with the new V_T similar to the previous treatment of the L_{gate} dependence, we

find that the modified current is higher than the long channel MOSFET as shown fig. 18.

V. SUMMAERY

In this paper, we developed an analytical model for the long-channel MOSFET and tested its I-V characteristics, explained the scaling down process and the phenomena appearing as we scaling down, then we added modifications to our model to predict the behavior of the short-channel MOSFET.

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