Communication Theory and Systems
NANENG 461
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Quadrature Phase-Shift Keying (QPSK) Project Report

Prepared by:
Shehab Bahaa | 201700313
Ahmed Hashem | 201700988
Mohamed Roshdy | 201701098

Supervised by:
Dr. Ahmed Eltrass

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1. Introduction

Quadratic phase shift keying (QPSK) Modulation technique transmits two bits per symbol. A QPSK symbol represents 00, 01, 10, or 11, Fig.1. The Carrier varies in terms of phase, and it is dependent on four possible phase shifts. Basically we are working with 0, 90, 180, 270 in degrees. The waveform of QPSK is as follows, which shows the modulated result for different instances of binary inputs [5]:

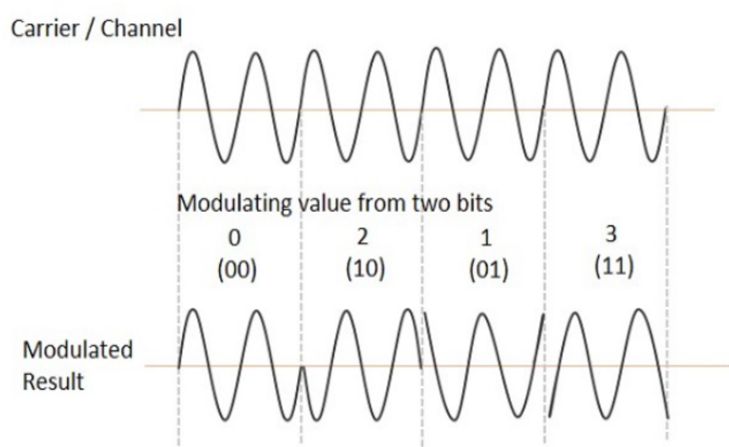

Fig.1

2. Application

Due to its performance on bandwidth efficiency and bit rate error, it is used in wireless communication and satellite transmission. QPSK allows the signal to carry twice as much as the ordinary BPSK Technique in addition to video conferencing and cable modems.

3. QPSK Modulator “Proposed designs”

In fig.2 & fig.3, we can find the QPSK Modulator circuit block which consists of:

- Bit-splitter we used serial to parallel converter then we obtained the phase shifts from 2 possible ways: the first was by RC configurations, and was replaced by phase shifted signals from the function generator due to noise added to the signal.

- 4 connected diodes used to obtain multiplication between carrier signal and Bits.
- Op-amp as a summing amplifier

This procedure had a lot of difficulties, and the output was not as expected so we started to debug each output from each component. Finally, we could not figure out where the error came from, so we changed our methodology [1].

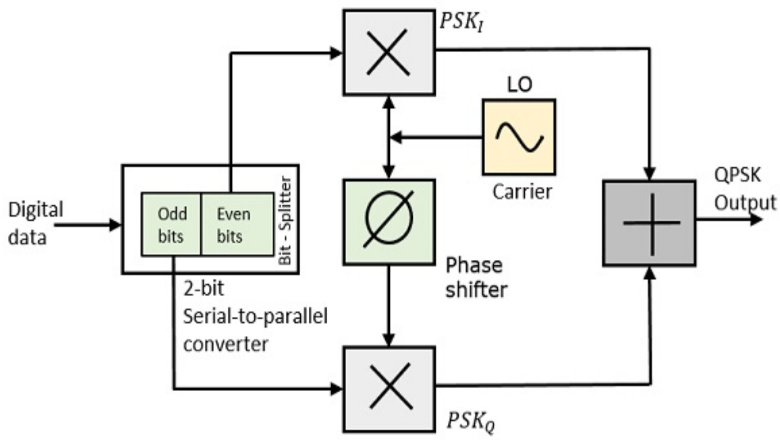

Fig.2

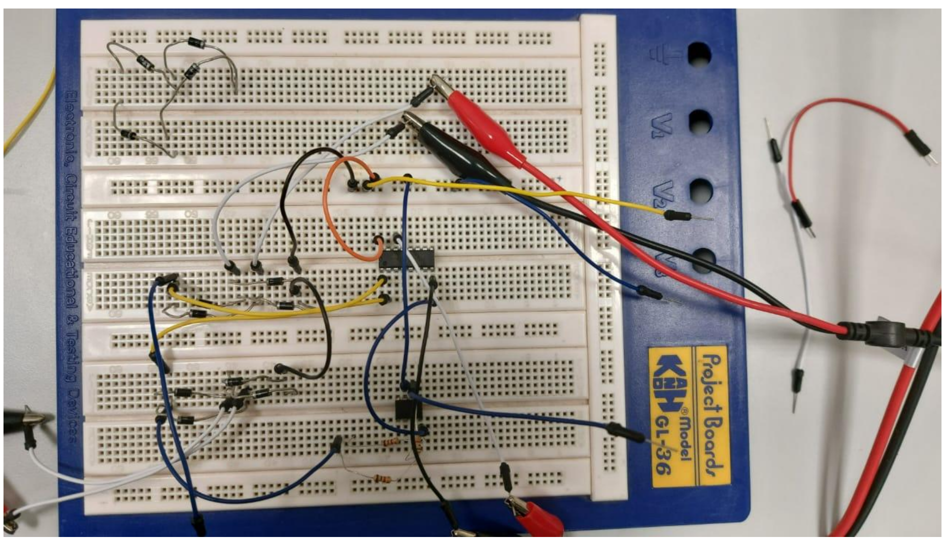

Fig.3

- Another Proposed Designs
  - As before we used a function generator again but now we stored shifted signals as input for 4-to-1 analog mux with the bits

00,01,11,10 as the select signal.

- This procedure was fine at the beginning, the output of the mux was as expected but the peak to peak was somewhat less than the generated signal. Also, we had a major problem with the received signal in the demodulation part. Outputs from mux for a pattern of 1's and 0's somewhat differ and may alter the required pattern. Finally we headed to Hardware Description Language (HDL) to implement the required modulation on SPARTAN 6 and we tried to make it as simple as possible, a synchronous shifted register module was created to serve as Serial in Parallel out Converted which has an input 2-bit Data_in and two outputs I,Q, then instantiate this module in the top module which implement 2 BPSK and its output is the QPSK, the major problem we faced in the approach was the implementation of the carrier signal, since sin() is not synthesizable, and no simple implementation was found for this problem, even we tried to save the values of each shifted sin() signal in an external file generated from matlab for example and then assigned it to a vector in the top module, unfortunately the result of this approach was distorted and far from the sin() signals that were sent, we believe that smaller sampling frequency needs to be generated which significantly affects simulation time and the complexity of the the file.

4. QPSK Demodulator

- In the following diagram Fig.4, we can find the QPSK Modulator circuit block which consists of:
- two multipliers (each 4 Diodes)
- A 2-bit serial to parallel converter (PISO)
- Two band pass filters.
- Two integrator circuits.

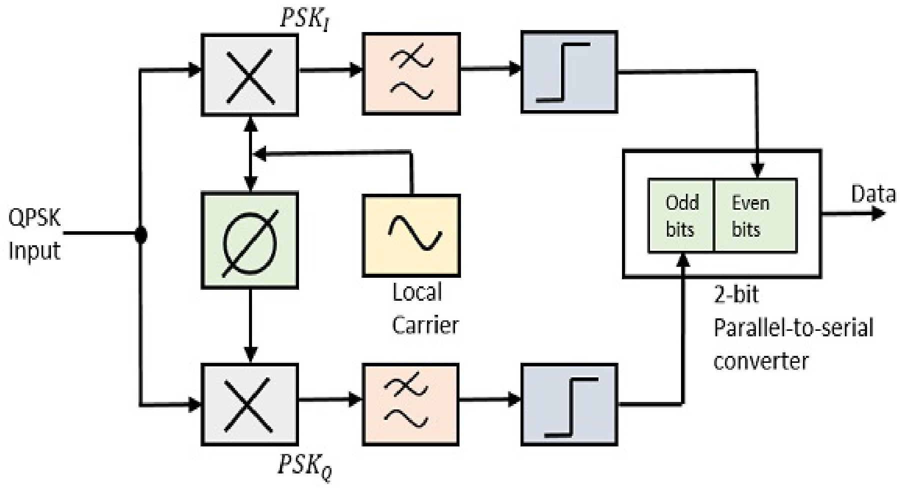

Fig.4

5. MATLAB

Part (1): modeling different channels and analyzing them

- The bitstream enters a quadrature phase shift keying modulator which has a constellation diagram as shown in figure (5).
- Regarding the channel, three types of channels were modeled:
  - First channel has additive white gaussian noise (AWGN) only. The constellation diagram of this channel (at SNR=10) and BER vs SNR curve are shown in figure (6) and (9), respectively.
  - Second channel is a Rayleigh channel with no noise. The constellation diagram of this channel (at SNR=10) and BER vs SNR curve are shown in figure (7) and (10), respectively.
  - Third channel is a Rayleigh channel with additive white gaussian noise (AWGN). The constellation diagram of this channel (at SNR=10) and BER vs SNR curve are shown in figure (8) and (11), respectively.
- Finally, a comparison between BER vs SNR curves of the three channels was done as shown in figure (12).

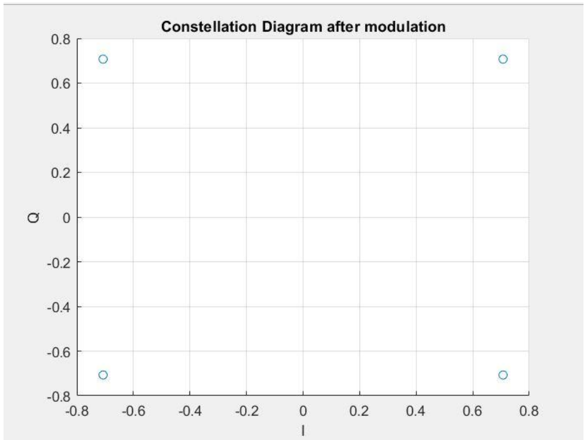

Figure (5)

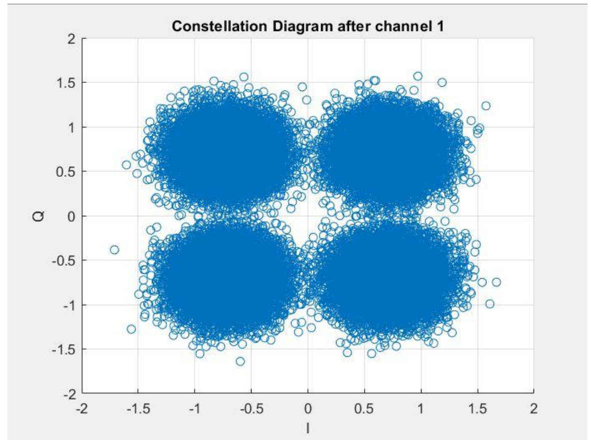

Figure (6)

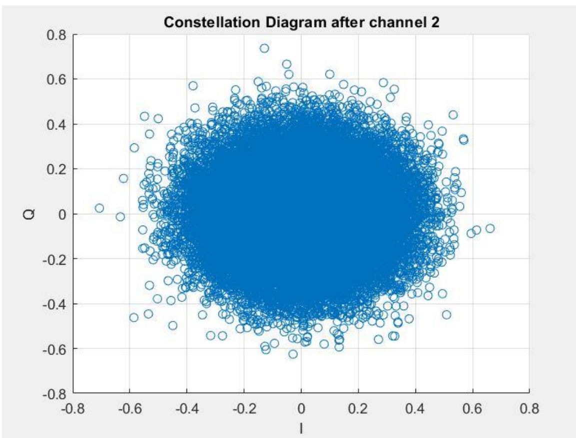

Figure (7)

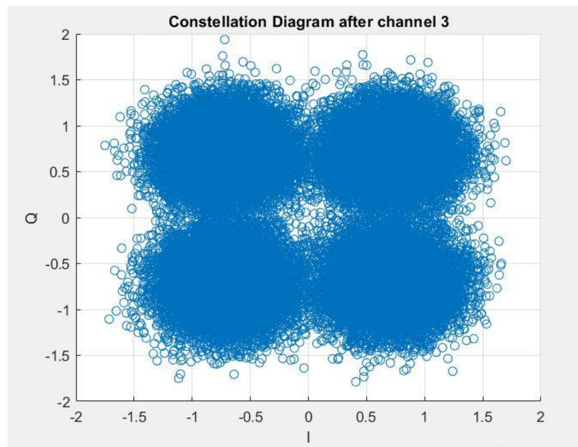

Figure (8)

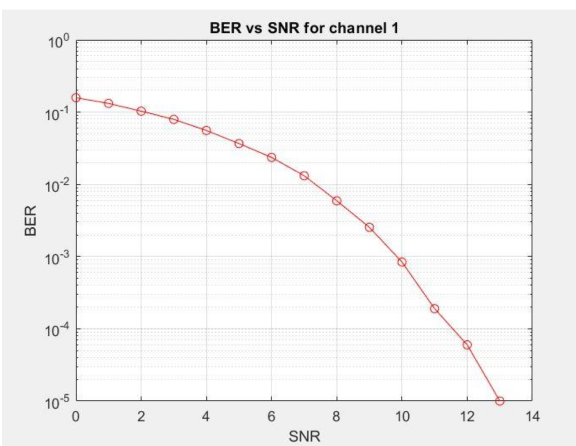

Figure (9)

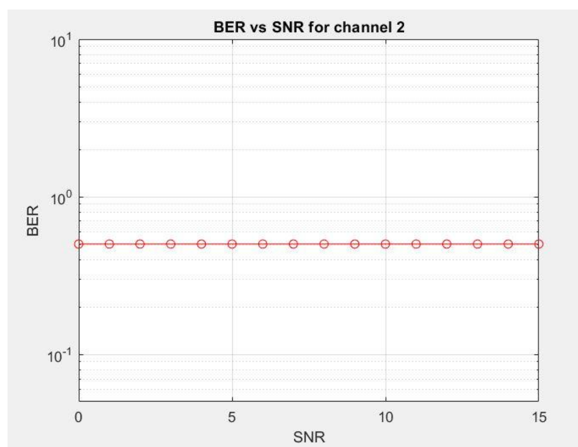

Figure (10)

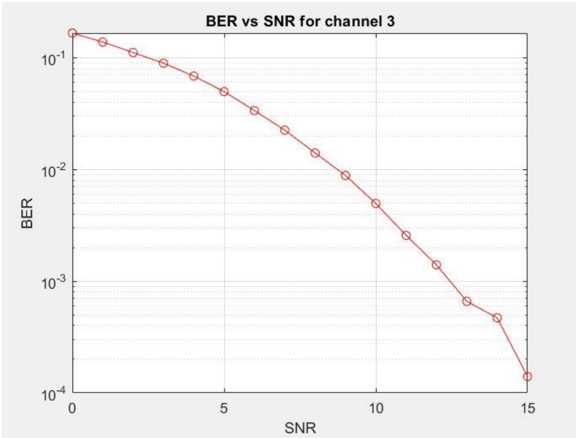

Figure (11)

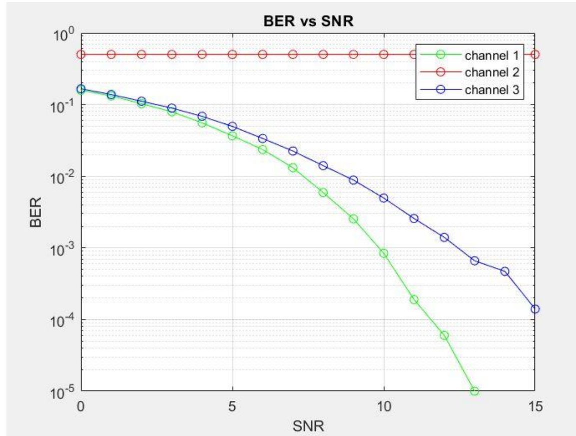

Figure (12)

Part (2): Sending and receiving an image

- Firstly, an image is used to generate a bitstream to be the input into the modulator.
- Then, the modulated data entered the three channels modeled in the previous part.
- Finally, the data was demodulated, and the received images corresponding to the different channels are shown in figure (14), (15), and (16) for channel 1,2, and 3, respectively.

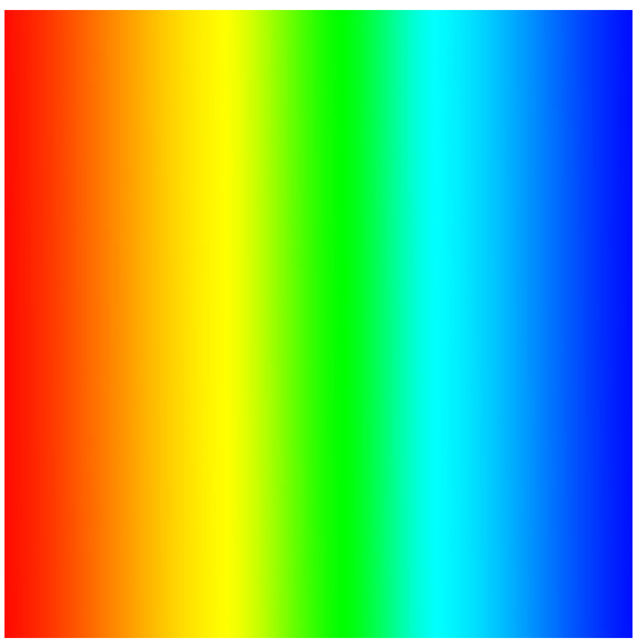

Figure (13): Sent Image

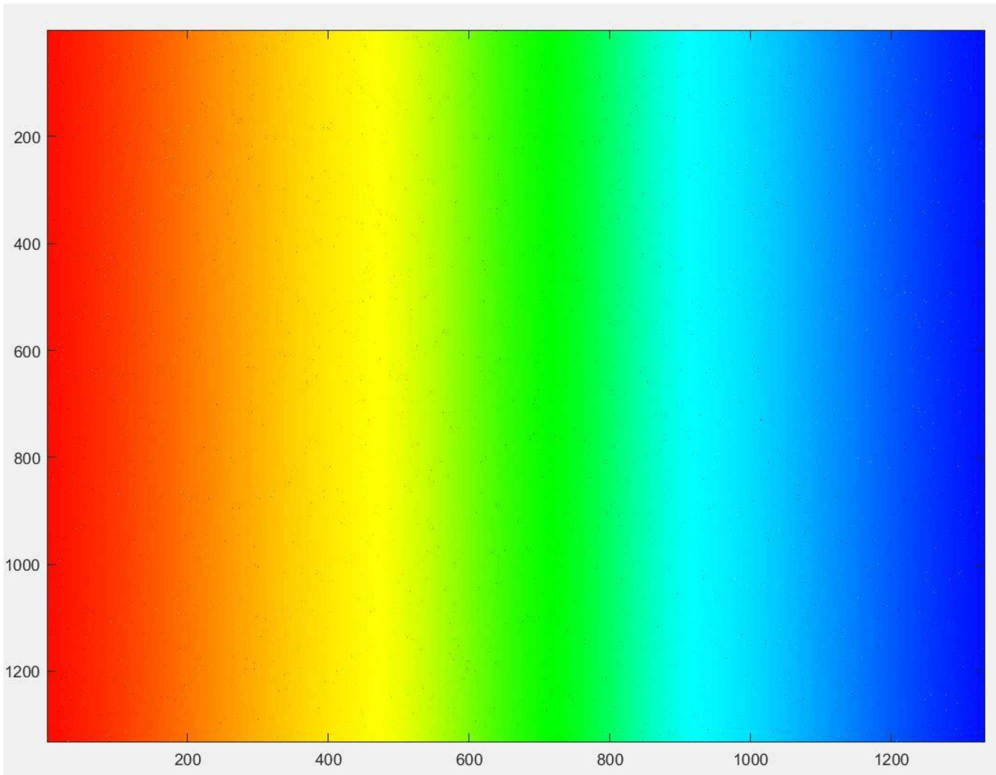

Figure (14): channel 1 results

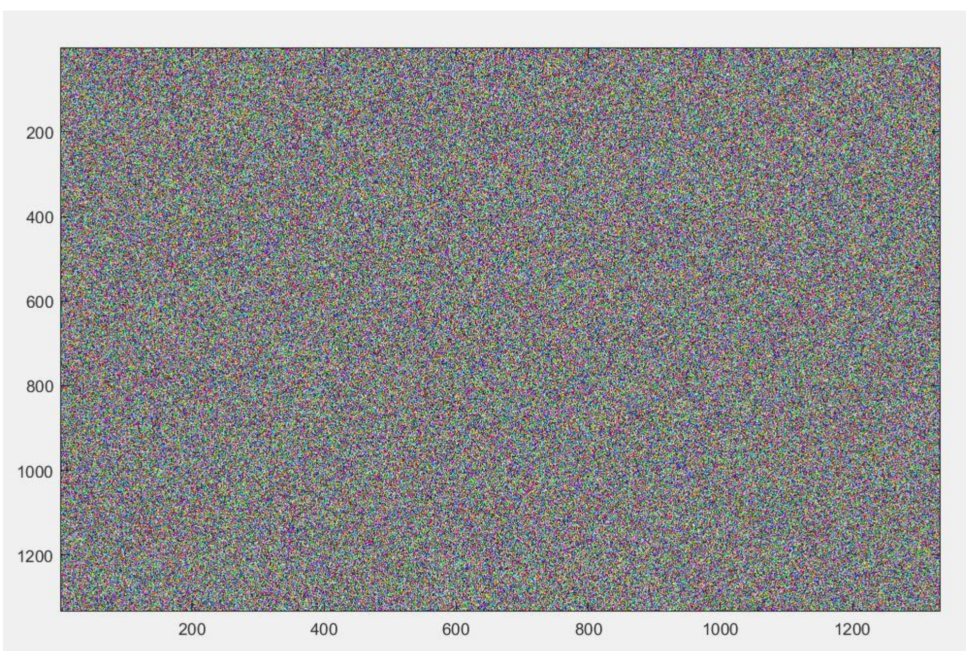

Figure (15): channel 2 results

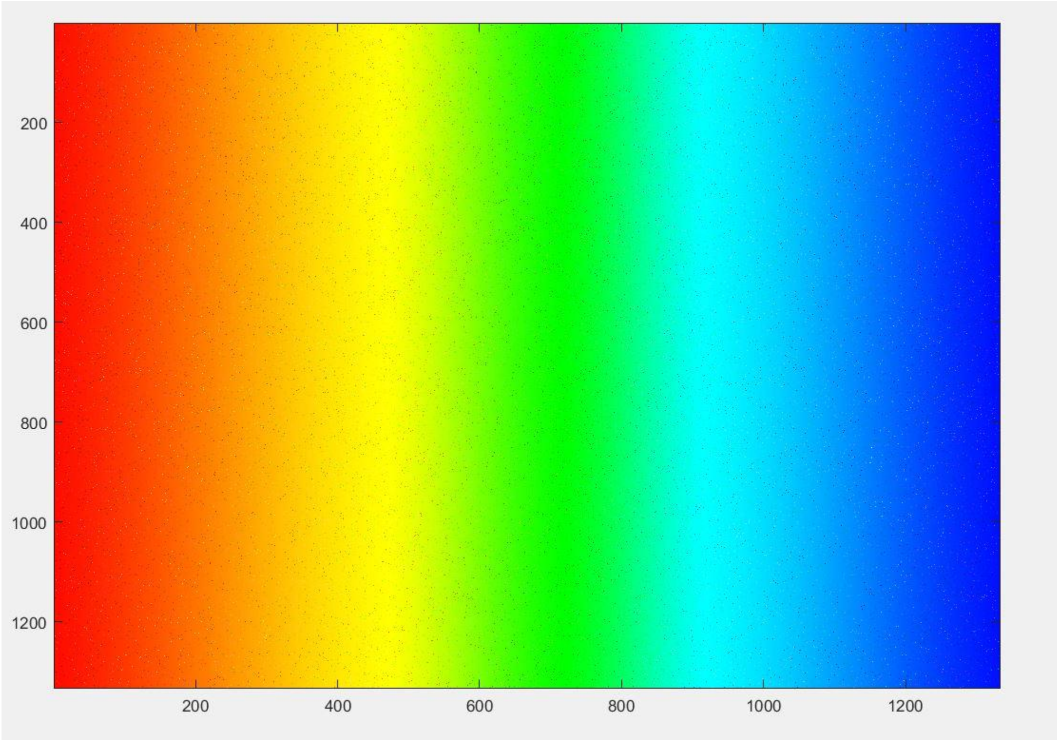

Figure (16): channel 3 results

6. Conclusion

In this project, a quadrature phase shift keying was implemented. The first part was a hardware implementation for the communication system using discrete electronic components. The second part was a matlab simulation. In this simulation, different types of channels were modeled and analysed, then an image was sent and received through these channels.

References

[1] "Quadrature Phase Shift Keying," *Tutorialspoint*. [Online]. Available: https://www.tutorialspoint.com/digital_communication/digital_communication_quadrature_phase_shift_keying.htm. [Accessed: 17-Jun-2021].