Class Test 3 Date: July 27, 2022

BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY

Department of Computer Science and Engineering

L-3/T-1 $\,$ CSE 305: Computer Architecture

Time: 20 minutes Marks: 20

Student Name:	Student No:

1. A full datapath with a control unit is given in the figure below. Highlight the functional components that will be active for the sw \$t1, 100(\$t2) instruction. Also, mention which control bits will be set.

0 M u x Add Add ALU result 1 Shift RegDst left 2 Branch MemRead Instruction [31-26] MemtoReg ALUOp MemWrite **ALUSrc** RegWrite Instruction [25-21] Read Read PC register 1 Read address data 1 Instruction [20-16] Read Zero Instruction [31–0] register 2 0 M u x 1 ALU _{ALU} result Address Read data Read data 2 (0 M u x 1) 1 M u x 0 Write Instruction Instruction [15-11] register memory Write data Registers Data Write Data data memory 16 32 Instruction [15-0] Sign-ALU extend control Instruction [5-0]

(10)

2. You want to design a control unit for a set of instructions consisting lw, sw, add, sub, AND, XOR. What is the minimum number of bits of opcodes needed? What is the minimum number of bits that will be needed to be fed from the main control unit to the ALU control unit? Draw the combinational circuit for the ALU control unit. Your implementation must be as compact and optimized as possible. [Hint: It does not necessarily have to adhere to the standard MIPS convention.]