Week 4 Task – CMOS Circuit Design (sky130-style)

Why This Task Matters (revised)

This task deepens your understanding of how transistor-level circuit properties (device physics, sizing, variation) drive the timing behavior that STA analyzes. By working through CMOS design and SPICE simulations (as in the sky130 workshop), you will see the "real" side of what STA approximates. This strengthens your intuition about slack, delay, noise margins, and variation impacts.

Download workshop Collaterals from below link
https://github.com/kunalg123/sky130CircuitDesignWorkshop/

Workshop will be enabled on VSDIAT platform

Task Components (adapted from sky130CircuitDesignWorkshop) (GitHub)

You will carry out a sequence of CMOS design and SPICE simulation activities, mirroring the flow in the sky130 workshop. The components are:

1. **MOSFET Behavior & Id vs. Vds Characteristics**
    - Simulate an NMOS device, sweeping (Vds) for different (Vgs), to observe linear and saturation regions
    - Plot (Id) vs. (Vds) curves
2. **Threshold Voltage Extraction & Velocity Saturation**
    - Sweep (Vgs) vs. (Id) and extract threshold (Vt) (e.g. by linear extrapolation)
    - Observe effects of velocity saturation in short-channel regime
3. **CMOS Inverter: Voltage Transfer Characteristic (VTC)**
    - Build a CMOS inverter (PMOS + NMOS)
    - Sweep input, plot (V{out}) vs. (V{in})
    - Identify the switching threshold (Vm) (point where (V{in} = V{out}))
4. **Transient Behavior: Rise / Fall Delays**
    - Apply a pulse input to the inverter
    - Extract rise and fall propagation delays (times at (Vdd}/2) crossing)

5. **Noise Margin / Robustness Analysis**
    - From the VTC plot, determine (V{IL}, V{IH}, V{OL}, V{OH})
    - Compute (NML = V{IL} - V{OL}) and (NMH = V{OH} - V{IH})
6. **Power-Supply and Device Variation Studies**
    - Vary supply voltage (Vdd) and re-plot VTCs to observe how switching threshold shifts
    - Modify transistor sizing (e.g. W/L of PMOS or NMOS) to simulate device variation, and observe effects on VTC, noise margins, delays

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Deliverables (document following style of sky130 repo) (GitHub)

You should document your work in a report (markdown or notebook) that mirrors the structure seen in the sky130 workshop repo. The deliverables include:

- **Introduction / Background**
  Briefly describe purpose of each experiment (e.g. why Id vs Vds, why VTC, etc.)
- **SPICE Netlists / Code**
  Include the full SPICE netlist(s) used for each component (Id/Vds, VTC, transient, variation).
- **Plots & Figures**
  For each experiment:
    - Graphs (Id vs Vds, Id vs Vgs, VTC, transient waveforms, VTC under variation)
    - Annotated (mark threshold point, switching point, points for noise margin, etc.)
- **Tabulated Results**
  Summary table(s) listing:
    - Extracted threshold voltage(s)
    - Rise / fall propagation delays
    - Noise margins (NM_L, NM_H)
    - Effect of variation (changes in switching point, noise margins, delay)

- **Observations / Analysis**
  For each experiment, a short discussion:
    - What you see (e.g. saturation onset, threshold shift)
    - Why it happens (device physics)
    - How this ties back to STA concepts (e.g. delay models, variation, margin)
- **Conclusions**
  Higher-level reflections:
    - How transistor-level behavior constrains timing in real circuits
    - How variation or supply changes can affect STA margins & critical paths
- **References / Citations**
  If you referenced any literature or models (e.g. from sky130 models), list them