Week 3 Task - Post-Synthesis GLS & STA Fundamentals

Objective

To understand and perform **Gate-Level Simulation (GLS)** after synthesis, validate functionality, and get introduced to **Static Timing Analysis (STA)** concepts with practical experiments using OpenSTA.

Part 1 – Post-Synthesis GLS

- Refer to this example for **GLS flow and methodology**:
  GLS Reference – VSD_HDP
- https://github.com/Ananya-KM/VSD_HDP/blob/main/Day%206.md

- Steps:
  1. Perform synthesis of the BabySoC design.
  2. Run **Gate-Level Simulation (GLS)** using the synthesized netlist.
  3. Compare **GLS output** with **functional simulation output** (Week 2 task). The results should match.
- **Deliverables**:
  - Synthesis logs
  - GLS waveform screenshots
  - Short note confirming GLS = Functional outputs
