CSE 345: Digital Logic Design

Section: 1, Spring 2020

Project

Submitted by:

Group: 9

Group Members:

AMIT ROY	2017-3-60-021
SIRAJUM MARIA MUNA	2017-3-60-020
SHEKHOR CHANDRA SAHA	2017-3-60-025
MD NABID HOSSAIN	2017-3-60-059

Submitted to:

Musharrat Khan

Senior Lecturer, Dept. of CSE

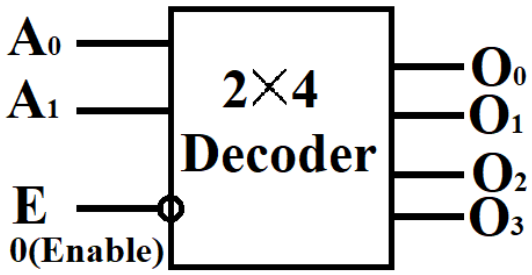
East West University

Date of Submission:09-05-2020

Question 1:

Draw the block diagram, truth table, equation and logic diagram of a 2-to-4 lines decoder with active- LOW outputs and active-LOW enable input.

Block diagram:



Block Diagram

Truth table:

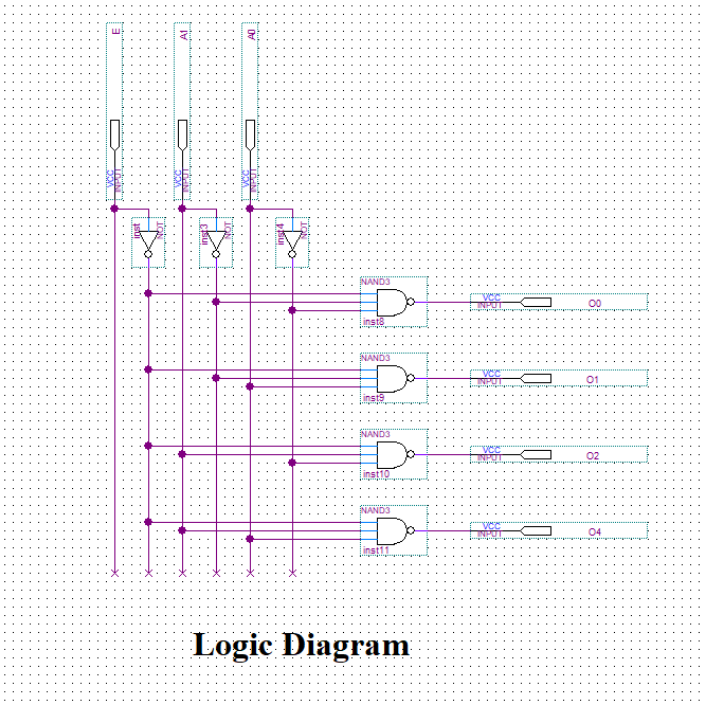
Inputs			Outputs			
E	A_0	A_1	O_3	O_2	O_1	O_0
0	0	0	1	1	1	0
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	0	1	1	1
1	0	0	1	1	1	1
1	0	1	1	1	1	1
1	1	0	1	1	1	1
1	1	1	1	1	1	1

Equation:

O_0=E+A_1+A_0 = (E′A_1′A_0′)′
O_1=E+A_1+A_0 ′= (E′A_1′A_0)′

O_2=E+A_1 ′+A_0 = (E′A_1A_0′)′
O_3=E+A_1 ′+A_0 ′= (E′A_1A_0)′

Logic diagram:

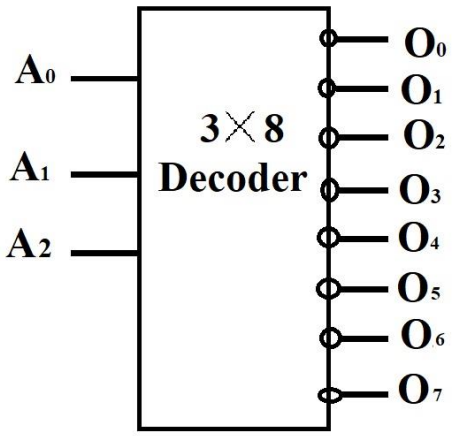


Logic Diagram

Question 2:

Draw the block diagram, truth table, equation and logic diagram of a 3-to-8-lines decoder with active-LOW outputs.

Block diagram:



Block Diagram

Truth table:

Inputs			outputs							
A_2	A_1	A_0	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0
0	0	0	1	1	1	1	1	1	1	0
0	0	1	1	1	1	1	1	1	0	1
0	1	0	1	1	1	1	1	0	1	1
0	1	1	1	1	1	1	0	1	1	1
1	0	0	1	1	1	0	1	1	1	1
1	0	1	1	1	0	1	1	1	1	1
1	1	0	1	0	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1

Equation:

$O_0=A_2+A_1+A_0 = (A_2'A_1'A_0')'$

$O_1=A_2+A_1+A_0' = (A_2'A_1'A_0)'$

$O_2=A_2+A_1'+A_0 = (A_2'A_1A_0')'$

$O_3=A_2+A_1'+A_0' = (A_2'A_1A_0)'$

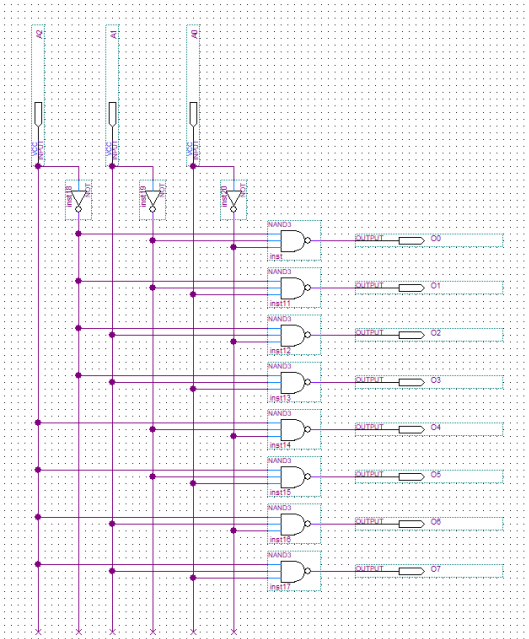
$O_4=A_2'+A_1+A_0 = (A_2A_1'A_0')'$

$O_5=A_2'+A_1+A_0' = (A_2A_1'A_0)'$

$O_6=A_2'+A_1'+A_0 = (A_2A_1A_0')'$

$O_7=A_2'+A_1'+A_0' = (A_2A_1A_0)'$

Logic Diagram:



Logic Diagram

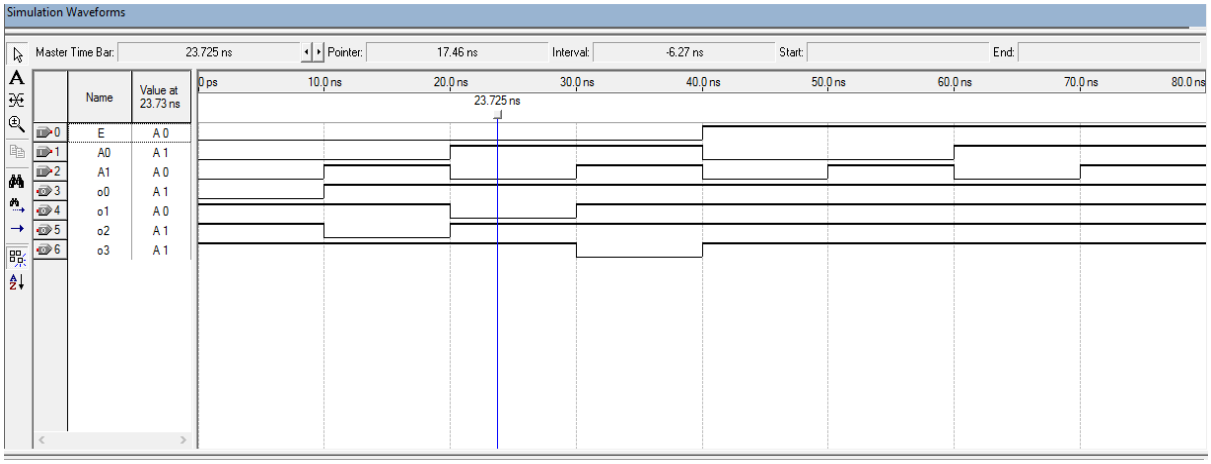
Question 3:

Write Structural Verilog code for logic diagram for 2-to-4-lines decoder with active-LOW outputs and active-LOW enable input and simulate it using Quartus II software.

Structural Verilog code:

```
module ques3(input E,A1,A0,output o0,o1,o2,o3);
nand (o0,~E,~A1,~A0),
(o1,~E,~A1,A0),
(o2,~E,A1,~A0),
(o3,~E,A1,A0);
Endmodule
```

Simulation:



Question 4:

Write Behavorial Verilog code for 3-to-8-lines decoder with active-LOW outputs and simulate it using Quartus II software.

Behavorial verilog code:

Procedural model:

```
Module3by8decoder( input A2, A1, A0, output reg o0, o1, o2, o3, o4, o5, o6, o7);
                    always@( A2, A1,A0) begin
                      case( {A2, A1, A0})
```

3′b 000 : o0=0;

3′b 001 :o1=0;

3′b 010: o2=0;

3′b 011: o3=0;

3′b 100: o4=0;

3′b 101: o5=0;

3′b 110: 06=0;

3′b 111: o7=0;

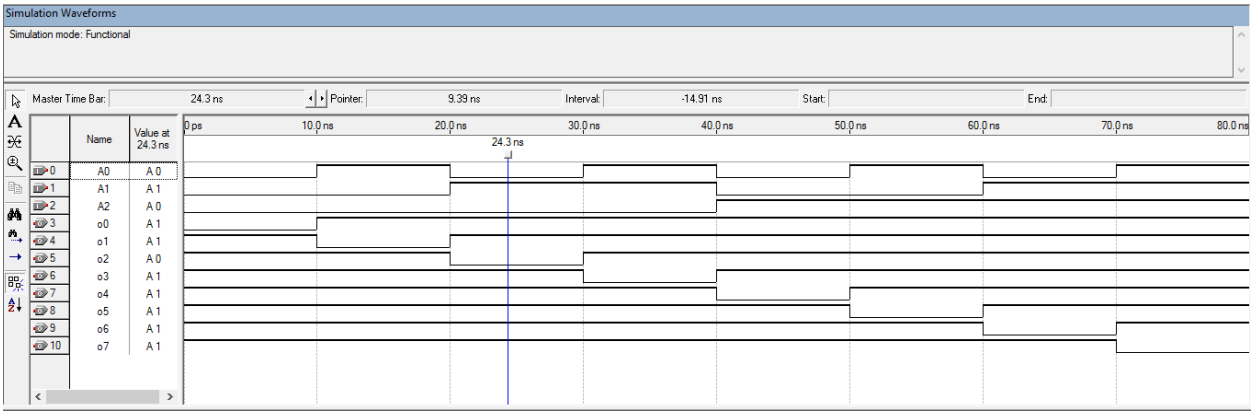
End

Endcase

Continuous assign statement:

```
module 3by8decoderassign( input A2, A1, A0, output o0, o1, o2, o3, o4, o5, o6, o7);
                                    assign o0=( ˜A2 & ˜A1 & ˜A0);
                                    assign o1=( ˜A2 & ˜A1 & A0);
                                    assign o2=( ˜A2 & A1 & ˜A0);
                                    assign o3=( ˜A2 & A1 & A0);
                                    assign o4=( A2 & ˜A1 & ˜A0);
                                    assign o5=( A2 & ˜A1 & A0);
                                    assign o6=( A2 & A1 &˜ A0);
                                    assign o7=( A2 & A1 & A0);
endmodule
```

Simulation:


Simulation Waveforms
Simulation mode: Functional
Master Time Bar: 24.3 ns
Pointer: 9.39 ns
Interval: -14.91 ns
Start:
End:
Name
Value at 24.3 ns
0 ps
10.0 ns
20.0 ns
30.0 ns
40.0 ns
50.0 ns
60.0 ns
70.0 ns
80.0 ns
24.3 ns
0 A0 A 0
1 A1 A 1
2 A2 A 0
3 o0 A 1
4 o1 A 1
5 o2 A 0
6 o3 A 1
7 o4 A 1
8 o5 A 1
9 o6 A 1
10 o7 A 1