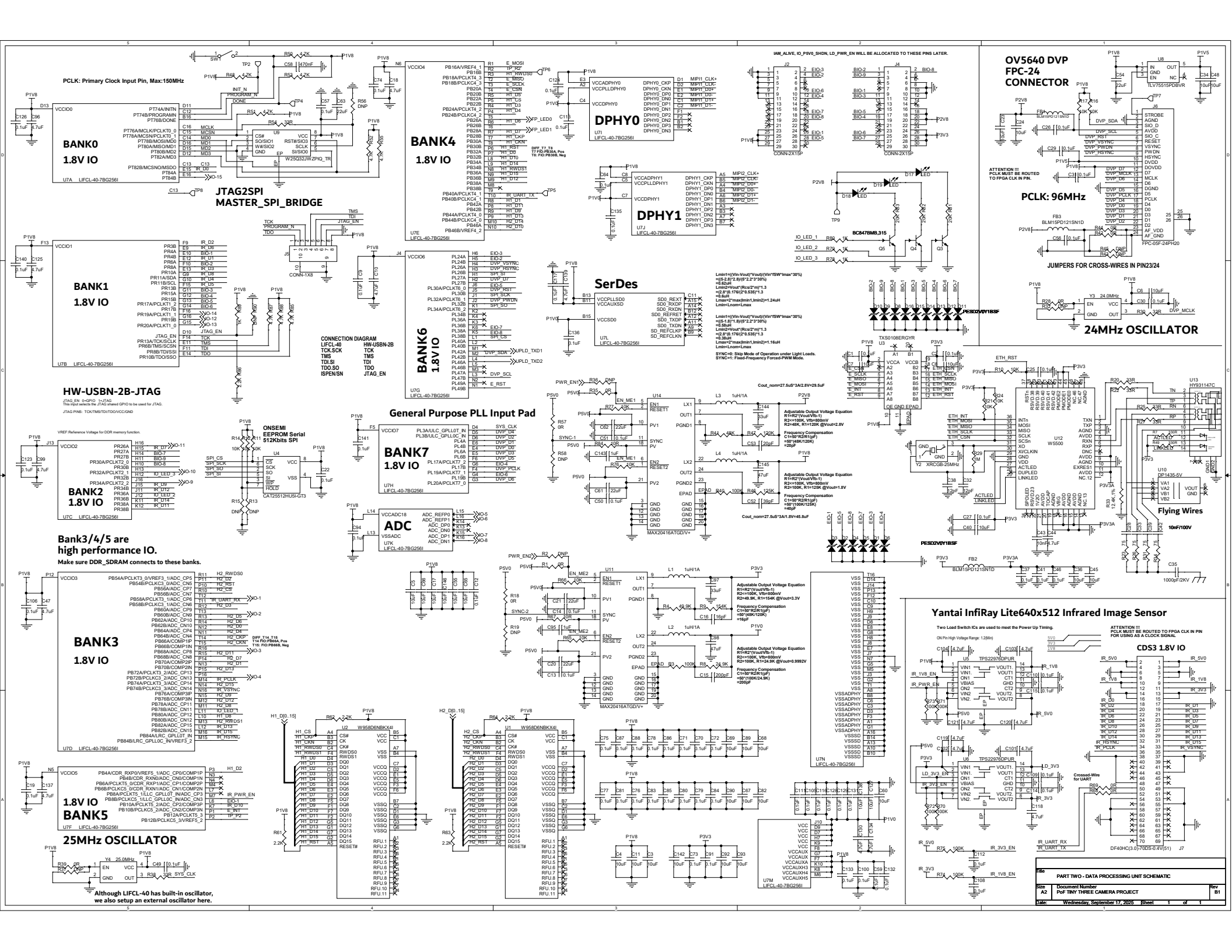
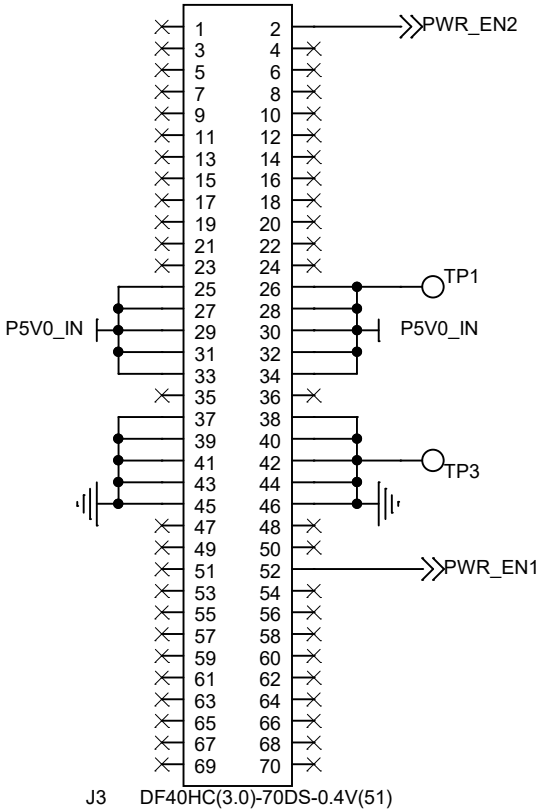
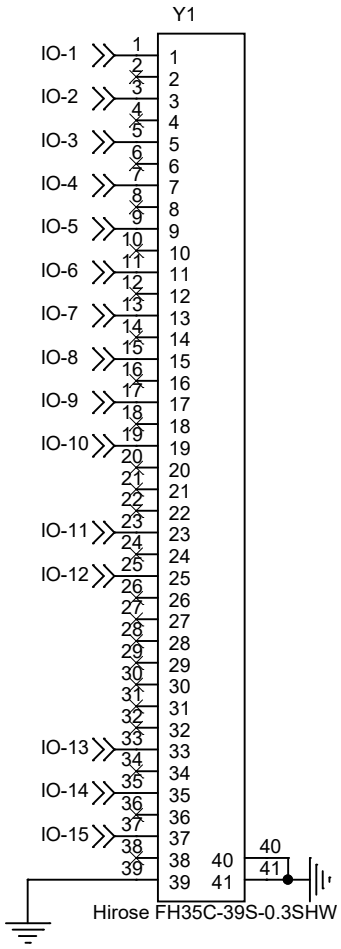

PCLK: Primary Clock Input Pin, Max:150MHz
BANK0
1.8V IO
U7A LIFCL-40-7BG256I
JTAG2SPI
MASTER_SPI_BRIDGE
BANK4
1.8V IO
U7E LIFCL-40-7BG256I
DPHY0
U7I LIFCL-40-7BG256I
CONN-2X15P
IAM_ALIVE, IO_PSV0_SHDN, LD_PWR_EN WILL BE ALLOCATED TO THESE PINS LATER.
OV5640 DVP
FPC-24
CONNECTOR
ATTENTION !!!
PCLK MUST BE ROUTED
TO FPGA CLK IN PIN.
PCLK: 96MHz
FPC-05F-24PH20
BANK1
1.8V IO
U7B LIFCL-40-7BG256I
DPHY1
U7J LIFCL-40-7BG256I
BC847BMB,315
JUMPERS FOR CROSS-WIRES IN PIN23/24
CONN-1X8
HW-USBN-2B-JTAG
JTAG_EN 0=GPIO 1=JTAG
This input selects the JTAG shared GPIO to be used for JTAG.
JTAG PINS: TCK/TMS/TDI/TDO/VCC/GND
BANK6
1.8V IO
U7G LIFCL-40-7BG256I
SerDes
U7L LIFCL-40-7BG256I
24MHz OSCILLATOR
CONNECTION DIAGRAM
LIFCL-40 HW-USBN-2B
TCK.SCK TCK
TMS TMS
TDI.SI TDI
TDO.SO TDO
ISPEN/SN JTAG_EN
PESD2V0Y1BSF
TXS0108ERGYR
General Purpose PLL Input Pad
BANK7
1.8V IO
U7H LIFCL-40-7BG256I
BANK2
1.8V IO
U7C LIFCL-40-7BG256I
ONSEMI
EEPROM Serial
512Kbits SPI
CAT25512HUSI-GT3
ADC
U7K LIFCL-40-7BG256I
MAX20416ATGD/V+
Flying Wires
10nF/100V
Bank3/4/5 are
high performance IO.
Make sure DDR_SDRAM connects to these banks.
BANK3
1.8V IO
U7D LIFCL-40-7BG256I
Yantai InfiRay Lite640x512 Infrared Image Sensor
Two Load Switch ICs are used to meet the Power Up Timing.
ON Pin High Voltage Range: 1.2(Min)
ATTENTION !!!
PCLK MUST BE ROUTED TO FPGA CLK IN PIN
FOR USING AS A CLOCK SIGNAL
CDS3 1.8V IO
TPS22976DPUR
DF40HC(3.0)-70DS-0.4V(51)
BANK5
1.8V IO
U7F LIFCL-40-7BG256I
25MHz OSCILLATOR
Although LIFCL-40 has built-in oscillator,
we also setup an external oscillator here.
W958D6NBKX4I
W25Q32JVZPIQ_TR
TLV75515PDBVR
TPS22976DPUR
TXS0108ERGYR
HY931147C
DP1435-5V
BLM15PD121SN1D
BLM15PD121SNTD
Title
PART TWO - DATA PROCESSING UNIT SCHEMATIC
Size A2
Document Number
PoF TINY THREE CAMERA PROJECT
Rev B1
Date: Wednesday, September 17, 2025
Sheet 1 of 1

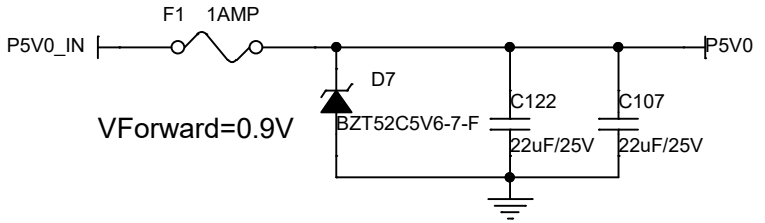
POWER FROM PSU



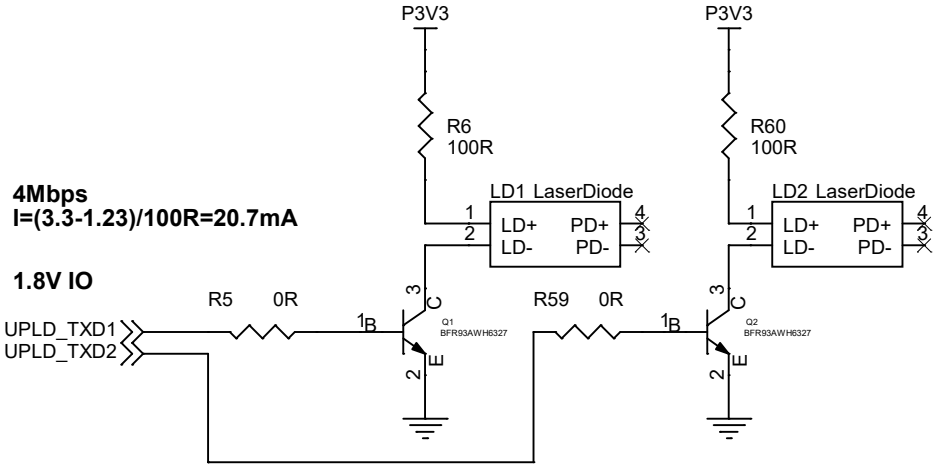
RESERVED IO



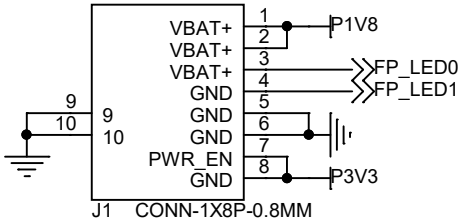
POLARITY REVERSE & OVER VOLTAGE/CURRENT PROTECTION



Vz=5.2V(MIN),5.6V(NOM),6.0V(MAX)



FRONT PANEL LED



Title: PART TWO - DATA PROCESSING UNIT SCHEMATIC		
Size: A	Document Number: PoF TINY THREE CAMERA PROJECT	Rev: B1
Date: Wednesday, September 17, 2025	Sheet 1 of 1	

```
######## 25.0MHz OSCILLATOR CLOCK INPUT.
ldc_set_location -site {D4} [get_ports iClk_25MHz]
ldc_set_attribute {USE_PRIMARY=TRUE} [get_nets iClk_25MHz]

##########Pinout for DEBUG LEDx3.
ldc_set_location -site {L11} [get_ports oLED1]
ldc_set_location -site {J12} [get_ports oLED2]
ldc_set_location -site {H12} [get_ports oLED3]
ldc_set_port -iobuf {PULLMODE=NONE IO_TYPE=LVCMOS18 CLAMP=OFF} [get_ports oLED1]
ldc_set_port -iobuf {PULLMODE=NONE IO_TYPE=LVCMOS18 CLAMP=OFF} [get_ports oLED2]
ldc_set_port -iobuf {PULLMODE=NONE IO_TYPE=LVCMOS18 CLAMP=OFF} [get_ports oLED3]


##########Pinout for FRONT PANEL LEDx2.
ldc_set_location -site {T5} [get_ports {FP_LED[0]}]
ldc_set_location -site {T6} [get_ports {FP_LED[1]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports {FP_LED[0]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports {FP_LED[1]}]

##########Pinout for HyperRAM-1.
###### DIFF_T7_T8,T7:FIO:PB30A,POS, T8:FIO:PB30B,NEG.
ldc_set_location -site {P7} [get_ports {ioH1_D[0]}]
ldc_set_location -site {R8} [get_ports {ioH1_D[1]}]
ldc_set_location -site {P3} [get_ports {ioH1_D[2]}]
ldc_set_location -site {R4} [get_ports {ioH1_D[3]}]
ldc_set_location -site {P4} [get_ports {ioH1_D[4]}]
ldc_set_location -site {R5} [get_ports {ioH1_D[5]}]
ldc_set_location -site {R6} [get_ports {ioH1_D[6]}]
ldc_set_location -site {R7} [get_ports {ioH1_D[7]}]
ldc_set_location -site {L10} [get_ports {ioH1_D[8]}]
ldc_set_location -site {R9} [get_ports {ioH1_D[9]}]
ldc_set_location -site {L8} [get_ports {ioH1_D[10]}]
ldc_set_location -site {P8} [get_ports {ioH1_D[11]}]
ldc_set_location -site {M9} [get_ports {ioH1_D[12]}]
ldc_set_location -site {P9} [get_ports {ioH1_D[13]}]
ldc_set_location -site {L9} [get_ports {ioH1_D[14]}]
ldc_set_location -site {N9} [get_ports {ioH1_D[15]}]
ldc_set_location -site {T7} [get_ports oH1_CKP]
ldc_set_location -site {T8} [get_ports oH1_CKN]
ldc_set_location -site {P5} [get_ports oH1_CSN]
ldc_set_location -site {P6} [get_ports oH1_RSTN]
ldc_set_location -site {R3} [get_ports ioH1_RWDS0]
ldc_set_location -site {N8} [get_ports ioH1_RWDS1]

ldc_set_port -iobuf {DIFFDRIVE=NA DIFFRESISTOR=OFF DRIVE=8 GLITCHFILTER=OFF OPENDRAIN=OFF SLEWRATE=FAST TERMINATION=OFF VREF=OFF IO_TYPE=LVCMOS18H CLAMP=ON PULLMODE=NONE HYSTERESIS=ON} [get_ports {ioH1_D[7]}]
ldc_set_port -iobuf {DIFFDRIVE=NA DIFFRESISTOR=OFF DRIVE=8 GLITCHFILTER=OFF OPENDRAIN=OFF SLEWRATE=FAST TERMINATION=OFF VREF=OFF IO_TYPE=LVCMOS18H CLAMP=ON PULLMODE=NONE HYSTERESIS=ON} [get_ports {ioH1_D[15]}]
ldc_set_port -iobuf {DIFFDRIVE=NA DIFFRESISTOR=OFF DRIVE=8 GLITCHFILTER=OFF OPENDRAIN=OFF SLEWRATE=FAST TERMINATION=OFF VREF=OFF IO_TYPE=LVCMOS18H CLAMP=ON PULLMODE=NONE HYSTERESIS=ON} [get_ports {ioH1_D[14]}]
ldc_set_port -iobuf {DIFFDRIVE=NA DIFFRESISTOR=OFF DRIVE=8 GLITCHFILTER=OFF OPENDRAIN=OFF SLEWRATE=FAST TERMINATION=OFF VREF=OFF IO_TYPE=LVCMOS18H CLAMP=ON PULLMODE=NONE HYSTERESIS=ON} [get_ports {ioH1_D[8]}]
ldc_set_port -iobuf {DIFFDRIVE=NA DIFFRESISTOR=OFF DRIVE=8 GLITCHFILTER=OFF OPENDRAIN=OFF SLEWRATE=FAST TERMINATION=OFF VREF=OFF IO_TYPE=LVCMOS18H CLAMP=ON PULLMODE=NONE HYSTERESIS=ON} [get_ports {ioH1_D[13]}]
ldc_set_port -iobuf {DIFFDRIVE=NA DIFFRESISTOR=OFF DRIVE=8 GLITCHFILTER=OFF OPENDRAIN=OFF SLEWRATE=FAST TERMINATION=OFF VREF=OFF IO_TYPE=LVCMOS18H CLAMP=ON PULLMODE=NONE HYSTERESIS=ON} [get_ports {ioH1_D[9]}]
ldc_set_port -iobuf {DIFFDRIVE=NA DIFFRESISTOR=OFF DRIVE=8 GLITCHFILTER=OFF OPENDRAIN=OFF SLEWRATE=FAST TERMINATION=OFF VREF=OFF IO_TYPE=LVCMOS18H CLAMP=ON PULLMODE=NONE HYSTERESIS=ON} [get_ports {ioH1_D[12]}]
ldc_set_port -iobuf {DIFFDRIVE=NA DIFFRESISTOR=OFF DRIVE=8 GLITCHFILTER=OFF OPENDRAIN=OFF SLEWRATE=FAST TERMINATION=OFF VREF=OFF IO_TYPE=LVCMOS18H CLAMP=ON PULLMODE=NONE HYSTERESIS=ON} [get_ports {ioH1_D[11]}]
ldc_set_port -iobuf {DIFFDRIVE=NA DIFFRESISTOR=OFF DRIVE=8 GLITCHFILTER=OFF OPENDRAIN=OFF SLEWRATE=FAST TERMINATION=OFF VREF=OFF IO_TYPE=LVCMOS18H CLAMP=ON PULLMODE=NONE HYSTERESIS=ON} [get_ports {ioH1_D[10]}]
ldc_set_port -iobuf {DIFFDRIVE=NA DIFFRESISTOR=OFF DRIVE=8 GLITCHFILTER=OFF OPENDRAIN=OFF SLEWRATE=FAST TERMINATION=OFF VREF=OFF IO_TYPE=LVCMOS18H CLAMP=ON PULLMODE=NONE HYSTERESIS=ON} [get_ports {ioH1_D[6]}]
ldc_set_port -iobuf {DIFFDRIVE=NA DIFFRESISTOR=OFF DRIVE=8 GLITCHFILTER=OFF OPENDRAIN=OFF SLEWRATE=FAST TERMINATION=OFF VREF=OFF IO_TYPE=LVCMOS18H CLAMP=ON PULLMODE=NONE HYSTERESIS=ON} [get_ports {ioH1_D[5]}]
ldc_set_port -iobuf {DIFFDRIVE=NA DIFFRESISTOR=OFF DRIVE=8 GLITCHFILTER=OFF OPENDRAIN=OFF SLEWRATE=FAST TERMINATION=OFF VREF=OFF IO_TYPE=LVCMOS18H CLAMP=ON PULLMODE=NONE HYSTERESIS=ON} [get_ports {ioH1_D[4]}]
ldc_set_port -iobuf {DIFFDRIVE=NA DIFFRESISTOR=OFF DRIVE=8 GLITCHFILTER=OFF OPENDRAIN=OFF SLEWRATE=FAST TERMINATION=OFF VREF=OFF IO_TYPE=LVCMOS18H CLAMP=ON PULLMODE=NONE HYSTERESIS=ON} [get_ports {ioH1_D[3]}]
ldc_set_port -iobuf {DIFFDRIVE=NA DIFFRESISTOR=OFF DRIVE=8 GLITCHFILTER=OFF SLEWRATE=FAST TERMINATION=OFF VREF=OFF IO_TYPE=LVCMOS18H CLAMP=ON PULLMODE=NONE OPENDRAIN=OFF HYSTERESIS=ON} [get_ports {ioH1_D[2]}]
ldc_set_port -iobuf {DIFFDRIVE=NA DIFFRESISTOR=OFF DRIVE=8 GLITCHFILTER=OFF SLEWRATE=FAST TERMINATION=OFF VREF=OFF IO_TYPE=LVCMOS18H CLAMP=ON PULLMODE=NONE OPENDRAIN=OFF HYSTERESIS=ON} [get_ports {ioH1_D[1]}]
ldc_set_port -iobuf {DIFFDRIVE=NA DIFFRESISTOR=OFF DRIVE=8 GLITCHFILTER=OFF SLEWRATE=FAST TERMINATION=OFF VREF=OFF IO_TYPE=LVCMOS18H CLAMP=ON PULLMODE=NONE HYSTERESIS=ON OPENDRAIN=OFF} [get_ports {ioH1_D[0]}]
ldc_set_port -iobuf {SLEWRATE=FAST VREF=OFF IO_TYPE=LVCMOS18H GLITCHFILTER=OFF HYSTERESIS=NA OPENDRAIN=OFF PULLMODE=NONE CLAMP=ON DIFFDRIVE=NA DIFFRESISTOR=OFF TERMINATION=OFF} [get_ports oH1_CKP]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18H DRIVE=8 CLAMP=ON VREF=OFF SLEWRATE=FAST} [get_ports oH1_CSN]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18H DRIVE=8 VREF=OFF SLEWRATE=FAST} [get_ports oH1_RSTN]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18H VREF=OFF TERMINATION=OFF SLEWRATE=FAST CLAMP=ON DRIVE=8 DIFFDRIVE=NA DIFFRESISTOR=OFF GLITCHFILTER=OFF PULLMODE=NONE OPENDRAIN=OFF HYSTERESIS=ON} [get_ports ioH1_RWDS0]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18H VREF=OFF TERMINATION=OFF SLEWRATE=FAST CLAMP=ON DRIVE=8 DIFFDRIVE=NA DIFFRESISTOR=OFF GLITCHFILTER=OFF OPENDRAIN=OFF PULLMODE=NONE HYSTERESIS=NA} [get_ports ioH1_RWDS1]

##########Pinout for HyperRAM-2.
###### DIFF_T14_T15,T14:FIO:PB66A,POS, T15:FIO:PB66B,NEG.
ldc_set_location -site {N12} [get_ports {ioH2_D[0]}]
ldc_set_location -site {N13} [get_ports {ioH2_D[1]}]
ldc_set_location -site {P11} [get_ports {ioH2_D[2]}]
ldc_set_location -site {R12} [get_ports {ioH2_D[3]}]
ldc_set_location -site {N11} [get_ports {ioH2_D[4]}]
ldc_set_location -site {R13} [get_ports {ioH2_D[5]}]
ldc_set_location -site {R14} [get_ports {ioH2_D[6]}]
ldc_set_location -site {P14} [get_ports {ioH2_D[7]}]
ldc_set_location -site {M11} [get_ports {ioH2_D[8]}]
ldc_set_location -site {N15} [get_ports {ioH2_D[9]}]
ldc_set_location -site {N10} [get_ports {ioH2_D[10]}]
ldc_set_location -site {R15} [get_ports {ioH2_D[11]}]
ldc_set_location -site {M12} [get_ports {ioH2_D[12]}]
ldc_set_location -site {P15} [get_ports {ioH2_D[13]}]
ldc_set_location -site {M10} [get_ports {ioH2_D[14]}]
ldc_set_location -site {N14} [get_ports {ioH2_D[15]}]
ldc_set_location -site {T14} [get_ports oH2_CKP]
ldc_set_location -site {T15} [get_ports oH2_CKN]
ldc_set_location -site {R10} [get_ports oH2_CSN]
ldc_set_location -site {P10} [get_ports oH2_RSTN]
ldc_set_location -site {R11} [get_ports ioH2_RWDS0]
ldc_set_location -site {M13} [get_ports ioH2_RWDS1]

ldc_set_port -iobuf {IO_TYPE=LVCMOS18H} [get_ports {ioH2_D[0]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18H} [get_ports {ioH2_D[1]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18H} [get_ports {ioH2_D[2]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18H} [get_ports {ioH2_D[3]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18H} [get_ports {ioH2_D[4]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18H} [get_ports {ioH2_D[5]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18H} [get_ports {ioH2_D[6]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18H} [get_ports {ioH2_D[7]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18H} [get_ports {ioH2_D[8]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18H} [get_ports {ioH2_D[9]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18H} [get_ports {ioH2_D[10]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18H} [get_ports {ioH2_D[11]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18H} [get_ports {ioH2_D[12]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18H} [get_ports {ioH2_D[13]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18H} [get_ports {ioH2_D[14]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18H} [get_ports {ioH2_D[15]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18H} [get_ports oH2_CKP]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18H} [get_ports oH2_CKN]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18H} [get_ports oH2_CSN]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18H} [get_ports oH2_RSTN]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18H} [get_ports ioH2_RWDS0]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18H} [get_ports ioH2_RWDS1]
```

CHECKLIST EMPHASIS
CKP/CKN MUST BE ROUTED TO FPGA DIFF_CLK OUTPUT PIN.

CHECKLIST EMPHASIS
CKP/CKN MUST BE ROUTED TO FPGA DIFF_CLK OUTPUT PIN.

CHECKLIST EMPHASIS
IR_PCLK MUST BE ROUTED TO FPGA CLK INPUT PIN.

```
##########Pinout for Yantai InfiRay Lite640x512 Image Sensor.
##########Configure UART. (Crossed wire here)
ldc_set_location -site {T10} [get_ports oIR_UART_TX]
ldc_set_location -site {T11} [get_ports iIR_UART_RX]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports oIR_UART_TX]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports iIR_UART_RX]

##########Power Management Signals. Pull up to enable. Pull down to disable.
ldc_set_location -site {M7} [get_ports oIR_PWR_EN]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports oIR_PWR_EN]

##########CDS3 Interface, 1 clock plus 8 data bits.
#IR_PCLK,M14,PB74A/PCLKT3_3/ADC_CP14.
ldc_set_location -site {E15} [get_ports {IR_D[0]}]
ldc_set_location -site {E12} [get_ports {IR_D[1]}]
ldc_set_location -site {F9} [get_ports {IR_D[2]}]
ldc_set_location -site {E13} [get_ports {IR_D[3]}]
ldc_set_location -site {G10} [get_ports {IR_D[4]}]
ldc_set_location -site {F15} [get_ports {IR_D[5]}]
ldc_set_location -site {E9} [get_ports {IR_D[6]}]
ldc_set_location -site {H15} [get_ports {IR_D[7]}]
ldc_set_location -site {G9} [get_ports {IR_D[8]}]
ldc_set_location -site {J15} [get_ports {IR_D[9]}]
ldc_set_location -site {K7} [get_ports {IR_D[10]}]
ldc_set_location -site {K12} [get_ports {IR_D[11]}]
ldc_set_location -site {J11} [get_ports {IR_D[12]}]
ldc_set_location -site {L12} [get_ports {IR_D[13]}]
ldc_set_location -site {K11} [get_ports {IR_D[14]}]
ldc_set_location -site {M16} [get_ports {IR_D[15]}]
ldc_set_location -site {M14} [get_ports IR_PCLK]
ldc_set_location -site {M15} [get_ports IR_HSYNC]
ldc_set_location -site {N16} [get_ports IR_VSYNC]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports {IR_D[0]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports {IR_D[1]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports {IR_D[2]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports {IR_D[3]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports {IR_D[4]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports {IR_D[5]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports {IR_D[6]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports {IR_D[7]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports {IR_D[8]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports {IR_D[9]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports {IR_D[10]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports {IR_D[11]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports {IR_D[12]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports {IR_D[13]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports {IR_D[14]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports {IR_D[15]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports IR_PCLK]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports IR_HSYNC]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports IR_VSYNC]
```

CHECKLIST EMPHASIS
iDVP_PCLK MUST BE ROUTED TO FPGA CLK INPUT PIN.

```
##########OV5640 VISIBLE-LIGHT IMAGE SENSOR.
#iDVP_PCLK,PL19A/PCLKT7_1.
ldc_set_location -site {E4} [get_ports {iDVP_D[0]}]
ldc_set_location -site {E6} [get_ports {iDVP_D[1]}]
ldc_set_location -site {D6} [get_ports {iDVP_D[2]}]
ldc_set_location -site {E5} [get_ports {iDVP_D[3]}]
ldc_set_location -site {D5} [get_ports {iDVP_D[4]}]
ldc_set_location -site {F6} [get_ports {iDVP_D[5]}]
ldc_set_location -site {G3} [get_ports {iDVP_D[6]}]
ldc_set_location -site {H2} [get_ports {iDVP_D[7]}]
ldc_set_location -site {F4} [get_ports iDVP_PCLK]
ldc_set_location -site {H4} [get_ports iDVP_VSYNC]
ldc_set_location -site {H3} [get_ports iDVP_HSYNC]
ldc_set_location -site {J5} [get_ports oDVP_RST]
ldc_set_location -site {J2} [get_ports oDVP_PWDN]
ldc_set_location -site {L3} [get_ports oDVP_SCL]
ldc_set_location -site {M2} [get_ports ioDVP_SDA]

ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports {iDVP_D[0]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports {iDVP_D[1]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports {iDVP_D[2]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports {iDVP_D[3]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports {iDVP_D[4]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports {iDVP_D[5]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports {iDVP_D[6]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports {iDVP_D[7]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports iDVP_PCLK]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports iDVP_VSYNC]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports iDVP_HSYNC]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports oDVP_RST]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports oDVP_PWDN]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports oDVP_SCL]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports ioDVP_SDA]


#W5500 TCP/IP MODULE Physical Pins.
ldc_set_location -site {P1} [get_ports iW5500_INTN]
ldc_set_location -site {T4} [get_ports oW5500_CSN]
ldc_set_location -site {T3} [get_ports oW5500_SCLK]
ldc_set_location -site {R1} [get_ports oW5500_MOSI]
ldc_set_location -site {T2} [get_ports iW5500_MISO]
ldc_set_location -site {N1} [get_ports oW5500_RSTN]

ldc_set_port -iobuf {IO_TYPE=LVCMOS18H} [get_ports iW5500_INTN]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18H} [get_ports oW5500_CSN]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18H} [get_ports oW5500_SCLK]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18H} [get_ports oW5500_MOSI]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18H} [get_ports iW5500_MISO]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18H} [get_ports oW5500_RSTN]

######## ONSEMI EEPROM SERIAL 512KBITS SPI.
ldc_set_location -site {L1} [get_ports oSPI_CS]
ldc_set_location -site {J1} [get_ports oSPI_SCK]
ldc_set_location -site {K1} [get_ports oSPI_SO]
ldc_set_location -site {H1} [get_ports iSPI_SI]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports oSPI_CS]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports oSPI_SCK]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports oSPI_SO]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18 PULLMODE=DOWN} [get_ports iSPI_SI]

#LASER DIODE UPLOAD TXD.
ldc_set_location -site {} [get_ports oUPLD_TXD1]
ldc_set_location -site {} [get_ports oUPLD_TXD2]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports oUPLD_TXD1]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports oUPLD_TXD2]

######## RESERVED IO, ROUTED TO PSU BOARD.
## PREVIOUS VERSION SIGNALS, LIKE IAM_ALIVE, IO_P5V0_SHDN, LD_PWR_EN,
## WILL BE ALLOCATED TO THESE PINS LATER.
ldc_set_location -site {L6} [get_ports {EIO[0]}]
ldc_set_location -site {H5} [get_ports {EIO[1]}]
ldc_set_location -site {H6} [get_ports {EIO[2]}]
ldc_set_location -site {G6} [get_ports {EIO[3]}]
ldc_set_location -site {J6} [get_ports {EIO[4]}]
ldc_set_location -site {G4} [get_ports {EIO[5]}]
ldc_set_location -site {K6} [get_ports {EIO[6]}]
ldc_set_location -site {K5} [get_ports {EIO[7]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports {EIO[0]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports {EIO[1]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports {EIO[2]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports {EIO[3]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports {EIO[4]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports {EIO[5]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports {EIO[6]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports {EIO[7]}]

ldc_set_location -site {E10} [get_ports {BIO[0]}]
ldc_set_location -site {F10} [get_ports {BIO[1]}]
ldc_set_location -site {G11} [get_ports {BIO[2]}]
ldc_set_location -site {G12} [get_ports {BIO[3]}]
ldc_set_location -site {G13} [get_ports {BIO[4]}]
ldc_set_location -site {G14} [get_ports {BIO[5]}]
ldc_set_location -site {H14} [get_ports {BIO[6]}]
ldc_set_location -site {H10} [get_ports {BIO[7]}]
ldc_set_location -site {H11} [get_ports {BIO[8]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports {BIO[0]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports {BIO[1]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports {BIO[2]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports {BIO[3]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports {BIO[4]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports {BIO[5]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports {BIO[6]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports {BIO[7]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports {BIO[8]}]

ldc_set_location -site {T12} [get_ports {IO[0]}]
ldc_set_location -site {T13} [get_ports {IO[1]}]
ldc_set_location -site {R16} [get_ports {IO[2]}]
ldc_set_location -site {P16} [get_ports {IO[3]}]
ldc_set_location -site {L15} [get_ports {IO[4]}]
ldc_set_location -site {L16} [get_ports {IO[5]}]
ldc_set_location -site {K15} [get_ports {IO[6]}]
ldc_set_location -site {K16} [get_ports {IO[7]}]
ldc_set_location -site {J16} [get_ports {IO[8]}]
ldc_set_location -site {H13} [get_ports {IO[9]}]
ldc_set_location -site {H16} [get_ports {IO[10]}]
ldc_set_location -site {G16} [get_ports {IO[11]}]
ldc_set_location -site {G15} [get_ports {IO[12]}]
ldc_set_location -site {F16} [get_ports {IO[13]}]
ldc_set_location -site {E16} [get_ports {IO[14]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports {IO[0]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports {IO[1]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports {IO[2]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports {IO[3]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports {IO[4]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports {IO[5]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports {IO[6]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports {IO[7]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports {IO[8]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports {IO[9]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports {IO[10]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports {IO[11]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports {IO[12]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports {IO[13]}]
ldc_set_port -iobuf {IO_TYPE=LVCMOS18} [get_ports {IO[14]}]
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Title	PART TWO - DATA PROCESSING UNIT SCHEMATIC	
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