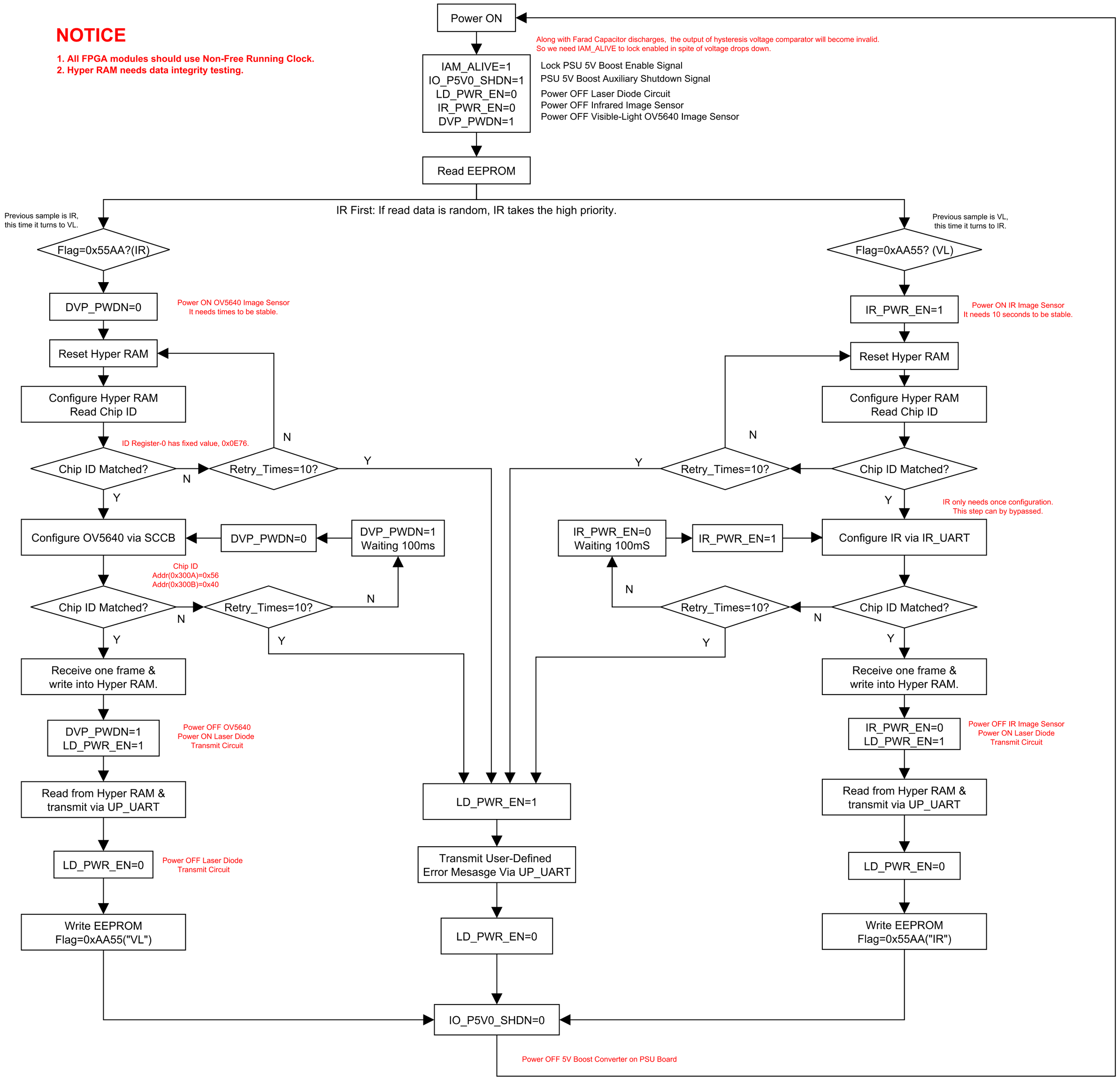
Power Over Fiber Dual Camera Workflow Diagram

NOTICE

1. All FPGA modules should use Non-Free Running Clock.
2. Hyper RAM needs data integrity testing.



IR Frame Structure and Byte Field Size

Frame Length				IR Image Sensor ID					HyperRAM ID		Reserved Area									Data Area			CRC32			
xx	xx	xx	xx	01	47	33	83	15	0E	76	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	... ...	xx	xx	xx	xx	xx

20 Bytes

n Bytes

VL Frame Structure and Byte Field Size

Frame Length				Visible Light OV5640 ID					HyperRAM ID		Reserved Area									Data Area			CRC32			
xx	xx	xx	xx	56	40	xx	xx	xx	0E	76	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	... ...	xx	xx	xx	xx	xx

Error Frame Structure and Byte Field Size

Frame Length				Error Message Type					Reserved Area											CRC32			
xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx

FF 00 00 01: Hyper RAM ID Does Not Match.
FF 00 00 02: Hyper RAM ID Data Integrity Error.
FF 00 10 01: OV5640 ID Does Not Match.
FF 00 20 01: Infrared Image Sensor ID Does Not Match.