

Edge Node System

Design Brief

Version Table

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PREFACE

This document describes the comprehensive details of Edge Node System design. This hardware system is a platform for bionic vision algorithms. It supports fast full-view imaging inside GIS device, also voice-prints data and other sensor data can be processed. More than 100 sensors are supported concurrently. Software prototypes, including Communication-Sensing-Storage-Calculation combined software module, supports images and voice-prints data analysis, nanosecond processing speed, data compressed ratio is greater than 80%. Dynamic bionic vision algorithms supports data processing in different intensity, dynamic range up to 80dB.

For applications, like partial discharging, overheating inside GIS, researching multi spectral pulse and visualization model. Researching event-driven bionic eyes sensing, transferring, processing mechanism, researching interior visualization detecting algorithms. Analyzing optics distribution, reflection and blocking factors, researching how to improve multi spectral imaging frame rate.

All personnel involved in this project, including engineers, researchers, and project managers, should refer to this document for comprehensive design details and implementation guidelines.

Abbreviation Table

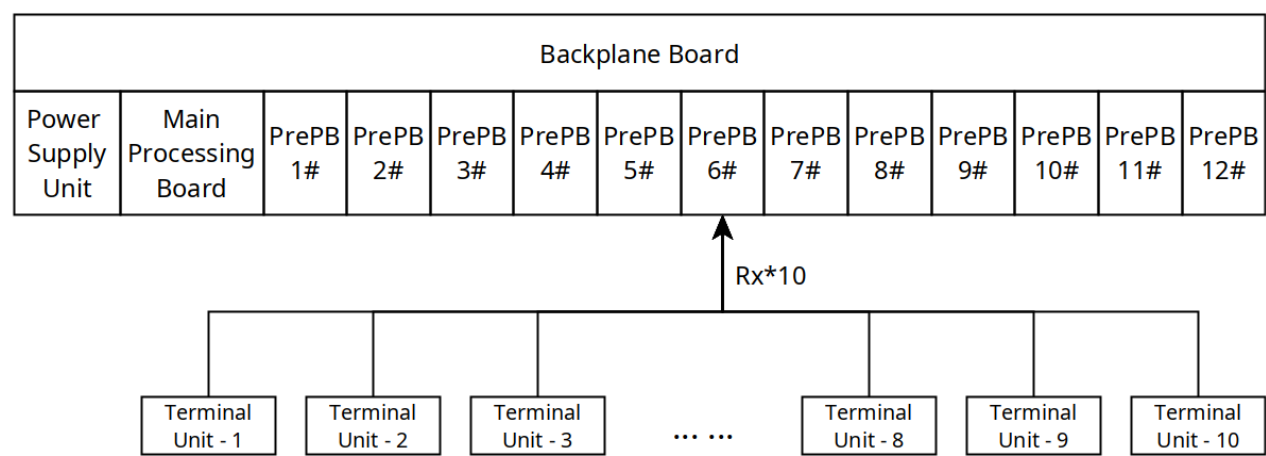
No.	Abbreviation	Full Spelling
1	MainPB	Main Processing Board
2	PrePB	Pre-Processing Board
3	PSU	Power Supply Unit
4	TU	Terminal Unit
5	BPB	Backplane Board
6	ID	Identification
7	SDR	Single Date Rate
8	DDR	Double Date Rate

1. System Topology

The entire Edge Node system is split into four parts, one BPB board, one PSU board, one MainPB and 12 PrePBs. All boards will be installed on BPB. BPB servers electrical connection and physical reinforcement.

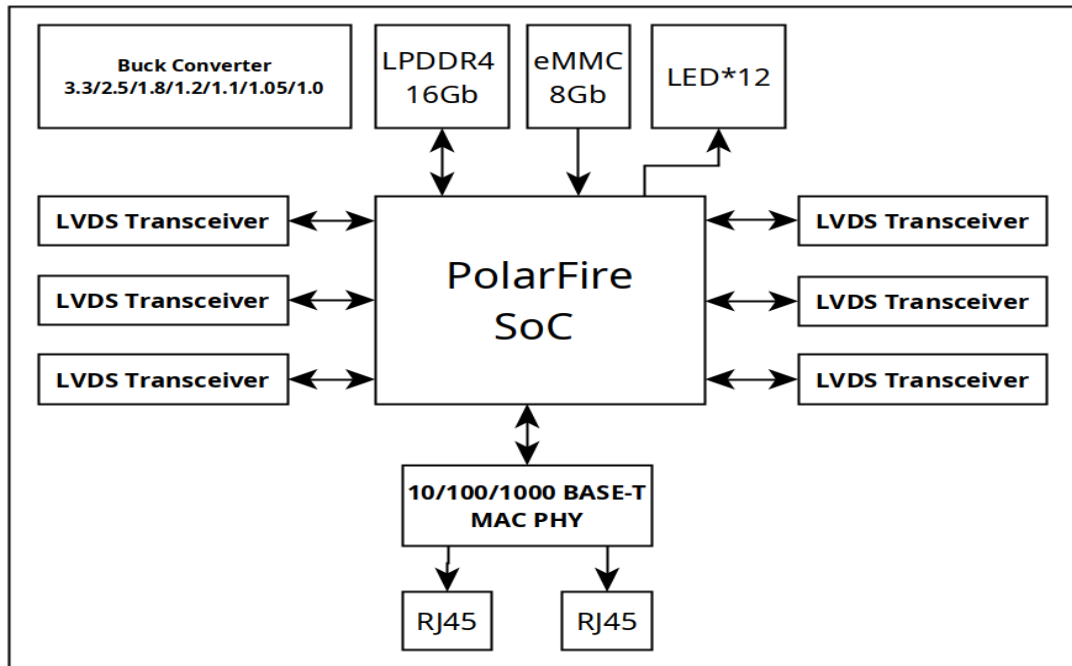
PSU distributes power supply to all boards. PrePB Board receives all data uploading from TUs. Each PrePB has 10 receive channels, all PrePB boards are capable of handling 120 TUs. The function of PrePB is to pre-process data, apply different algorithms then transfer to MainPB. BPB features all transmit and receive LVDS channels and distributes power supply, it also support physical connection.

MainPB aims to collect all PrePB data and transfer out via 100/1000Base-T Ethernet. PrePB has responsibility of collecting all raw data from terminal units, apply various of pre-processing algorithms then upload the result to MainPB.



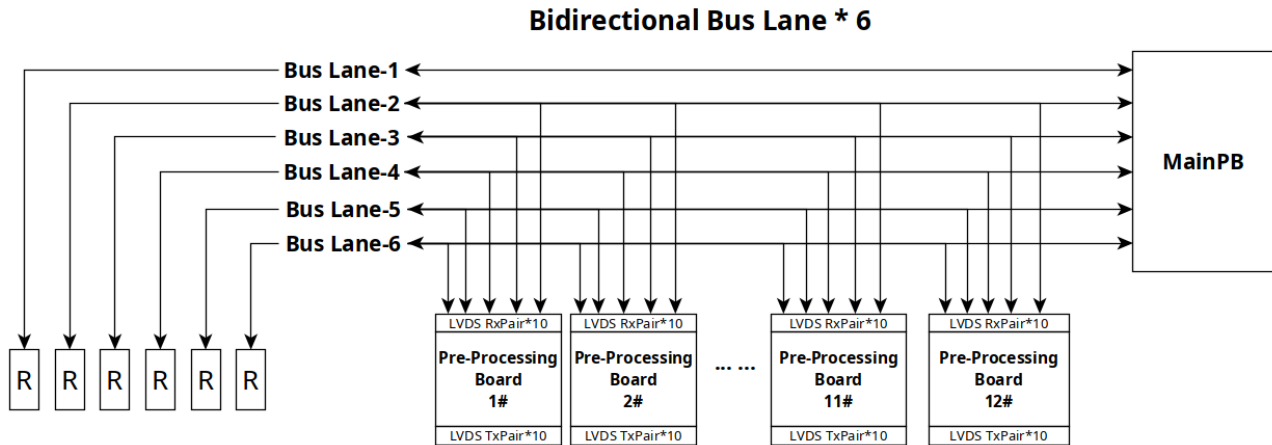
2. MainPB Architecture

Following figure shows the brief architecture of MainPB board. The main controller we use is Microchip PolarFire SoC FPGA, model type is MPFS250T-ECVG484EES. We expand an LPDDR4 SDRAM with memory size 16Gb onboard, the MAC PHY chip VSC8662 has two built-in MAC layers to support two RJ45 sockets for 10/100/1000Mbps Ethernet, an eMMC chip with memory size 8Gb is used for MSS subsystem. We also design 12 LEDs to indicate the status of respective channel. Six independent LVDS channels, bidirectional transceiver. With this feature, MainPB can broadcast data to all PrePBs and recall data from each PrePB.



2.1 Bus Lane Overview

There are six bus lanes on board. They support bidirectional communication, but only work in half-duplex mode. The direction can be configured by software to suit different application needs. Each lane contains 10 differential signals, CS, CLK and D0~D7. All data are synchronized to CLK.



2.2 Bus Lane Configuration

From hardware design view, all bus lanes are bidirectional. Each lane is half-duplex, it only can be used as transmit or receive at the same time. For special applications that the requirement of uploading bandwidth is higher than downloading, users can configure five bus lanes as uploading, one bus lane as downloading. When the downloading finishes, the bus lane also can be switched to uploading. Here are some possible configurations.

2.2.1 Downloading(1) and Uploading(5)

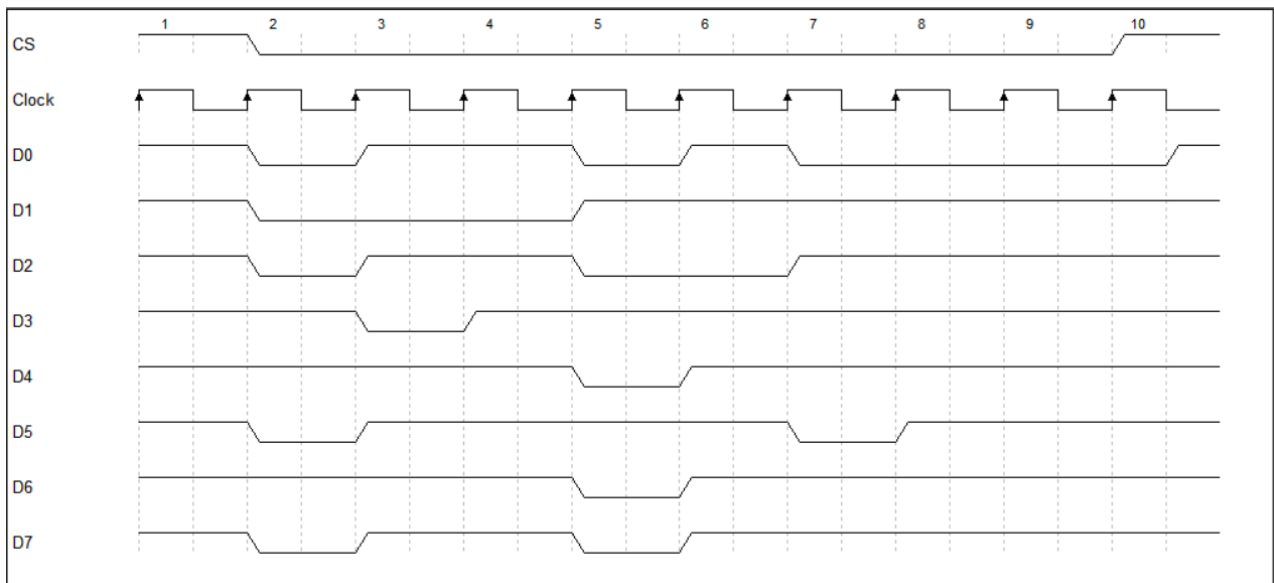
Direction	Bus Lane	Data Flow	MainPB	PrePB	Communication
Downloading	Bus Lane-1	MainPB → All PrePBs	Tx	Rx	Broadcast or Point to Point
Uploading	Bus Lane-2	PrePB(1/6/11) → MainPB	Rx	Tx	Poll each device sequentially
	Bus Lane-3	PrePB(2/7/12) → MainPB	Rx	Tx	Poll each device sequentially
	Bus Lane-4	PrePB(3/8) → MainPB	Rx	Tx	Poll each device sequentially
	Bus Lane-5	PrePB(4/9) → MainPB	Rx	Tx	Poll each device sequentially
	Bus-Lane-6	PrePB(5/10) → MainPB	Rx	Tx	Poll each device sequentially

2.2.2 Downloading Work Principle

Downloading Bus Lane can work in SDR or DDR mode. In SDR mode, each clock period it carries 8-bits. In DDR mode, each clock period it carries 16-bits. During download period, MainPB transmits data, all PrePBs that connected on download bus can receive data simultaneously. Since each PrePB has its own unique address, it can recognize whether the data on Downloading Bus Lane belongs to it or not.

There are two types of address on protocol layer, Broadcast Address and Device Address. If MainPB sends data with broadcast address, all PrePBs could receive and process. But if MainPB sends data with a specific device address, only the corresponded PrePB could take action, others stay idle.

MainPB sends data at rising edge of clock, PrePB latches data in at falling edge of clock. CS remains low during the single progress, CS pulls high to end single transferring.



2.2.3 Uploading Work Principle

The Uploading Bus Lane is a synchronous and time-shared bus. In above configuration, three PrePBs use it to upload data, so how to prevent the bus arbitration is a critical problem. In this design, we intend to use Request/Response communication mechanism which is also well-known as Master/Slave. MainPB plays the master role, it issues command over Downloading Bus. On Downloading Bus, Only MainPB is the master, all PrePBs are slaves. Once master sends command, all slaves could receive command simultaneously. All slaves receive commands and compare the address field contained in command to itself unique ID, if they're matched, the addressed slave takes action. If not matched, abandon this command and be ready to receive next command.

Since the uploading bus is multiple nodes shared, MainPB uses polling mechanism to request data from each PrePB. Normally, the addressed PrePB responds commands and uploads data, it uploads a fixed series bytes to mark the end. MainPB receives and recognizes the end mark, then poll next PrePB. In some applications, TU data are not needed to be pre-processed, TU transmits data to PrePB directly. Therefore, the FPGA located on PrePB board can be bypassed to reduce latency and complication.

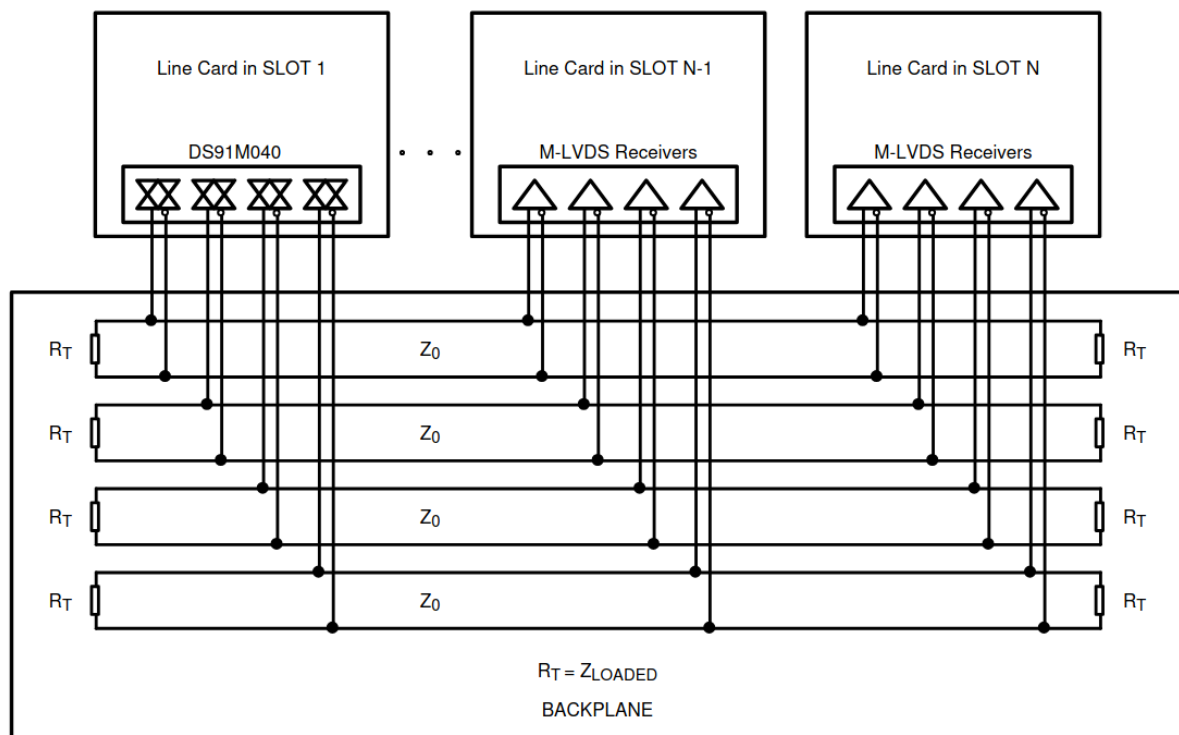
MainPB also have timeout mechanism to prevent abnormal circumstances, likely PrePB does not work well, or it's missed. This prevents MainPB enters a dead-waiting state.

In some applications, TU data are not needed to be pre-processed, TU transmits data to PrePB directly. Therefore, the FPGA located on PrePB board can be bypassed to reduce latency and complication.

2.4 LVDS Transceiver

In our design, we use DS91M040 LVDS Transceiver. The DS91M040 is a quad Multipoint LVDS transceiver designed for driving/receiving clock or data signals to/from to four multipoint networks. A single channel is a half-duplex transceiver that accepts LVTTTL/LVCMOS signals at the driver inputs and converts them to differential M-LVDS signal levels. The receiver inputs accept low voltage differential signals (LVDS, BLVDS, M-LVDS, LVPECL and CML) and convert them to 3V LVCMOS signals.

The DS91M040 supports up to 125MHz, maximum data rate is 250Mbps in DDR mode. Its differential output voltage magnitude is between 480mV and 650mV at the condition of load 50-ohms and 5pF.



2.5 Bandwidth Consideration

MainPB must have performance to handle 12 input channels concurrently. In this design, we assume the data rate of each channel is up to 10Mbps. If all channels data come simultaneously, the input data rate will be 120Mbps, MainPB must receive all data and store in LPDDR4 SDRAM temporarily. The capacity is 16Gbits, adequate for data buffering. After FPGA logic writes all data to SDRAM, it notifies RISC-V to transfer data out via Ethernet.

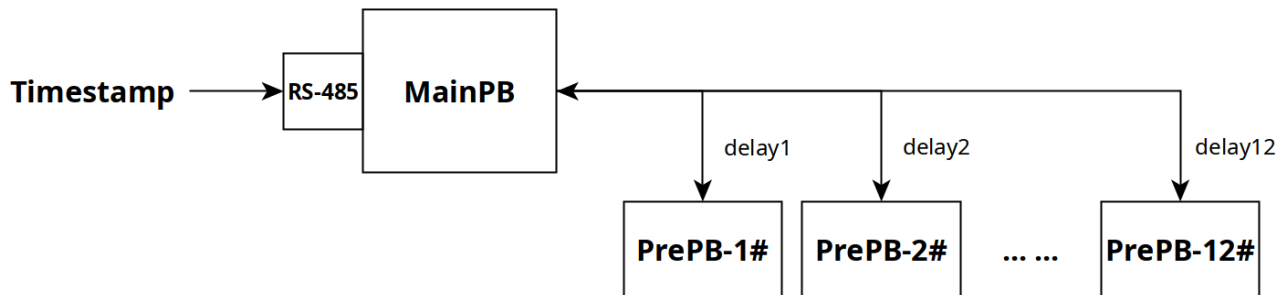
Since all data have been processed on PrePB boards, the stress suffered on MainPB declined. In order to double the bandwidth, the bus lanes can work in DDR mode. Following table shows the comparison of Six Bus Lanes bandwidth working in different mode.

Bus	Work Mode	Clock (MHz)	Data width (bits)	Bandwidth (Mbps)
Bus Lane	SDR	10	8	80
		20	8	160
		25	8	200
	DDR	10	8	160
		20	8	320
		25	8	400

2.6 Time Synchronization

The time synchronization mechanism is designed to ensure accurate and consistent timekeeping across all distributed nodes in this system. This mechanism will enable precise coordination, logging and event sequencing for nodes that require time accuracy.

MainPB works as the master node, all PrePBs works as slave nodes. Master node receives timestamps from RS-485 interface, then broadcast timestamps to all slave nodes, slave nodes calculate delay and adjust their clock accordingly. This achieves precise time synchronization across all slave nodes. Support for PTP(Precision Time Protocol), NTP(Network Time Protocol), and GNSS-based synchronization. On board, FPGA or micro-controller for time stamping and synchronization management. Each board has a high stability oscillator to minimize synchronization drift and latency.



2.7 Power Rails

Following table lists power rails requirement of key components in this system, involves the main hybrid SoC, LPDDR4 SDRAM, SGMII network interface, eMMC and LVDS transceivers. After merged, 3.3V 2.5V 1.8V 1.2V 1.1V are needed. It's better to use a Power Management IC that supports five power rails rather than several discrete chips. A PMIC is a great choice for reducing board space and improve efficiency.

No.	Component	Power Requirement
1	MPFS250T	3.3V 2.5V 1.8V 1.1V
1	LPDDR4	1.8V 1.1V
2	SGMII	3.3V 1.2V
3	eMMC	3.3V 1.8V
4	LVDS Transceiver	3.3V

2.8 Status Indication

MainPB should indicate the status of all PrePBs through LED Flashing. The FPGA Logic should control the flashing frequency of LED to assist with maintenance. Likely, slow flashing, fast flashing, continuous on and off.

Limited by mechanical front panel size, only 12 LEDs are provided on board. Each LED indicates respective channel status by different flashing combination.

Comprehensive LED status will be defined in software design document.

3. PrePB Architecture

3.1 PrePB Requirement

PrePB must support up to 10 input channels. The maximum data rate is 10Mbps. And considering all channels data may come simultaneously. So the bandwidth of output port should be $10\text{Mbps} \times 10 = 100\text{Mbps}$ at least. If PrePB can't transfer data out in data rate of 100Mbps, data will lose. The bandwidth between input port and output port are not match. A better way to solve this problem is adding an external DDR SDRAM.

Following table shows single frame data size of different image sensors. This table offers a reference approximately, it determines the capacity of DDR SDRAM that we need. Bigger resolution, more capacity. Here one frame of Visible-Light Image, the data size is 75Mbits. For 10 channels, we need $75\text{Mbits} \times 10 = 750\text{Mbits}$. So strongly recommend to place a 2Gb DDR SDRAM on board.

/	Visible-Light Image	Infrared Image		Ultraviolet Image
Resolution	2560*1920	640*512	256*192	1280*1024
Data Depth	16-bits	14-bits	14-bits	8-bits
Total (in bits)	75Mbits	5Mbits	0.75Mbits	20Mbits

Total (in Bytes)	9.37MBytes	0.62MBytes	0.09MBytes	2.5MBytes
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3.2 Bandwidth Consideration

The ideal situation is the output bandwidth matched to input bandwidth, so no data will lose. In this design, each PrePB has 10 input channels data stream and the data rate is up to 10Mbps, that means if all channels data come in simultaneously, the input bandwidth will be 100Mbps. But we only have one output port with 20MHz in SDR mode. Even if we operate it in DDR mode, the bandwidth is 40Mbps. Not matched perfectly.

So pre-processing data is essential to reduce bandwidth cost. With less data size, PrePB can transfer data out in time.

3.3 Channel Status Indication

PrePB should indicate the status of all channels through LED Flashing. The FPGA Logic will control the flashing frequency of LED to assist with maintenance. Likely, slow flashing, fast flashing, continuous on and off.

Comprehensive LED status will be defined in software design document.

4. Power Supply Unit

The PSU board supplies power to all electric components. It accepts 180VAC~230VAC input, converts AC to DC, outputs 12V power rails with 25A maximum current. The PSU board has over-current protection, thermal protection and smart fan controller.

4.1 Key Parameters

Following table shows key parameters of power supply unit.

Item	Parameter	Memo
Topology	AC/DC	
Input Voltage Range	180VAC~230VAC 50Hz	
Output Voltage	12V	
Output Current (Max.)	25A	
Ripple and Noise		
Power Efficiency	90%	
Load Regulation		
Line Regulation		
Overload Protection	Support	Alarm
Thermal Protection	Support	Alarm and shutdown when overheated.

4.2 Power Consumption Estimation

Following table shows the power supply requirement of each board. This is the maximum estimation, at least 20% safety margins are acceptable.

Board Name	Power Consumption	
MainPB	6 Watts	12V/0.5A
PrePB		

5. Backplane Board

5.1 Connector Pin Assignment

The aim of BPB is to distribute power supply and route bus signals. And also LVDS terminate resistors on board. In this design, BPB has 14 sockets totally, each socket integrates two connectors, the top connector is used to distribute power supply and LVDS pairs. For the bottom connector, it routes ID allocation and LVDS pairs. Following table shows pin assignment.

There are 60 LVDS pairs totally in the back plane board. LVDS transceivers we use only work in half-duplex mode, software layers determine the direction. The minimum swing is only 460mV, PCB layout must be very careful to reduce impact from impedance match.

Normally, 30% safety margins are acceptable, for the connector we're using, current capacity of each pin is 200mA approximately. We assign 9 pins to distribute 12V voltage, the maximum current capacity is calculated by the equation, $200\text{mA} \times 9 = 1.8\text{A}$. The numbers of GND pin is twice times of 12V.

Current carrying capacity of PCB vias are described as below for a reference guideline.

Via Diameter	Max Current
0.15mm	0.5A
0.2mm	0.7A
0.3mm	1A
0.4mm	1.5A
0.5mm	2A
0.6mm	2.5A
0.8mm	4A
1.0mm	6A

No.	Top Connector – 3x32P						Bottom Connector – 3x32P					
1	A1	12V	A2	12V	A3	12V	A1	GND	A2	GND	A3	GND
2	B1	12V	B2	12V	B3	12V	B1	TR25_P	B2	TR13_P	B3	TR1_P
3	C1	12V	C2	12V	C3	12V	C1	TR25_N	C2	TR13_N	C3	TR1_N
4	D1	GND	D2	GND	D3	GND	D1	TR26_P	D2	TR14_P	D3	TR2_P
5	E1	GND	E2	GND	E3	GND	E1	TR26_N	E2	TR14_N	E3	TR2_N
6	F1	GND	F2	GND	F3	GND	F1	GND	F2	GND	F3	GND
7	G1	GND	G2	GND	G3	GND	G1	TR27_P	G2	TR15_P	G3	TR3_P
8	H1	GND	H2	GND	H3	GND	H1	TR27_N	H2	TR15_N	H3	TR3_N
9	I1	GND	I2	GND	I3	GND	I1	TR28_P	I2	TR16_P	I3	TR4_P
10	J1	TR53_P	J2	TR45_P	J3	TR37_P	J1	TR28_N	J2	TR16_N	J3	TR4_N
11	K1	TR53_N	K2	TR45_N	K3	TR37_N	K1	GND	K2	GND	K3	GND
12	L1	GND	L2	GND	L3	GND	L1	TR29_P	L2	TR17_P	L3	TR5_P
13	M1	TR54_P	M2	TR46_P	M3	TR38_P	M1	TR29_N	M2	TR17_N	M3	TR5_N
14	N1	TR54_N	N2	TR46_N	N3	TR38_N	N1	TR30_P	N2	TR18_P	N3	TR6_P
15	O1	GND	O2	GND	O3	GND	O1	TR30_N	O2	TR18_N	O3	TR6_N
16	P1	TR55_P	P2	TR47_P	P3	TR39_P	P1	GND	P2	GND	P3	GND
17	Q1	TR55_N	Q2	TR47_N	Q3	TR39_N	Q1	TR31_P	Q2	TR19_P	Q3	TR7_P
18	R1	GND	R2	GND	R3	GND	R1	TR31_N	R2	TR19_N	R3	TR7_N
19	S1	TR56_P	S2	TR48_P	S3	TR40_P	S1	TR32_P	S2	TR20_P	S3	TR8_P
20	T1	TR56_N	T2	TR48_N	T3	TR40_N	T1	TR32_N	T2	TR20_N	T3	TR8_N
21	U1	GND	U2	GND	U3	GND	U1	GND	U2	GND	U3	GND
22	V1	TR57_P	V2	TR49_P	V3	TR41_P	V1	TR33_P	V2	TR21_P	V3	TR9_P
23	W1	TR57_N	W2	TR49_N	W3	TR41_N	W1	TR33_N	W2	TR21_N	W3	TR9_N
24	X1	GND	X2	GND	X3	GND	X1	TR34_P	X2	TR22_P	X3	TR10_P
25	Y1	TR58_P	Y2	TR50_P	Y3	TR42_P	Y1	TR34_N	Y2	TR22_N	Y3	TR10_N
26	Z1	TR58_N	Z2	TR50_N	Z3	TR42_N	Z1	GND	Z2	GND	Z3	GND
27	AA1	GND	AA2	GND	AA1	GND	AA1	TR35_P	AA2	TR23_P	AA1	TR11_P
28	AB1	TR59_P	AB2	TR51_P	AB1	TR43_P	AB1	TR35_N	AB2	TR23_N	AB1	TR11_N
29	AC1	TR59_N	AC2	TR51_N	AC1	TR43_N	AC1	TR36_P	AC2	TR24_P	AC1	TR12_P
30	AD1	GND	AD2	GND	AD1	GND	AD1	TR36_N	AD2	TR24_N	AD1	TR12_N
31	AE1	TR60_P	AE2	TR52_P	AE1	TR44_P	AE1	GND	AE2	GND	AE1	ID1
32	AF1	TR60_N	AF2	TR52_N	AF1	TR44_N	AF1	ID2	AF2	ID3	AF1	ID4

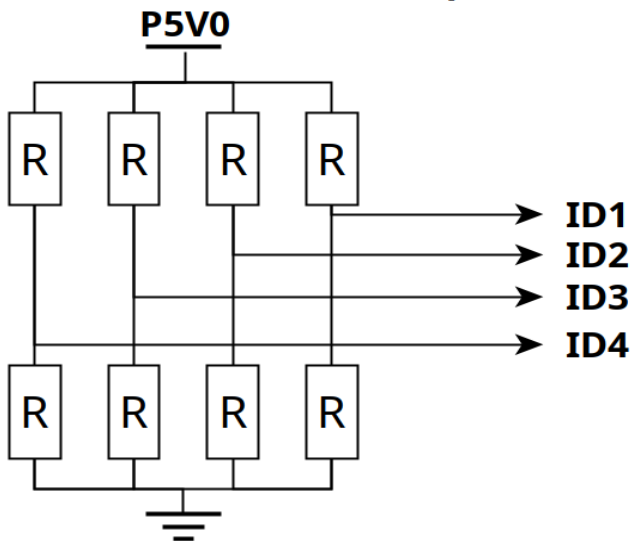
5.2 ID Allocation

Since we have 12 PrePB boards connected in parallel, so there's ID allocation circuit designed special for PrePB boards recognition. Initially, PrePBs has no fixed ID. Once it's plugged into BPB, BPB allocates a unique ID to it. Later, PrePB read this ID to transfer data and response command from MainPB. MainPB distinguishes each PrePB by unique ID accurately.

Here, 4 bits can address $2^4=16$ boards, adequate for our needs. ID[4:1]=1111 is the broadcast ID, it means that the command will be send to all PrePBs.

Place these circuit beside each socket on In some applications, TU data are not needed to be pre-processed, TU transmits data to PrePB directly. Therefore, the FPGA located on PrePB board can be bypassed to reduce latency and complication. BPB, and soldering respective resistors in fabrication. Duplicated IDs could cause confusion and data collision.

Backplane Board ID Allocation



ID[4:1]	Board
0000	MainPB
0001	PrePB-1
0010	PrePB-2
0011	PrePB-3
0100	PrePB-4
0101	PrePB-5
0110	PrePB-6
0111	PrePB-7
1000	PrePB-8
1001	PrePB-9
1010	PrePB-10
1011	PrePB-11
1100	PrePB-12
1101	Reserved
1110	PSU
1111	Broadcast

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