Edge Node System

Design Brief

Version Table

Version No.	Contents	Author	Date
V0.0.1	The Initial Version	Anonymous	March 20, 2025
V0.0.2	Append more contents.	Anonymous	April 2, 2025

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PREFACE

This document describes the comprehensive details of Edge Node System design. This hardware system is a platform for bionic vision algorithms. It supports fast full-view imaging inside GIS device, also voice-prints data and other sensor data can be processed. More than 100 sensors are supported concurrently. Software prototypes, including Communication-Sensing-Storage-Calculation combined software module, supports images and voice-prints data analysis, nanosecond processing speed, data compressed ratio is greater than 80%. Dynamic bionic vision algorithms supports data processing in different intensity, dynamic range up to 80dB.

For applications, like partial discharging, overheating inside GIS, researching multi spectral pulse and visualization model. Researching event-driven bionic eyes sensing, transferring, processing mechanism, researching interior visualization detecting algorithms. Analyzing optics distribution, reflection and blocking factors, researching how to improve multi spectral imaging frame rate.

All personnel involved in this project, including engineers, researchers, and project managers, should refer to this document for comprehensive design details and implementation guidelines.

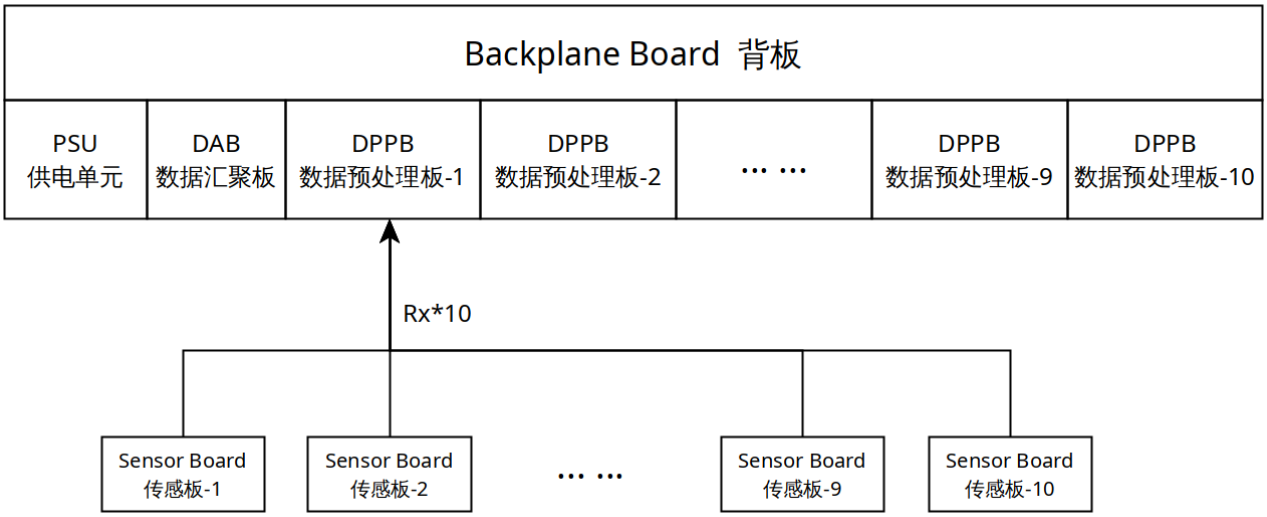
Abbreviation Table

No.	Abbreviation	Full Spelling
1	DAB	Data Aggregation Board
2	DPPB	Data Pre-Processing Board
3	PSU	Power Supply Unit
4	SB	Sensor Board
5	BPB	Backplane Board
6	ID	Identification
7	SDR	Single Date Rate
8	DDR	Double Date Rate

1. System Topology

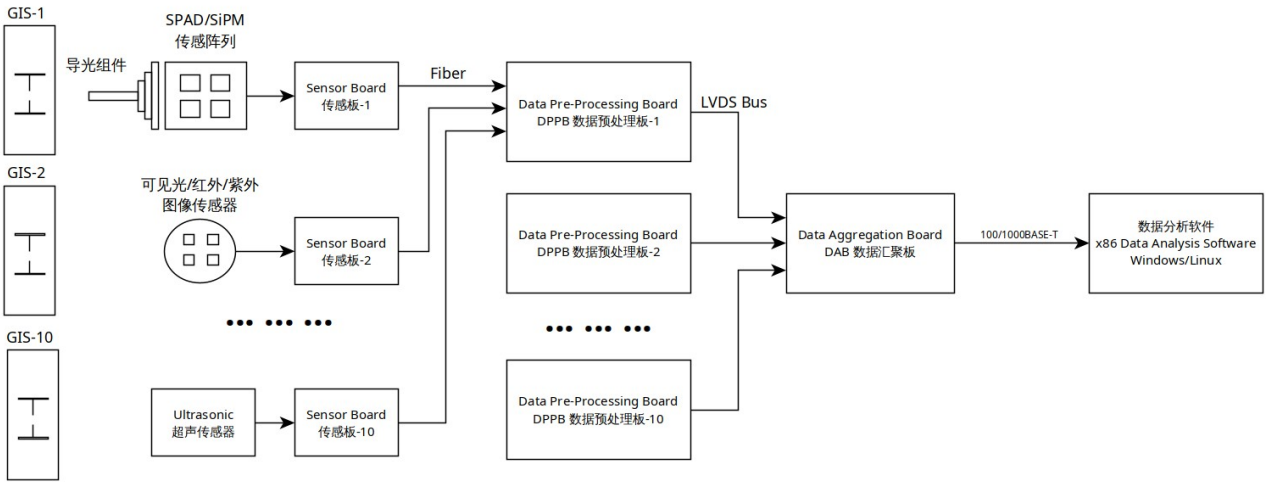
1.1 Block Diagram

The entire Edge Node system is split into four parts, 1 BPB board, 1 PSU board, 1 DAB and 10 DPPBs. All boards will be installed on BPB. BPB servers electrical connection and physical reinforcement.

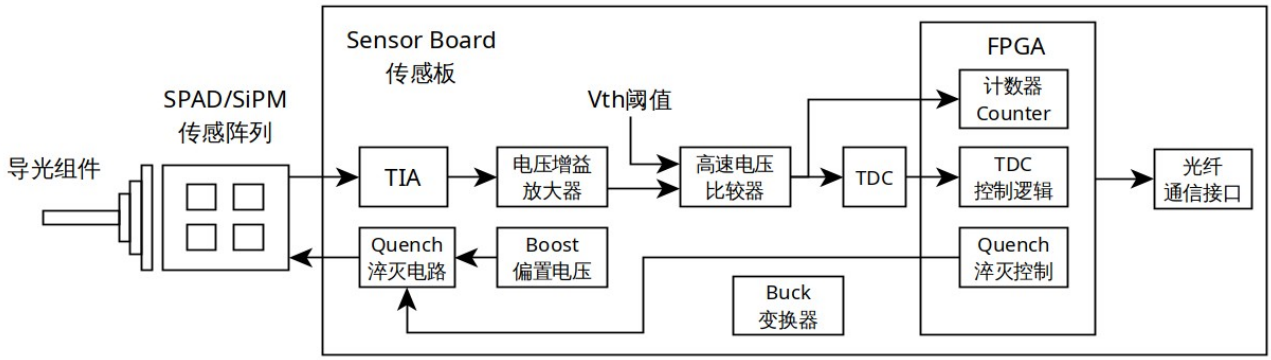


PSU distributes power supply to all boards. The DPPB Board receives all data uploading from various sensor boards. Each DPPB has 10 receive channels, all DPPB boards are capable of handling up to 100 sensors. The function of DPPB is to pre-process data, apply different algorithms then transfer results to DAB. BPB features all transmit and receive high speed LVDS channels and distributes power supply, it also supports physical connection.

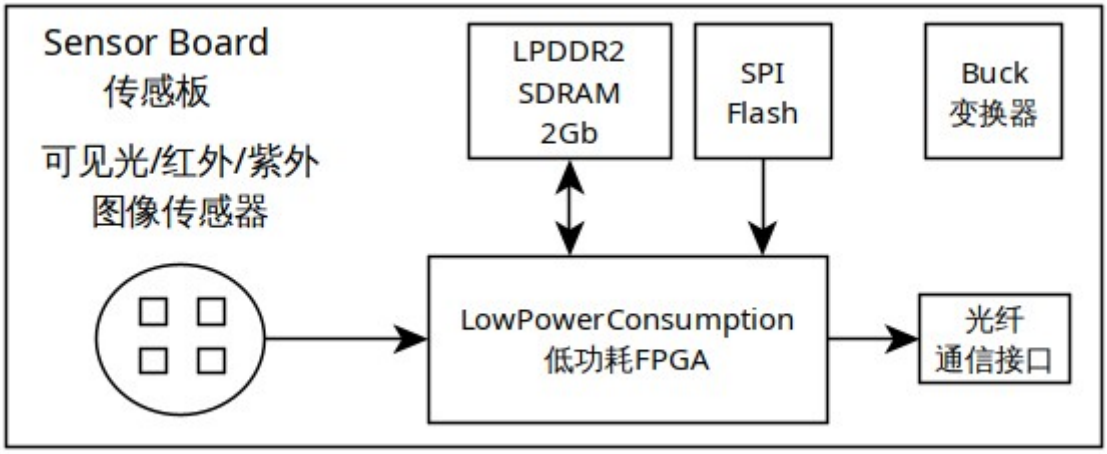
DAB aims to collect all DPPB data and transfer out via 100/1000Base-T Ethernet. DPPB has responsibility of collecting all raw data from sensor boards, apply various of pre-processing algorithms then upload the result to DAB.



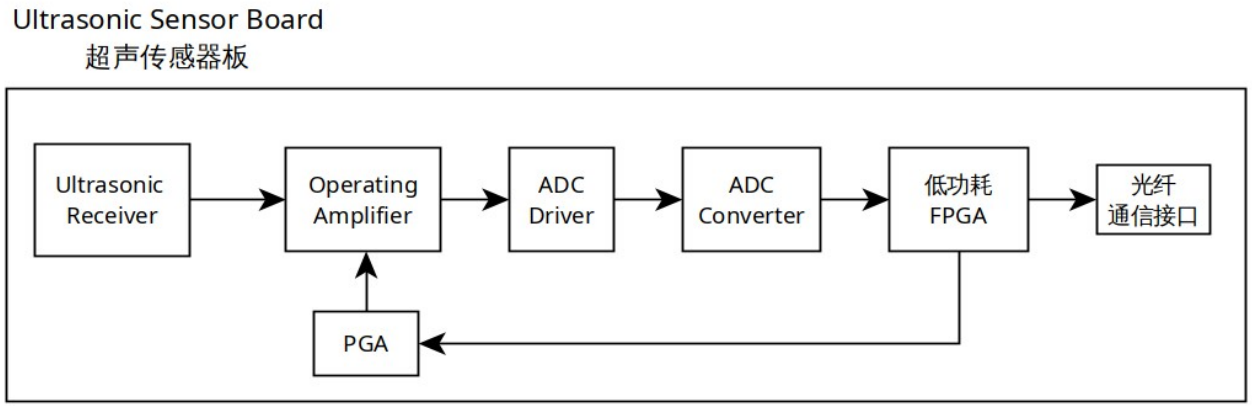
1.2 Optical Partial Discharging Sensor Board



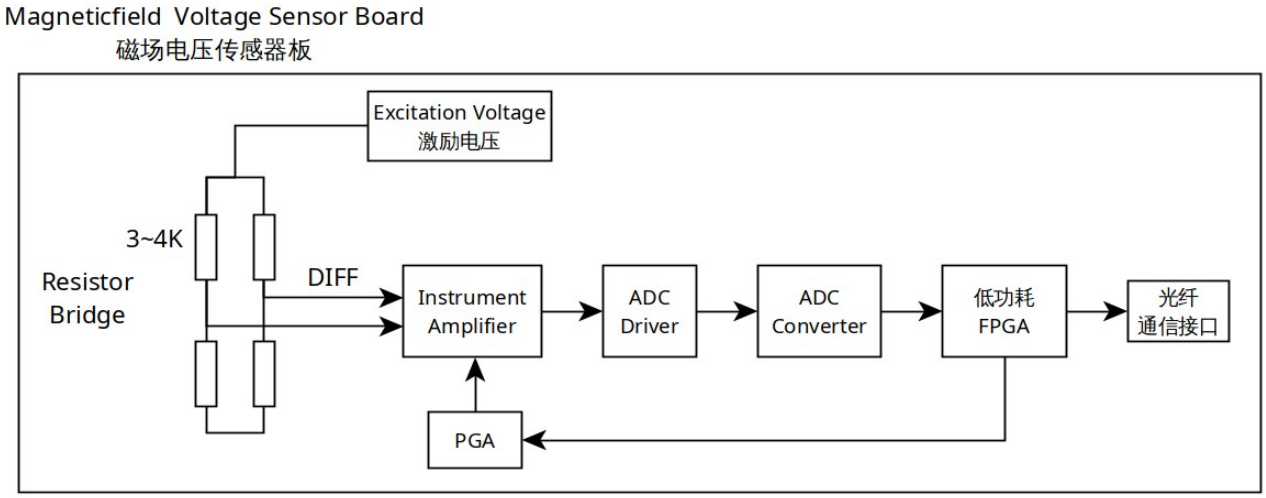
1.3 Camera Sensor Board



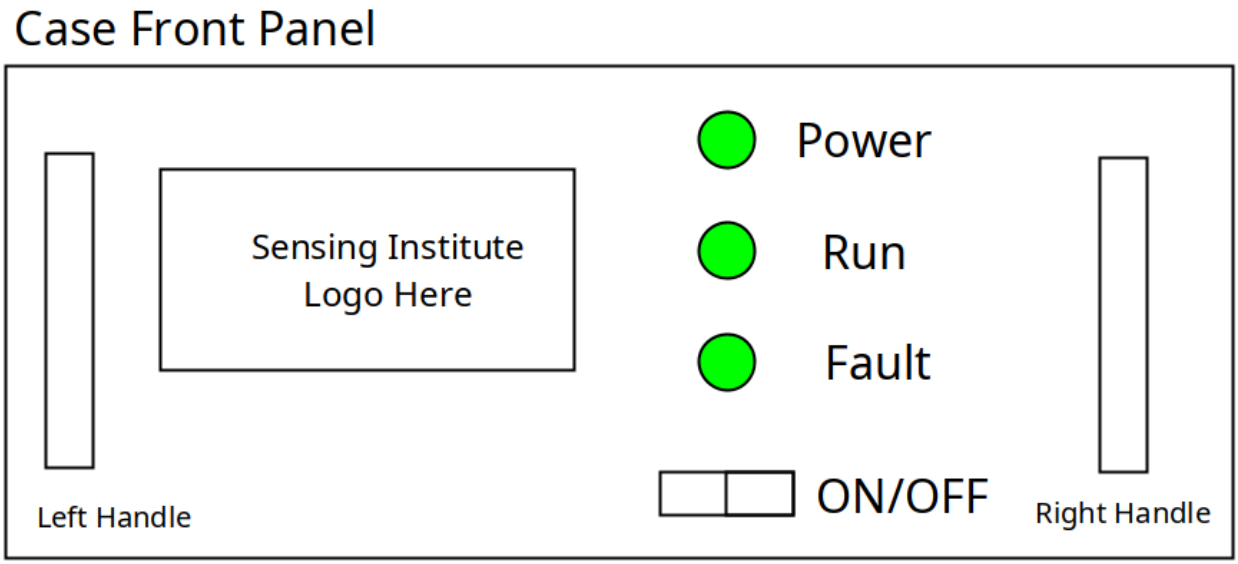
1.4 Ultrasonic Sensor Board

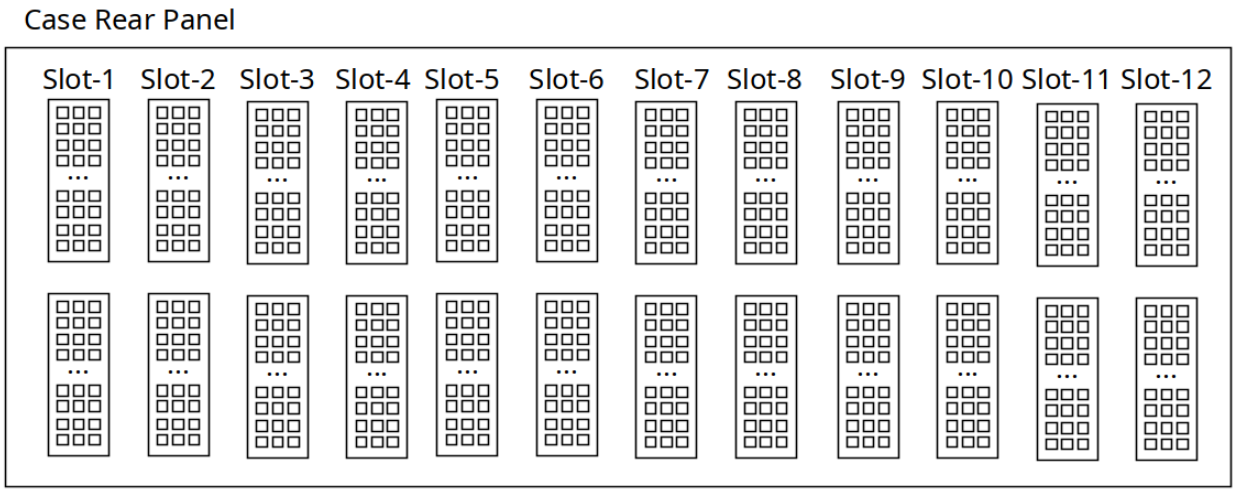


1.5 Magnetic-field Voltage Sensor Board



2. 4U Rack mount Case



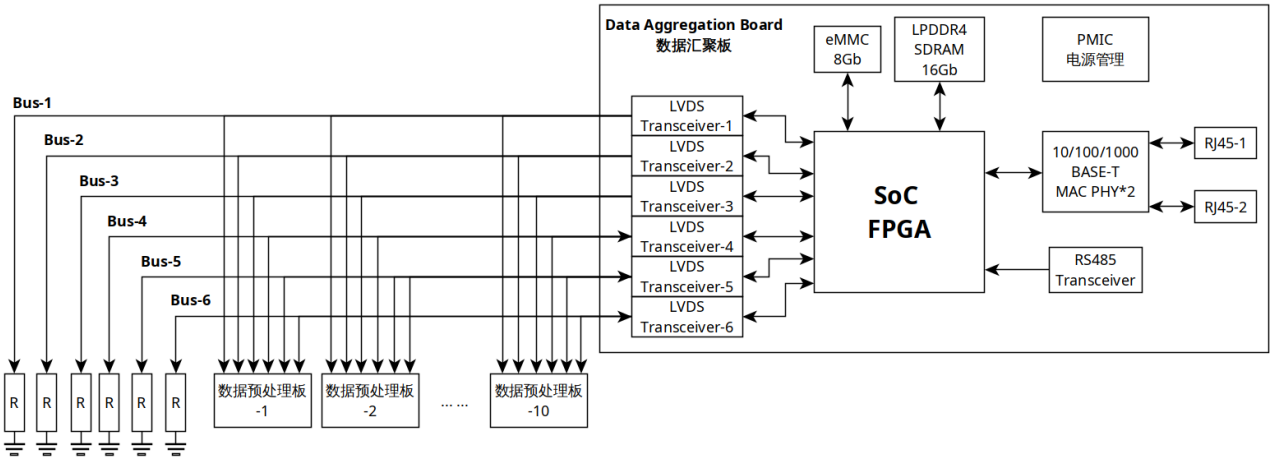


The above block diagram shows briefly the front view of case front panel. Two handles are located at left and right. We design 3 LEDs to indicate system working status. The 1st LED labeled Power indicate the whole system gets power supply and the main power rail turns on. The 2nd LED labeled Run is driven by Data Aggregation Board to show the working status by flashing it in different frequency. And Data Aggregation Board also drive the 3rd LED to flash in case of fault occurs. There's also a switch used to turn on or turn off the Power Supply Unit. The three LEDs and switch are located on a tiny PCB that is installed on front panel with screws. An external wires cable connects the tiny board and DAB.

For the rear panel, there are 12 slots available for plugging in different types of board. Attention here, PSU and DAB have fixed location, please plug in correct slots. The DPPB board has no fixed ID, it reads a unique ID once it's plugged in slot randomly.

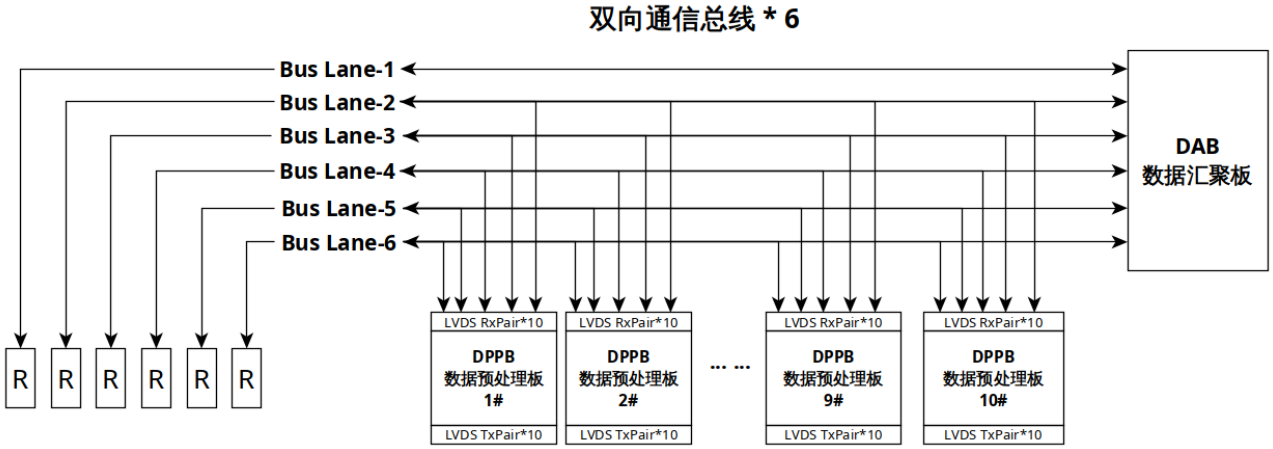
3. Data Aggregation Board

Following figure shows the brief architecture of DAB board. The main controller we use is Microchip PolarFire SoC FPGA, model type is MPFS250T-ECVG484EES. We expand an LPDDR4 SDRAM with memory size 16Gb onboard, the MAC PHY chip VSC8662 has two built-in MAC layers to support two RJ45 sockets for 10/100/1000Mbps Ethernet, an eMMC chip with memory size 8Gb is used for MSS subsystem. We also design 10 LEDs to indicate the status of respective channel. Six independent high speed LVDS buses, bidirectional transceiver, each channel supports up to 10 signals. With this feature, DAB can broadcast data to all DPPBs and recall data from each DPPB.



3.1 Bus Lane Overview

There are six bus lanes on board. They support bidirectional communication, but only work in half-duplex mode. The direction can be configured by software to suit different application needs. Each lane contains 10 differential signals, CS, CLK and D0~D7. All data are synchronized to CLK.



3.2 Bus Lane Configuration

From hardware design view, all bus lanes are bidirectional. Each lane is half-duplex, it only can be used as transmit or receive at the same time. For special applications that the requirement of uploading bandwidth is higher than downloading, users can configure five bus lanes as uploading, one bus lane as downloading. When the downloading finishes, the bus lane also can be switched to uploading. Here are some possible configurations.

3.2.1 Downloading(1) and Uploading(5)

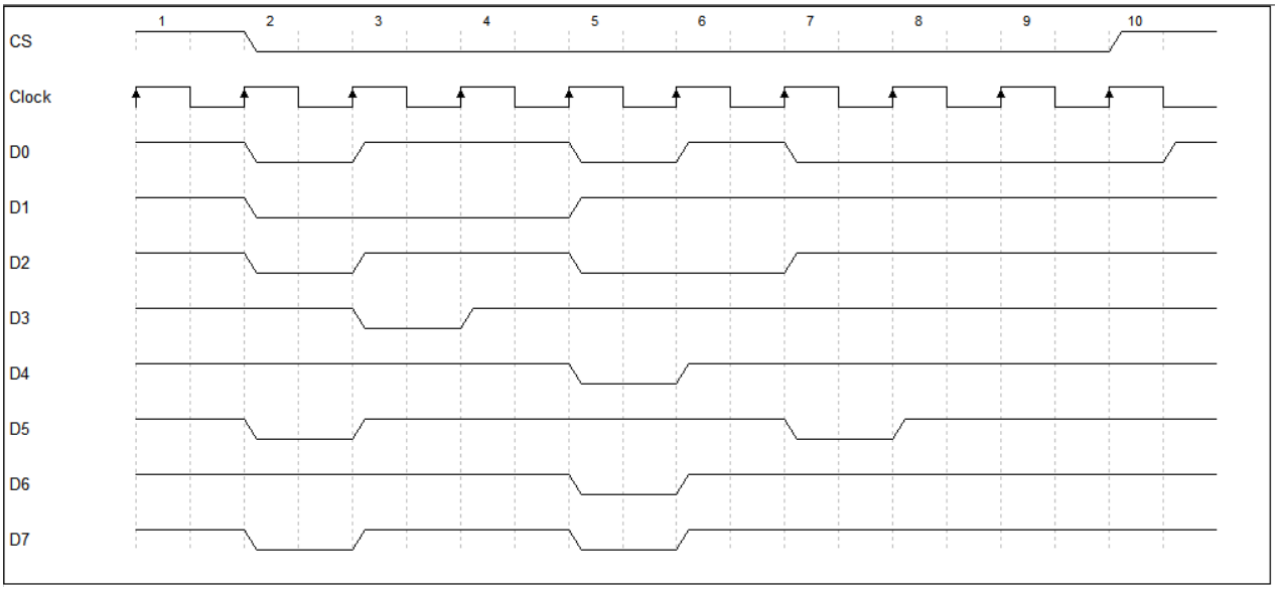
Direction	Bus Lane	Data Flow	DAB	DPPB	Communication
Downloading	Bus Lane-1	DAB → All DPPB	Tx	Rx	Broadcast or Point to Point
Uploading	Bus Lane-2	DPPB(1/6/11) → DAB	Rx	Tx	Poll each device sequentially
	Bus Lane-3	DPPB(2/7/12) → DAB	Rx	Tx	Poll each device sequentially
	Bus Lane-4	DPPB(3/8) → DAB	Rx	Tx	Poll each device sequentially
	Bus Lane-5	DPPB(4/9) → DAB	Rx	Tx	Poll each device sequentially
	Bus-Lane-6	DPPB(5/10) → DAB	Rx	Tx	Poll each device sequentially

3.2.2 Downloading Work Principle

Downloading Bus Lane can work in SDR or DDR mode. In SDR mode, each clock period it carries 8-bits. In DDR mode, each clock period it carries 16-bits. During download period, DAB transmit data, all DPPBs that connected on download bus can receive data simultaneously. Since each DPPB has its own unique address, it can recognize whether the data on Downloading Bus Lane belongs to it or not.

There are two types of address on protocol layer, Broadcast Address and Device Address. If DAB sends data with broadcast address, all DPPBs could receive and process. But if DAB sends data with a specific device address, only the corresponded DPPB could take action, others stay idle.

DAB sends data at rising edge of clock, DPPB latches data in at falling edge of clock. CS remains low during the single progress, CS pulls high to ends single transferring.



3.2.3 Uploading Work Principle

The Uploading Bus Lane is a synchronous and time-shared bus. In above configuration, three DPPBs use it to upload data, so how to prevent the bus arbitration is a critical problem. In this design, we intend to use Request/Response communication mechanism which is also well-known as Master/Slave. DAB plays the master role, it issues command over Downloading Bus. On Downloading Bus, Only DAB is the master, all DPPBs are slaves. Once master sends command, all slaves could receive command simultaneously. All slaves receive commands and compare the address field contained in command to itself unique ID, if they're matched, the addressed slave takes action. If not matched, abandon this command and be ready to receive next command.

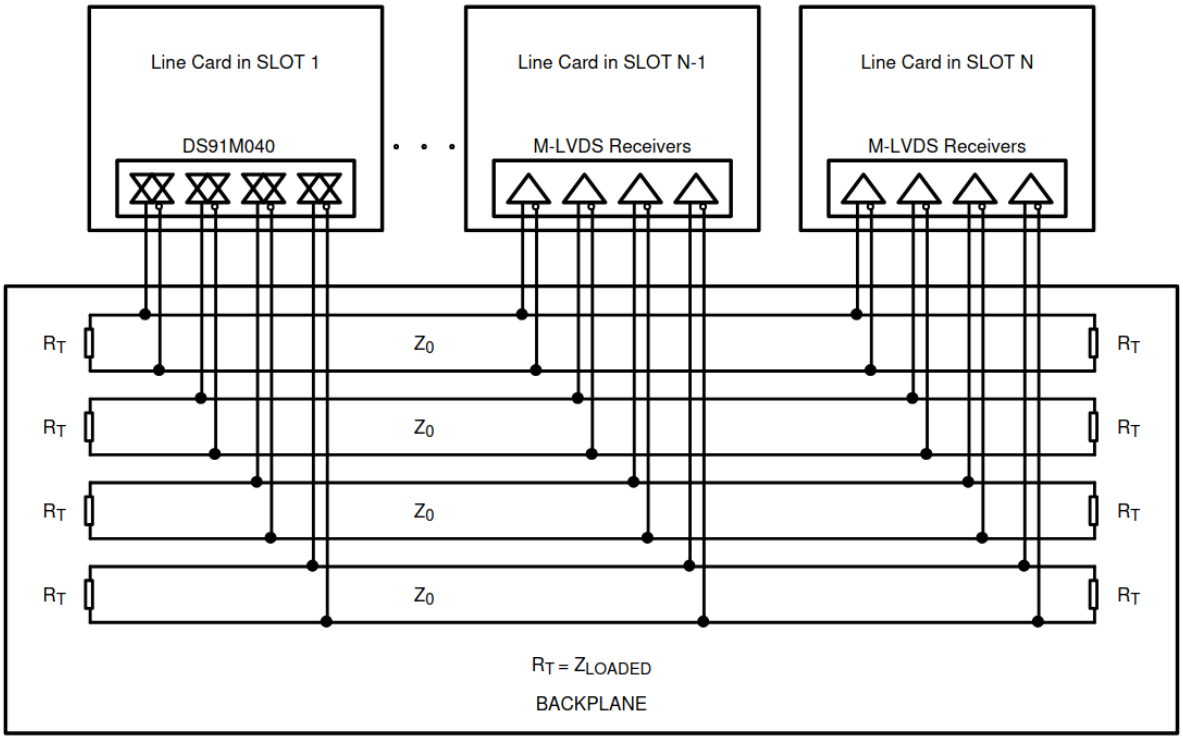
Since the uploading bus is multiple nodes shared, DAB uses polling mechanism to request data from each DPPB. Normally, the addressed DPPB responses commands and uploads data, it uploads a fixed series bytes to mark the end. DAB receives and recognizes the end mark, then poll next DPPB. In some applications, sensing data are not needed to be pre-processed, Sensor board transmits data to DPPB directly. Therefore, the FPGA located on DPPB board can be bypassed to reduce latency and complication.

DAB also have timeout mechanism to prevent abnormal circumstances, likely DPPB does not work well, or it's missed. This prevents DAB enters a dead-waiting state.

3.3 LVDS Transceiver

In our design, we use DS91M040 LVDS Transceiver. The DS91M040 is a quad Multipoint LVDS transceiver designed for driving/receiving clock or data signals to/from to four multipoint networks. A single channel is a half-duplex transceiver that accepts LVTTL/LVCMOS signals at the driver inputs and converts them to differential M-LVDS signal levels. The receiver inputs accept low voltage differential signals (LVDS, BLVDS, M-LVDS, LVPECL and CML) and covert them to 3V LVCMOS signals.

The DS91M040 supports up to 125MHz, maximum date rate is 250Mbps in DDR mode. Its differential output voltage magnitude is between 480mV and 650mV at the condition of load 50-ohms and 5pF.



3.4 Bandwidth Consideration

DAB must have performance to handle 12 input channels concurrently. In this design, we assume the date rate of each channel is up to 10Mbps. If all channels data come simultaneously, the input date rate will be 120Mbps, DAB must receive all data and store in LPDDR4 SDRAM temporarily. The capacity is 16Gbits, adequate for data buffering. After FPGA logic writes all data to SDRAM, it notifies RISC-V to transfer data out via Ethernet.

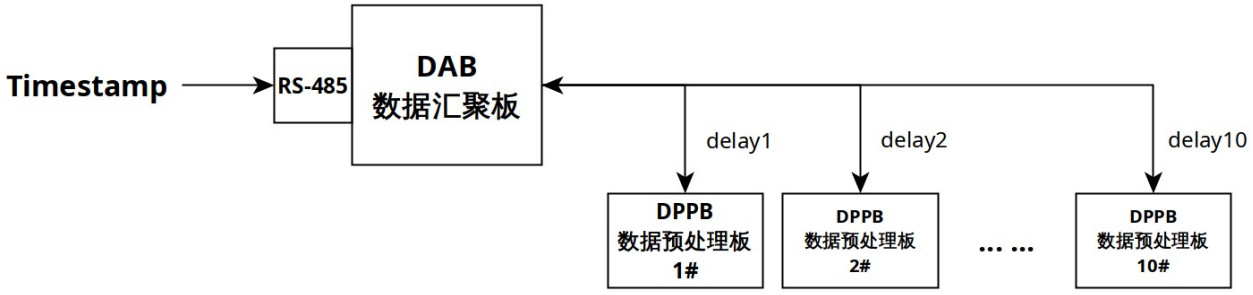
Since all data have been processed on DPPB boards, the stress suffered on DAB declined. In order to double the bandwidth, the bus lanes can work in DDR mode. Following table shows the comparison of Six Bus Lanes bandwidth working in different mode.

Bus	Work Mode	Clock (MHz)	Data width (bits)	Bandwidth (Mbps)
Bus Lane	SDR	10	8	80
		20	8	160
		25	8	200
	DDR	10	8	160
		20	8	320
		25	8	400

3.5 Time Synchronization

The time synchronization mechanism is designed to ensure accurate and consistent timekeeping across all distributed nodes in this system. This mechanism will enable precise coordination, logging and event sequencing for nodes that require time accuracy.

DAB works as the master node, all DPPBs works as slave nodes. Master node receives timestamps from RS-485 interface, then broadcast timestamps to all slave nodes, slave nodes calculate delay and adjust their clock accordingly. This achieves precise time synchronization across all slave nodes. Support for PTP(Precision Time Protocol), NTP(Network Time Protocol), and GNSS-based synchronization. On board, FPGA or micro-controller for time stamping and synchronization management. Each board has a high stability oscillator to minimize synchronization drift and latency.



3.6 Power Rails Consumption

Following table lists power rails requirement of key components in this system, involves the main hybrid SoC, LPDDR4 SDRAM, SGMII network interface, eMMC and LVDS transceivers. After merged, 3.3V 2.5V 1.8V 1.2V 1.1V are needed. It's better to use a Power Management IC that supports five power rails rather than several discrete chips. A PMIC is a great choice for reducing board space and improve efficiency.

No.	Component	Power Rails Requirement	Power Consumption
1	FPGA MPFS250T	3.3V 2.5V 1.8V 1.1V	To be continued...
2	LPDDR4	1.8V 1.1V	0.5 Watts
3	Ethernet PHY VSC8662	3.3V 1.2V	1.0 Watts
4	eMMC	3.3V 1.8V	0.66 Watts
5	LVDS Transceiver	3.3V	1.482 Watts

3.6.1 PolarFire SoC FPGA

Static Power Consumption and Dynamic Power Consumption.

To be continued….

3.6.2 LPDDR4

Table 5: LPDDR4 I_{DD} Specifications under 3733 Mb/s – Single Die

V_{DD2}, V_{DDQ} = 1.06–1.17V; V_{DD1} = 1.70–1.95V

Parameter	Supply	T_C/3733 Mb/s			Unit	Note
		95°C	105°C	125°C		
I_{DD01}	V_{DD1}	3.7	3.7	4.4	mA	
I_{DD02}	V_{DD2}	52.0	52.0	54.0		
I_{DD0Q}	V_{DDQ}	0.75	0.75	0.75		
I_{DD2P1}	V_{DD1}	1.2	1.2	2.8	mA	
I_{DD2P2}	V_{DD2}	3.6	3.6	4.0		
I_{DD2PQ}	V_{DDQ}	0.75	0.75	0.75		
I_{DD2PS1}	V_{DD1}	1.2	1.2	2.8	mA	
I_{DD2PS2}	V_{DD2}	3.6	3.6	4.0		
I_{DD2PSQ}	V_{DDQ}	0.75	0.75	0.75		
I_{DD2N1}	V_{DD1}	1.4	1.4	3.2	mA	
I_{DD2N2}	V_{DD2}	34.0	34.0	35.0		
I_{DD2NQ}	V_{DDQ}	0.75	0.75	0.75		
I_{DD2NS1}	V_{DD1}	1.4	1.4	3.2	mA	
I_{DD2NS2}	V_{DD2}	28.0	28.0	29.0		
I_{DD2NSQ}	V_{DDQ}	0.75	0.75	0.75		
I_{DD3P1}	V_{DD1}	1.2	1.2	3.0	mA	
I_{DD3P2}	V_{DD2}	16.0	16.0	16.0		
I_{DD3PQ}	V_{DDQ}	0.75	0.75	0.75		
I_{DD3PS1}	V_{DD1}	1.2	1.2	3.0	mA	
I_{DD3PS2}	V_{DD2}	16.0	16.0	16.0		

I_{DD3PSQ}	V_{DDQ}	0.75	0.75	0.75		
I_{DD3N1}	V_{DD1}	1.7	1.7	3.4	mA	
I_{DD3N2}	V_{DD2}	38.0	38.0	40.0		
I_{DD3NQ}	V_{DDQ}	0.75	0.75	0.75		
I_{DD3NS1}	V_{DD1}	1.7	1.7	3.4	mA	
I_{DD3NS2}	V_{DD2}	36.0	36.0	38.0		
I_{DD3NSQ}	V_{DDQ}	0.75	0.75	0.75		
I_{DD4R1}	V_{DD1}	3.4	3.4	4.5	mA	2, 3
I_{DD4R2}	V_{DD2}	320	320	340		
I_{DD4RQ}	V_{DDQ}	62.6	62.6	62.6		
I_{DD4W1}	V_{DD1}	2.2	2.2	2.9	mA	3
I_{DD4W2}	V_{DD2}	270	270	280		
I_{DD4WQ}	V_{DDQ}	0.75	0.75	0.75		

Table 5: LPDDR4 I_{DD} Specifications under 3733 Mb/s – Single Die (Continued)

V_{DD2}, V_{DDQ} = 1.06–1.17V; V_{DD1} = 1.70–1.95V

Parameter	Supply	T_C/3733 Mb/s			Unit	Note
		95°C	105°C	125°C		
I_{DD51}	V_{DD1}	14.0	14.0	14.0	mA	
I_{DD52}	V_{DD2}	120	120	130		
I_{DD5Q}	V_{DDQ}	0.75	0.75	0.75		
I_{DD5AB1}	V_{DD1}	1.9	1.9	3.7	mA	
I_{DD5AB2}	V_{DD2}	36.0	36.0	38.0		
I_{DD5ABQ}	V_{DDQ}	0.75	0.75	0.75		
I_{DD5PB1}	V_{DD1}	1.9	1.9	3.7	mA	
I_{DD5PB2}	V_{DD2}	36.0	36.0	38.0		
I_{DD5PBQ}	V_{DDQ}	0.75	0.75	0.75		

I_{DD} Specifications

I_{DD} values are for the entire operating voltage range, and all of them are for the entire standard temperature range.

Table 188: I_{DD} Specification Parameters and Operating Conditions

LPDDR4: V_{DD2}, V_{DDQ} = 1.06–1.17V; V_{DD1} = 1.70–1.95V

LPDDR4X: V_{DD2}= 1.06–1.17V; V_{DDQ} = 0.57–0.65V; V_{DD1} = 1.70–1.95V

Parameter/Condition	Symbol	Power Supply	Notes
Operating one bank active-precharge current: ^{t}CK = ^{t}CK (MIN); ^{t}RC = ^{t}RC (MIN); CKE is HIGH; CS is LOW between valid commands; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	I_{DD01} 4.4mA	V_{DD1} 1.8V	
	I_{DD02} 54mA	V_{DD2} 1.1V	
	I_{DD0Q} 0.75mA	V_{DDQ} 1.1V	2
Idle power-down standby current: ^{t}CK = ^{t}CK (MIN); CKE is LOW; CS is LOW; All banks are idle; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	I_{DD2P1} 2.8mA	V_{DD1} 1.8V	
	I_{DD2P2} 4.0mA	V_{DD2} 1.1V	
	I_{DD2PQ} 0.75mA	V_{DDQ} 1.1V	2
Idle power-down standby current with clock stop: CK_t = LOW, CK_c = HIGH; CKE is LOW; CS is LOW; All banks are idle; CA bus inputs are stable; Data bus inputs are stable; ODT is disabled	I_{DD2PS1}	V_{DD1}	
	I_{DD2PS2}	V_{DD2}	
	I_{DD2PSQ}	V_{DDQ}	2
Idle non-power-down standby current: ^{t}CK = ^{t}CK (MIN); CKE is HIGH; CS is LOW; All banks are idle; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	I_{DD2N1}	V_{DD1}	
	I_{DD2N2}	V_{DD2}	
	I_{DD2NQ}	V_{DDQ}	2
Idle non-power-down standby current with clock stopped: CK_t = LOW; CK_c = HIGH; CKE is HIGH; CS is LOW; All banks are idle; CA bus inputs are stable; Data bus inputs are stable; ODT is disabled	I_{DD2NS1}	V_{DD1}	
	I_{DD2NS2}	V_{DD2}	
	I_{DD2NSQ}	V_{DDQ}	2
Active power-down standby current: ^{t}CK = ^{t}CK (MIN); CKE is LOW; CS is LOW; One bank is active; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	I_{DD3P1}	V_{DD1}	
	I_{DD3P2}	V_{DD2}	
	I_{DD3PQ}	V_{DDQ}	2
Active power-down standby current with clock stop: CK_t = LOW, CK_c = HIGH; CKE is LOW; CS is LOW; One bank is active; CA bus inputs are stable; Data bus inputs are stable; ODT is disabled	I_{DD3PS1}	V_{DD1}	
	I_{DD3PS2}	V_{DD2}	
	I_{DD3PSQ}	V_{DDQ}	3
Active non-power-down standby current: ^{t}CK = ^{t}CK (MIN); CKE is HIGH; CS is LOW; One bank is active; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	I_{DD3N1}	V_{DD1}	
	I_{DD3N2}	V_{DD2}	
	I_{DD3NQ}	V_{DDQ}	3
Active non-power-down standby current with clock stopped: CK_t = LOW, CK_c = HIGH; CKE is HIGH; CS is LOW; One bank is active; CA bus inputs are stable; Data bus inputs are stable; ODT is disabled	I_{DD3NS1}	V_{DD1}	
	I_{DD3NS2}	V_{DD2}	
	I_{DD3NSQ}	V_{DDQ}	3
Operating burst READ current: ^{t}CK = ^{t}CK (MIN); CS is LOW between valid commands; One bank is active; BL = 16 or 32; RL = RL (MIN); CA bus inputs are switching; 50% data change each burst transfer; ODT is disabled	I_{DD4R1} 4.5mA	V_{DD1} 1.8V	
	I_{DD4R2} 340mA	V_{DD2} 1.1V	
	I_{DD4RQ} 62.6mA	V_{DDQ} 1.1V	4

4.4*1.8+54*1.1+0.75*1.1
68.14

68.14mW

2.8*1.1+4.0*1.1+0.75*1.1
8.30

8.3mW

4.5*1.8+340*1.1+62.6*1.1
450.96

450.96mW

Table 188: I_{DD} Specification Parameters and Operating Conditions (Continued)

LPDDR4: V_{DD2}, V_{DDQ} = 1.06–1.17V; V_{DD1} = 1.70–1.95V

LPDDR4X: V_{DD2}= 1.06–1.17V; V_{DDQ} = 0.57–0.65V; V_{DD1} = 1.70–1.95V

Parameter/Condition	Symbol	Power Supply	Notes
Operating burst WRITE current: ^{t}CK = ^{t}CK (MIN); CS is LOW between valid commands; One bank is active; BL = 16 or 32; WL = WL (MIN); CA bus inputs are switching; 50% data change each burst transfer; ODT is disabled	I_{DD4W1} 2.9mA	V_{DD1} 1.8V	
	I_{DD4W2} 280mA	V_{DD2} 1.1V	
	I_{DD4WQ} 0.75mA	V_{DDQ} 1.1V	3
All-bank REFRESH burst current: ^{t}CK = ^{t}CK (MIN); CKE is HIGH between valid commands; ^{t}RC = $^{t}RFCab$ (MIN); Burst refresh; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	I_{DD51}	V_{DD1}	
	I_{DD52}	V_{DD2}	
	I_{DD5Q}	V_{DDQ}	3
All-bank REFRESH average current: ^{t}CK = ^{t}CK (MIN); CKE is HIGH between valid commands; ^{t}RC = $^{t}REFI$; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	I_{DD5AB1}	V_{DD1}	
	I_{DD5AB2}	V_{DD2}	
	I_{DD5ABQ}	V_{DDQ}	3
Per-bank REFRESH average current: ^{t}CK = ^{t}CK (MIN); CKE is HIGH between valid commands; ^{t}RC = $^{t}REFI/8$; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	I_{DD5PB1}	V_{DD1}	
	I_{DD5PB2}	V_{DD2}	
	I_{DD5PBQ}	V_{DDQ}	3
Power-down self refresh current: CK_t = LOW, CK_c = HIGH; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable; Maximum 1x self refresh rate; ODT is disabled	I_{DD61}	V_{DD1}	5, 6
	I_{DD62}	V_{DD2}	5, 6
	I_{DD6Q}	V_{DDQ}	3, 5, 6

2.9*1.8+280*1.1+0.75*1.1
314.04

314.04mW

3.6.3 Ethernet PHY

5.2 Current Consumption

There are three sets of current consumption values:

- Typical current consumption
- Current consumption in SerDes/SGMII to 1000BASE-X mode
- Current consumption in SerDes/SGMII to 100BASE-FX mode or SerDes pass-through mode

The typical current consumption values are based on nominal voltages with all ports operating at 1000BASE-T speeds with full-duplex enabled and a 64-bit random data pattern at 100% utilization.

Table 74 • **Typical Current Consumption**

Parameter	Symbol	Typical	Maximum	Unit
Worst-case power consumption	P_D		3.19	W
Current with V_{DDIO} at 1.8 V	I_{VDDIO}	1		mA
Current with V_{DDIO} at 2.5 V	I_{VDDIO}	1		mA
Current with V_{DDIO} at 3.3 V	I_{VDDIO}	1		mA
Current with V_{DD33} at 3.3 V	I_{VDD33}	228		mA
Current with V_{DD12} at 1.2 V	I_{VDD12}	390		mA
Current with V_{DD12A} at 1.2 V	I_{VDD12A}	224		mA

If all ports are running in SerDes/SGMII to 1000BASE-X mode, the current consumption values are shown in the following table.

Table 75 • **Current Consumption in SerDes/SGMII to 1000BASE-X Mode**

Parameter	Symbol	Typical	Maximum	Unit
Worst-case power consumption(1)	P_D		0.57	W
Current with V_{DDIO} at 1.8 V	I_{VDDIO}	1		mA
Current with V_{DDIO} at 2.5 V	I_{VDDIO}	1		mA
Current with V_{DDIO} at 3.3 V	I_{VDDIO}	1		mA
Current with V_{DD33} at 3.3 V	I_{VDD33}	38		mA
Current with V_{DD12} at 1.2 V	I_{VDD12}	58		mA
Current with V_{DD12A} at 1.2V	I_{VDD12A}	238		mA

1. Worst-case power only applies if the 1000BASE-X media operating mode is set by CMODE configuration. When any Cat5 media operating mode is selected using CMODE, the worst-case power consumption in the preceding table applies. For information, see Table 74, page 69.

If all ports are running in SerDes/SGMII to 100BASE-FX mode or SerDes pass-through mode, the current consumption values are as shown in the following table.

Table 76 • **Consumption in SerDes/SGMII to 100BASE-FX or SerDes Pass-Through Mode**

Parameter	Symbol	Typical	Maximum	Unit
Worst-case power consumption(1)	P_D		0.59	W
Current with V_{DDIO} at 1.8 V	I_{VDDIO}	1		mA
Current with V_{DDIO} at 2.5 V	I_{VDDIO}	1		mA
Current with V_{DDIO} at 3.3 V	I_{VDDIO}	1		mA
Current with V_{DD33}	I_{VDD33}	34		mA
Current with V_{DD12}	I_{VDD12}	49		mA
Current with V_{DD12A}	I_{VDD12A}	202		mA

1. Worst-case power only applies if the 100BASE-FX media operating mode is set by CMODE configuration. When any Cat5 media operating mode is selected using CMODE, the worst-case power consumption listed earlier in this section applies. For information, see Table 74, page 69.

3.6.4 eMMC Memory Chip

3.1. Typical Power Requirements

Table 3 - iNAND Power Requirements (Ta=25°C@3.3V)

		Max Value	Measurement
Auto Sleep mode		350	uA
Sleep (CMD5)		200 (Max) 130 (Typical)	uA
Read	Default Speed	100	mA
	High-Speed	200	mA
Write	Default Speed	100	mA
	High-Speed	200	mA
VCC (ripple: max, 60mV peak-to-peak) 2.7 V – 3.6 V			

200MA * 3.3V = 0.66 Watts

3.6.5 LVDS Transceiver

SUPPLY CURRENT (V_{CC})						
I_{CCD}	Driver Supply Current	R_L = 50Ω, DE = H, $\overline{RE}$ = H		67	75	mA
I_{CCZ}	TRI-STATE Supply Current	DE = L, $\overline{RE}$ = H		22	26	mA
I_{CCR}	Receiver Supply Current	DE = L, $\overline{RE}$ = L		32	38	mA
I_{CCPD}	Power Down Supply Current	MDE = L		3	5	mA

From this table, we know DS91M040 consumes 75mA maximum in driving mode, 38mA maximum in receiving mode. Since there are 6 transceivers on board, we assume they all work in driving mode, so the total current consumed is calculated by following equation,

75mA * 3.3V * 6 = 1.482 Watts.

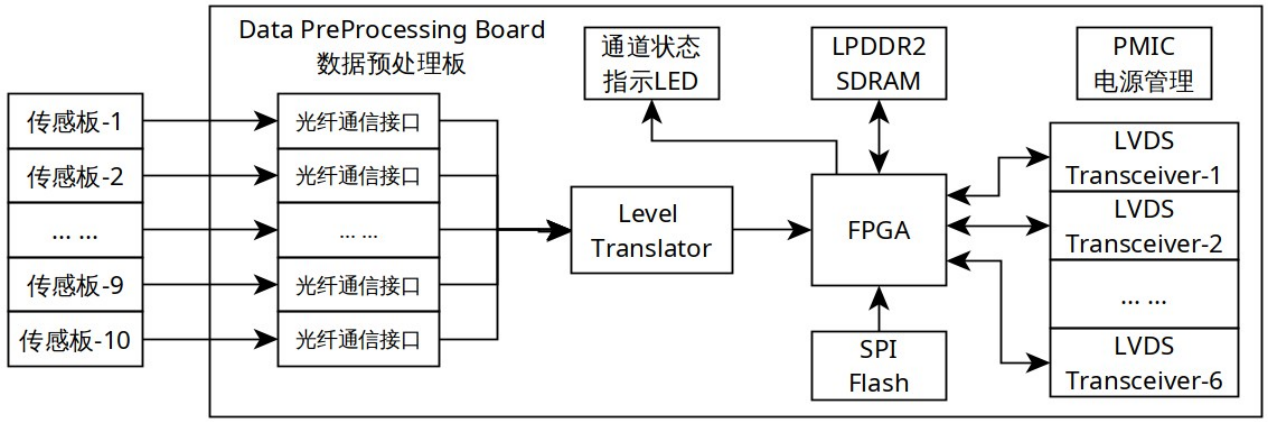
3.7 Status Indication

DAB should indicate the status of all DPPBs through LED Flashing. The FPGA Logic should control the flashing frequency of LED to assist with maintenance. Likely, slow flashing, fast flashing, continuous on and off.

Limited by mechanical front panel size, only 12 LEDs are provided on board. Each LED indicates respective channel status by different flashing combination.

Comprehensive LED status will be defined in software design document.

4. DPPB Architecture



4.1 DPPB Requirement

DPPB must support up to 10 input channels. The maximum date rate is 10Mbps. And considering all channels data may come simultaneously. So the bandwidth of output port should be 10Mbps*10=100Mbps at least. If DPPB can't transfer data out in date rate of 100Mbps, data will lose. The bandwidth between input port and output port are not match. A better way to solve this problem is adding an external DDR SDRAM.

Following table shows single frame data size of different image sensors. This table offers a reference approximately, it determines the capacity of DDR SDRAM that we need. Bigger resolution, more capacity. Here one frame of Visible-Light Image, the data size is 75Mbits. For 10 channels, we need 75Mbits*10=750Mbits. So strongly recommend to place a 2Gb DDR SDRAM on board.

/	Visible-Light Image	Infrared Image		Ultraviolet Image
Resolution	2560*1920	640*512	256*192	1280*1024
Data Depth	16-bits	14-bits	14-bits	8-bits
Total (in bits)	75Mbits	5Mbits	0.75Mbits	20Mbits
Total (in Bytes)	9.37MBytes	0.62MBytes	0.09MBytes	2.5MBytes

4.2 Bandwidth Consideration

The ideal situation is the output bandwidth matched to input bandwidth, so no data will lose. In this design, each DPPB has 10 input channels data stream and the date rate is up to 10Mbps, that means if all channels data come in simultaneously, the input bandwidth will be 100Mbps. But we only have one output port with 20MHz in SDR mode. Even if we operate it in DDR mode, the bandwidth is 40Mbps. Not matched perfectly.

So pre-processing data is essential to reduce bandwidth cost. With less data size, DPPB can transfer data out in time.

4.3 Channel Status Indication

DPPB should indicate the status of all channels through LED Flashing. The FPGA Logic will control the flashing frequency of LED to assist with maintenance. Likely, slow flashing, fast flashing, continuous on and off.

Comprehensive LED status will be defined in software design document.

5. Power Supply Unit

The PSU board supplies power to all electric components. It accepts 180VAC~230VAC input, converts AC to DC, outputs 12V power rails with 25A maximum current. The PSU board has over-current protection, thermal protection and smart fan controller.

5.1 Key Parameters

Following table shows key parameters of power supply unit.

Item	Parameter	Memo
Topology	AC/DC	
Input Voltage Range	180VAC~230VAC 50Hz	
Output Voltage	12V	
Output Current (Max.)	25A	
Ripple and Noise		
Power Efficiency	90%	
Load Regulation		
Line Regulation		
Overload Protection	Support	Alarm
Thermal Protection	Support	Alarm and shutdown when overheated.

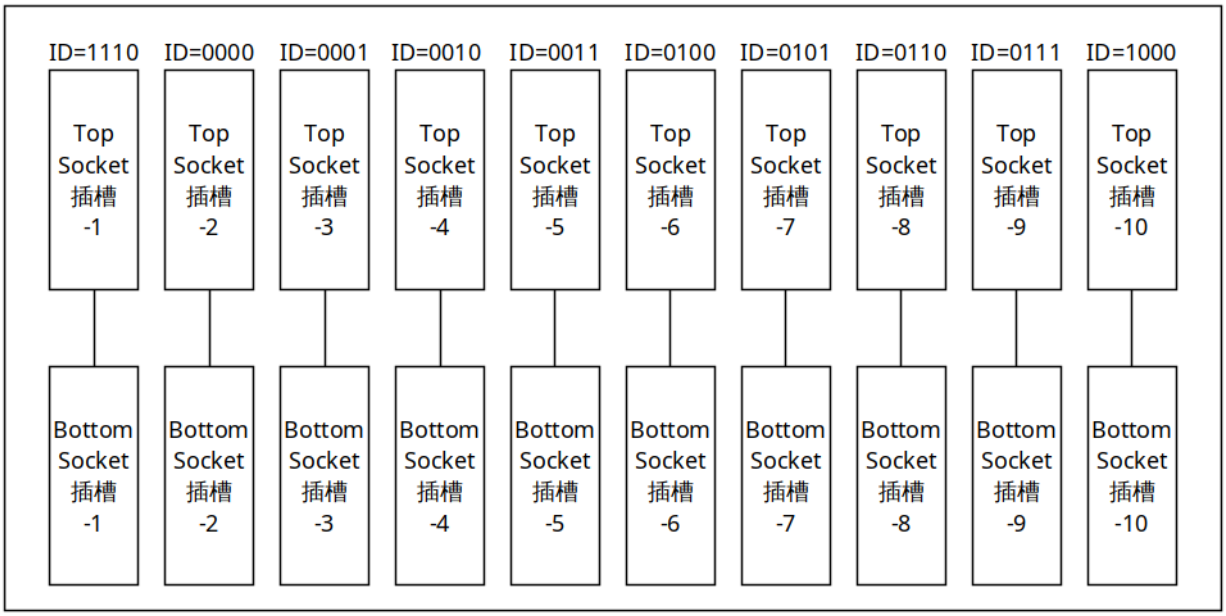
5.2 Power Consumption Estimation

Following table shows the power supply requirement of each board. This is the maximum estimation, at least 20% safety margins are acceptable.

Board Name	Power Consumption	
DAB	6 Watts	12V/0.5A
DPPB		

6. Backplane Board

Backplane Board 背板



6.1 Connector Pin Assignment

The aim of BPB is to distribute power supply and route bus signals. And also LVDS terminate resistors on board. In this design, BPB has 14 sockets totally, each socket integrates two connectors, the top connector is used to distribute power supply and LVDS pairs. For the bottom connector, it routes ID allocation and LVDS pairs. Following table shows pin assignment.

There are 60 LVDS pairs totally in the back plane board. LVDS transceivers we use only work in half-duplex mode, software layers determine the direction. The minimum swing is only 460mV, PCB layout must be very careful to reduce impact from impedance match.

Normally, 30% safety margins are acceptable, for the connector we’re using, current capacity of each pin is 200mA approximately. We assign 9 pins to distribute 12V voltage, the maximum current capacity is calculated by the equation, 200mA*9=1.8A. The numbers of GND pin is twice times of 12V.

Current carrying capacity of PCB vias are described as below for a reference guideline.

Via Diameter	Max Current
0.15mm	0.5A
0.2mm	0.7A
0.3mm	1A
0.4mm	1.5A
0.5mm	2A
0.6mm	2.5A
0.8mm	4A
1.0mm	6A

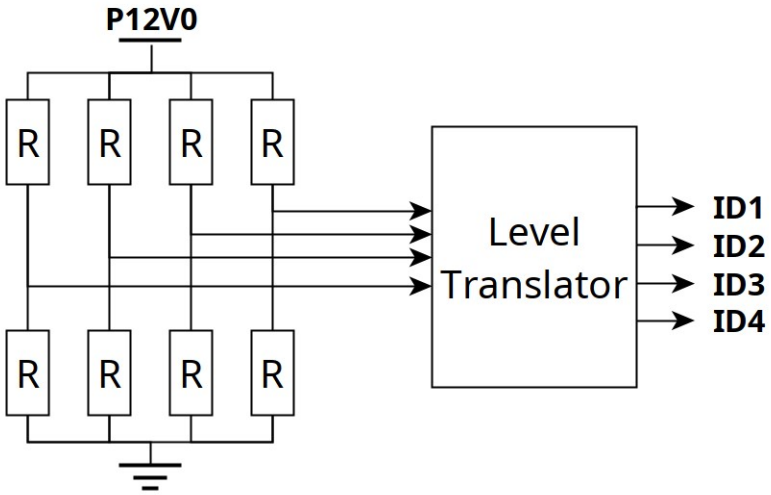
No.	Top Connector – 3x32P						Bottom Connector – 3x32P					
1	A1	12V	A2	12V	A3	12V	A1	GND	A2	GND	A3	GND
2	B1	12V	B2	12V	B3	12V	B1	TR25_P	B2	TR13_P	B3	TR1_P
3	C1	12V	C2	12V	C3	12V	C1	TR25_N	C2	TR13_N	C3	TR1_N
4	D1	GND	D2	GND	D3	GND	D1	TR26_P	D2	TR14_P	D3	TR2_P
5	E1	GND	E2	GND	E3	GND	E1	TR26_N	E2	TR14_N	E3	TR2_N
6	F1	GND	F2	GND	F3	GND	F1	GND	F2	GND	F3	GND
7	G1	GND	G2	GND	G3	GND	G1	TR27_P	G2	TR15_P	G3	TR3_P
8	H1	GND	H2	GND	H3	GND	H1	TR27_N	H2	TR15_N	H3	TR3_N
9	I1	GND	I2	GND	I3	GND	I1	TR28_P	I2	TR16_P	I3	TR4_P
10	J1	TR53_P	J2	TR45_P	J3	TR37_P	J1	TR28_N	J2	TR16_N	J3	TR4_N
11	K1	TR53_N	K2	TR45_N	K3	TR37_N	K1	GND	K2	GND	K3	GND
12	L1	GND	L2	GND	L3	GND	L1	TR29_P	L2	TR17_P	L3	TR5_P
13	M1	TR54_P	M2	TR46_P	M3	TR38_P	M1	TR29_N	M2	TR17_N	M3	TR5_N
14	N1	TR54_N	N2	TR46_N	N3	TR38_N	N1	TR30_P	N2	TR18_P	N3	TR6_P
15	O1	GND	O2	GND	O3	GND	O1	TR30_N	O2	TR18_N	O3	TR6_N
16	P1	TR55_P	P2	TR47_P	P3	TR39_P	P1	GND	P2	GND	P3	GND
17	Q1	TR55_N	Q2	TR47_N	Q3	TR39_N	Q1	TR31_P	Q2	TR19_P	Q3	TR7_P
18	R1	GND	R2	GND	R3	GND	R1	TR31_N	R2	TR19_N	R3	TR7_N
19	S1	TR56_P	S2	TR48_P	S3	TR40_P	S1	TR32_P	S2	TR20_P	S3	TR8_P
20	T1	TR56_N	T2	TR48_N	T3	TR40_N	T1	TR32_N	T2	TR20_N	T3	TR8_N
21	U1	GND	U2	GND	U3	GND	U1	GND	U2	GND	U3	GND
22	V1	TR57_P	V2	TR49_P	V3	TR41_P	V1	TR33_P	V2	TR21_P	V3	TR9_P
23	W1	TR57_N	W2	TR49_N	W3	TR41_N	W1	TR33_N	W2	TR21_N	W3	TR9_N
24	X1	GND	X2	GND	X3	GND	X1	TR34_P	X2	TR22_P	X3	TR10_P
25	Y1	TR58_P	Y2	TR50_P	Y3	TR42_P	Y1	TR34_N	Y2	TR22_N	Y3	TR10_N
26	Z1	TR58_N	Z2	TR50_N	Z3	TR42_N	Z1	GND	Z2	GND	Z3	GND
27	AA1	GND	AA2	GND	AA1	GND	AA1	TR35_P	AA2	TR23_P	AA1	TR11_P
28	AB1	TR59_P	AB2	TR51_P	AB1	TR43_P	AB1	TR35_N	AB2	TR23_N	AB1	TR11_N
29	AC1	TR59_N	AC2	TR51_N	AC1	TR43_N	AC1	TR36_P	AC2	TR24_P	AC1	TR12_P
30	AD1	GND	AD2	GND	AD1	GND	AD1	TR36_N	AD2	TR24_N	AD1	TR12_N
31	AE1	TR60_P	AE2	TR52_P	AE1	TR44_P	AE1	GND	AE2	GND	AE1	ID1
32	AF1	TR60_N	AF2	TR52_N	AF1	TR44_N	AF1	ID2	AF2	ID3	AF1	ID4

6.2 ID Allocation

Since we have 12 DPPB boards connected in parallel, so there's ID allocation circuit designed special for DPPB boards recognition. Initially, DPPBs has no fixed ID. Once it's plugged into BPB, BPB allocates a unique ID to it. Later, DPPB read this ID to transfer data and response command from DAB. DAB distinguishes each DPPB by unique ID accurately.

Here, 4 bits can address 2^4=16 boards, adequate for our needs. ID[4:1]=1111 is the broadcast ID, it means that the command will be send to all DPPBs.

Place these circuit beside each socket on In some applications, TU data are not needed to be pre-processed, TU transmits data to DPPB directly. Therefore, the FPGA located on DPPB board can be bypassed to reduce latency and complication. BPB, and soldering respective resistors in fabrication. Duplicated IDs could cause confusion and data collision.



背板ID分配

ID[4:1]	Board
0000	DAB数据汇聚板
0001	DPPB数据预处理板-1
0010	DPPB数据预处理板-2
0011	DPPB数据预处理板-3
0100	DPPB数据预处理板-4
0101	DPPB数据预处理板-5
0110	DPPB数据预处理板-6
0111	DPPB数据预处理板-7
1000	DPPB数据预处理板-8
1001	DPPB数据预处理板B-9
1010	DPPB数据预处理板-10
1011	Reserved
1100	Reserved
1101	Reserved
1110	PSU供电单元
1111	Broadcast广播地址

********** The End of File **********