PoF (Power Over Fiber)

Tiny Dual Camera Surveillance System

Design Document

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| --- | --- | --- |
| VERSION | DATE | MEMO |
| 0.0.1 | DEC 5, 2024 | Initial Version. |
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# 1. Purpose

This technical design document helps all engineers and managers involved in this project to understand the system working principle completely. And analyze all conditions before taking action. All potential technological risks will be revealed and give out elegant solutions.

# 2. Entire System Description

## 2.1 Entire System Block Diagram

Considering this system will be installed in Ultra High Voltage Valve, no AC 220V power supply available. In reality, we use PoF (Power Over Fiber) Technology. Power transmission and data communication use only one single core optical fiber. We split the whole system into two separate PCB boards. The benefits of module design is that we can reuse the mature and stable parts in different projects. In this design, two parts are involved, one is named to Energy Harvest Board, another is named to Image Capture Board. The Energy Harvest Board is used to convert light energy to electricity, it charges a farad capacitor, when farad capacitor is charged full, it triggers Image Capture Board. The Image Capture Board is used to capture infrared image and visible-light image from different image sensors and does some simple processing then upload data to remote client.

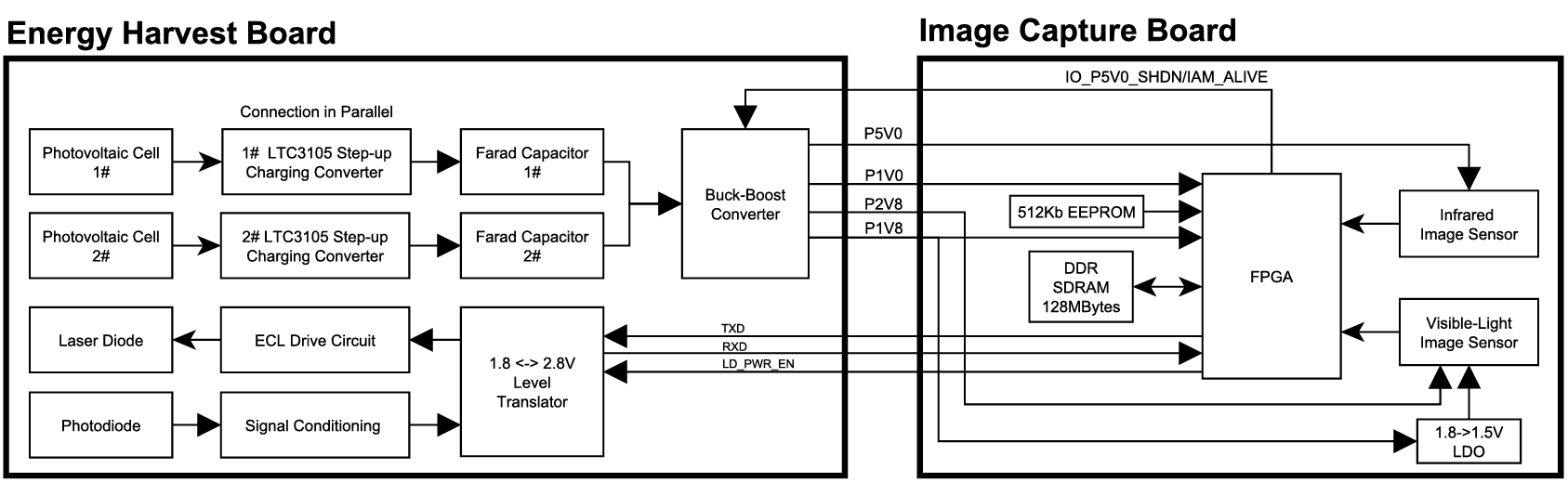


Figure 1. Entire System Block Diagram

## 2.2 Estimated Power Consumption Table

|  |  |  |
| --- | --- | --- |
| Items | Rated Power | Memo |
| Infrared  Image Sensor | <=350mW | VDD=5V, Sensor+ISP |
| Visible-Light  Image Sensor | <=260mW | VCore: 1.5V, VAnalog: 2.8V  VIO: 1.8V |
| Laser diode | 2.65mW | VFD=1.23V, Vth=9.02mA, IOP=18mA |
| FPGA | 150mW | Dynamic |
| SDRAM | <=45mW | VDD=1.8V, VIO=1.8V  Read/Write @133MHz (X16) =23mA |
| Total | ≈550mW | Only Infrared Image Sensor Working  350mW+2.65mW+150mW+45mW=547.65mW |
| ≈500mW | Only Visible Light Image Sensor Working  260mW+2.65W+150mW+45mW=457.65mW |

## 2.3 Watts to Joules Calculation

The formula for calculating energy in Joules is

**E(J)=P(W)\*t(S)**

where E is the energy in Joules, P is the power in Watts and t is the time in seconds.

In our design, we limit the total power consumption within 1 Watt, continuously work within 60 seconds, so the energy needed is calculated by following equation.

**E = 1 (Watt) \* 60 (Seconds) = 60 (Joules)**

## 2.4 Farad Capacitor Storage Energy Calculation

The formula to calculate the energy stored in a farad capacitor is

**E=0.5\*C\*V^2**

where E is the energy stored in the capacitor, measured in Joules. C is the capacitance of the capacitor, measured in Farads. V is the voltage applied across the capacitor, measured in Volts.

In our design, the termination charging voltage is 4.35V, so the capacitance of the farad capacitor we need is calculated by following equation. The reason we choose 4.35V is that the default register value of MAX20361 after reset is 4.35V. We can reconfigure register value to the maximum value 4.75V through I2C interface.

**60 (Joules) = 0.5 \* C \* (4.35^2)**

**C=60/0.5/(4.35^2)=6.34(F)**

I made a comparison table below showing how much capacitance we need in different situation of Watts. The less energy we need, the smaller the farad capacitor will be.

|  |  |  |  |
| --- | --- | --- | --- |
| **Back-end Circuit Power Consumption**  **(in Milliwatts unit)** | **Continuously  Working Time (in Seconds unit)** | **Charging  Termination Voltage (in Volts unit)** | **Farad Capacitor Capacitance (in Farads unit)** |
| 1000mW | 60s | 4.35V | 6.34F |
| 800mW | 60s | 4.35V | 5F |
| 500mW | 60s | 4.35V | 3.17F |
| 500mW | 40s | 4.35V | 2.12F |
| 500mW | 30s | 4.35V | 1.59F |

# 3. Energy Harvest Board

## 3.1 Energy Harvest Board Block Diagram

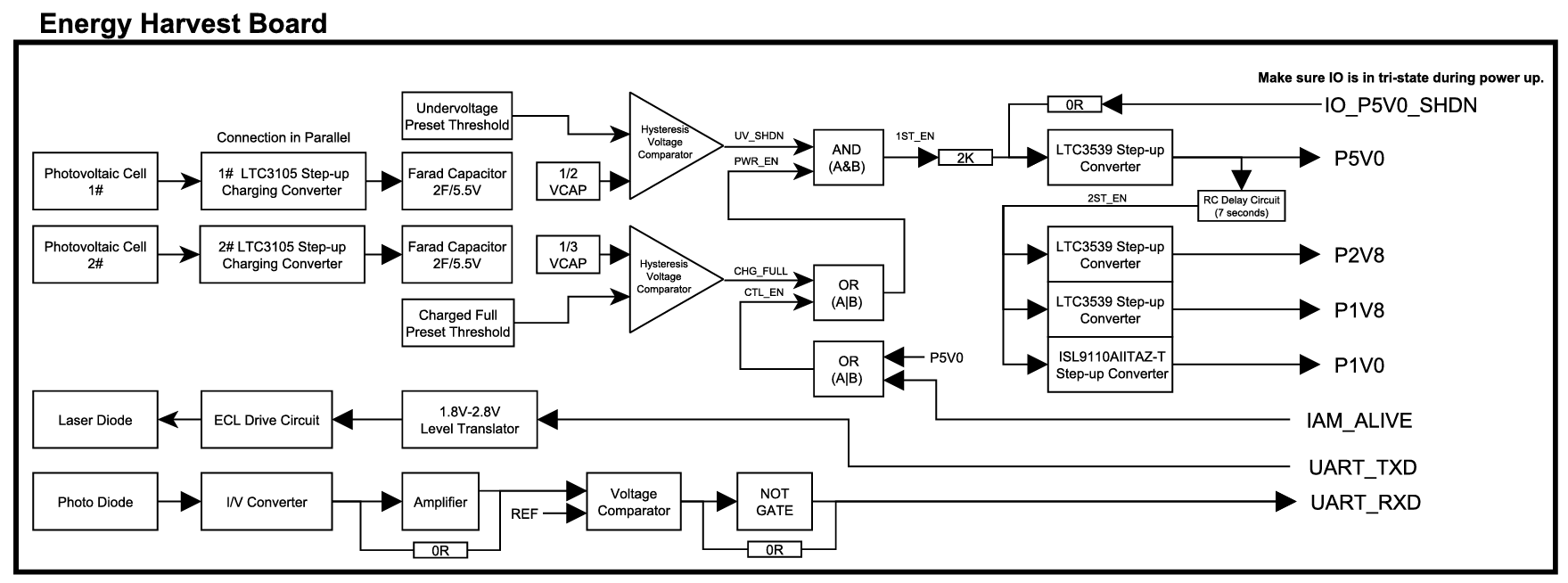


Figure 2. Energy Harvest Board Block Diagram

The main aim of this board is designed to convert light energy to electricity. We use two photovoltaic cells on board, connected in parallel to increase the total power supply capability. LTC3105 is used as a charging converter, to charge the farad capacitor. We set two threshold values, the low value is for under voltage protection, the high value is to enable LTC3539 step up converter for the first time. Three discrete components, a AND gate and two OR gates are combined for power supply logic processing.

|  |  |  |  |
| --- | --- | --- | --- |
| Harvest IC | Input Voltage Range | Output Voltage Adjust Range | Peak Current Limit/Power |
| LTC3105 | 225mV~5V | 1.6~5.25V | 0.4A@3.3V |
| MAX20361 | 225mV~2.5V | 4~4.7V | 300mW |
| SPV1040 | 300mV~5.5V | 2V~5.5V | 3W |

For the second stage, the reason we choose LTC3559 is that its minimum start-up voltage can be low to 700mV. Once it starts up, the input voltage even can drop to 500mV. I launched a survey to compare various of multiple channel PMICs on market, majority of them require a minimum input voltage above 2.0V, and they are deliberately designed for FPGA, inappropriate for our design. As the farad capacitor discharges, the voltage declines, when it drops down 50% of the charged threshold 2.5V, it reaches the minimum start-up voltage of majority chips.

The LTC3105 features a 2.2V/6mA auxiliary LDO while the main output is charging. Since we use two chips on board, in order to distribute power supply in a balance state, LDO22-1 and LDO22-2 are used simultaneously. LDO22-1 is used to power the unit gain amplifier, the 1st hysteresis voltage comparator and an AND gate. LDO22-2 is used to power the 2nd hysteresis voltage comparator and two OR gates.

## 3.2 Rated Power Versus Working Mode

The maximum rated power of single cell is 250mW, overload will cause permanent damage. For some applications which power consumption are less than 250mW, only one cell is sufficient. If power consumption exceeds 250mW but less than 500mW, two cells will be used simultaneously. Once rated power consumption of the back-end system is over 500mW, this solution cannot support it runs continuously. We use two farad capacitors on board to support it runs discontinuously and periodically. The higher power consumption of the load is, the bigger power capacity is needed.

|  |  |  |
| --- | --- | --- |
| **Power Consumption** | **How Many Photovoltaic Cells will be used** | **Working Mode** |
| P<250mW | 1 | Continuous |
| 250mW<=P<=500mW | 2 | Continuous |
| P>500mW | 2 | Periodical |

Table 1. Power Consumption Versus Working Mode

## 3.3 Start Up and Shutdown

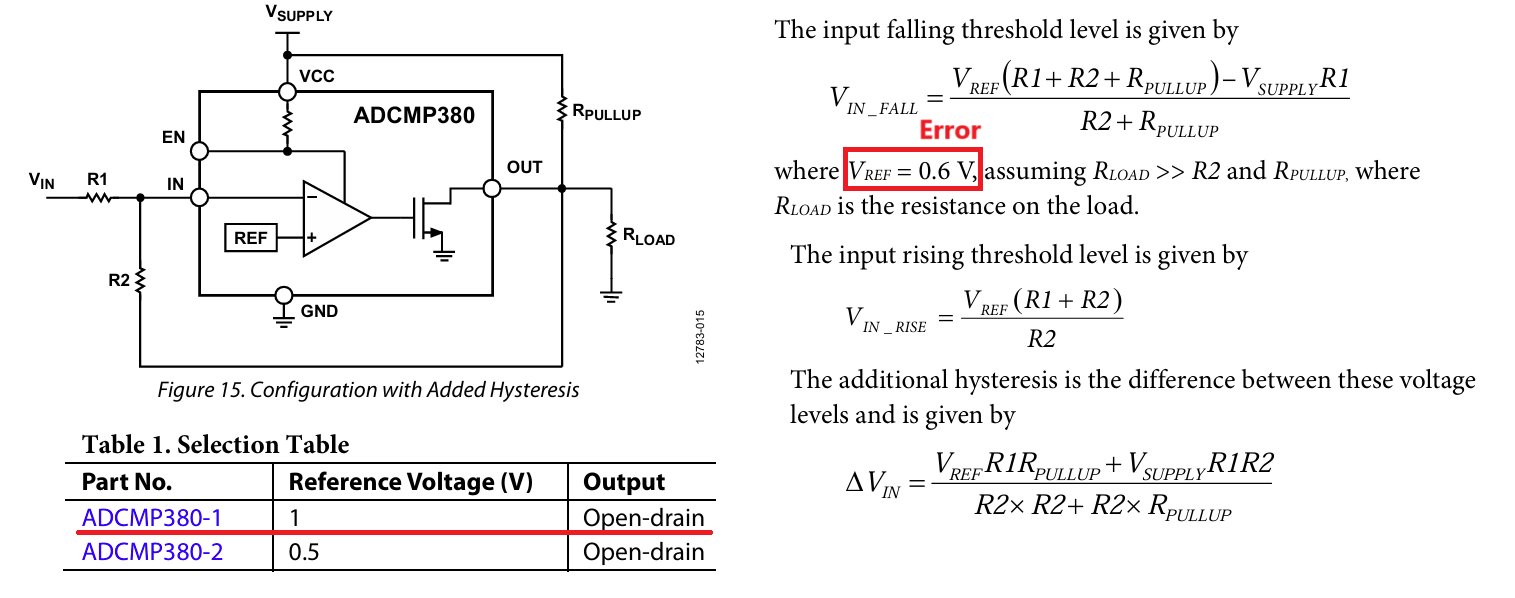
Two stages power converters are available, the 1st stage is used to charge the farad capacitor. The buck-boost converter chip we use is special chosen, it outputs 2.2V power rails in addition. We use this 2.2 power rail to supply voltage comparators and logic gates. Voltage of farad capacitor determines back-end system to run or not. If the voltage is too low, the under-voltage shutdown signal UV\_SHDN will be issued to cut off the converter. And also, if the voltage reaches the highest level, the charged full signal CHG\_FULL will be issued to enable the converter, then back-end system starts to work. Actually, along with power consuming, the voltage on farad capacitor drops down and CHG\_FULL will become invalid. In order to prevent it shuts down the converter, two additional signals P5V0 and IAM\_ALIVE are used to lock the enabled state. P5V0 plays the significant role before IAM\_ALIVE becomes valid. At this point, CHG\_FULL threshold value must be chosen carefully. It leaves adequate time before P5V0 becomes valid. Once back-end system starts up, it drives IAM\_ALIVE to HIGH to replace P5V0. Because of the OR gate in circuit, either CHG\_FULL nor CTL\_EN will keep 1ST\_EN to be HIGH to enable the converter.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Signals** | **UV\_SHDN** | **CHG\_FULL** | **P5V0** | **IAM\_ALIVE** | **1ST\_EN** |
| **Power Up** | 0 | X | X | X | 0 |
| **Charging** | 1 | 0 | X | X | 0 |
| **Charged Full** | 1 | 1 | 0 | X | 0 |
| **Image Sensor/FPGA Starts Up** | 1 | 1 | 1 | X | 1 |
| 1 | 0 | 1 | X | 1 |
| 1 | 0 | 0 | 1 | 1 |
| **FPGA**  **Commit Suicide** | 1 | 0 | 0 | 0 | 0 |

Table 1. True Table of Key Points

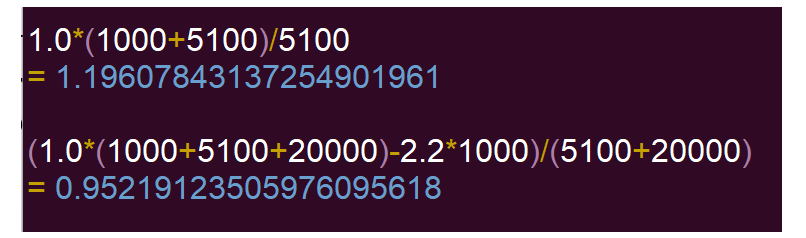
In order to keep theoretical calculation accurately, after the voltage resistor division network, we use an operating amplifier to work as an emit-follower, to increase the input impedance. Firstly, VCAP will be divided by 2, then it goes into unit gain operating amplifier for impedance match, finally the voltage comparator compares presetting threshold and VCAP/2. We use two comparators in design, one is for under voltage detection, another is for charged full detection.

The hysteresis voltage comparator for under-voltage protection is set as 1.9V for falling, 2.4V for rising. Another comparator for charged full trigger is set as 2.94V for falling, 4.59V for rising. We concentrate emphasis here, charged full threshold voltage must be less than VCAP ultimate voltage. In this design, we set charged full trigger to 4.59V, the first charging converter charges farad capacitors to 4.75V, this strategy ensures charged full trigger must be valid before farad capacitors are charged full.

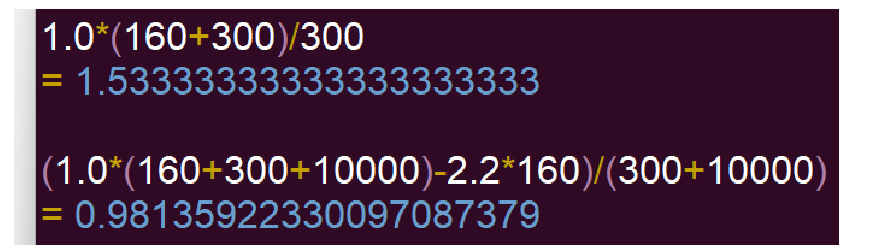


Under voltage protection strategy is to shutdown converters when the voltage of farad capacitors drops down below a specific threshold. As voltage drops down, the energy it can source declines. Attention here, Reference Voltage is 1.0V, not 0.6V !

For UV\_SHDN, we configure R1=1K, R2=5.1K, RPULLUP=20K, calculation as follows. Here Vrise=1.2V, Vfall=0.95V. Because the voltage comparator is powered by 2.2V, we add a 1/2 voltage resistor network, the realistic action voltages are Vrise=1.2V\*2=2.4V, Vfall=0.95V\*2=1.9V.



For CHG\_FULL, the combined configuration of R1=160, R2=200, RPULLUP=10K are used. Using the equation to get Vrise=1.53V, Vfall=0.98V. Because the limitation of power rail 2.2V, a 1/3 voltage resistor network is used before the signal enters the voltage comparator. The realistic action voltages are Vrise=1.53V\*3=4.59V, Vfall=0.98V\*3=2.94V.



## 3.4 RC Delay Circuit

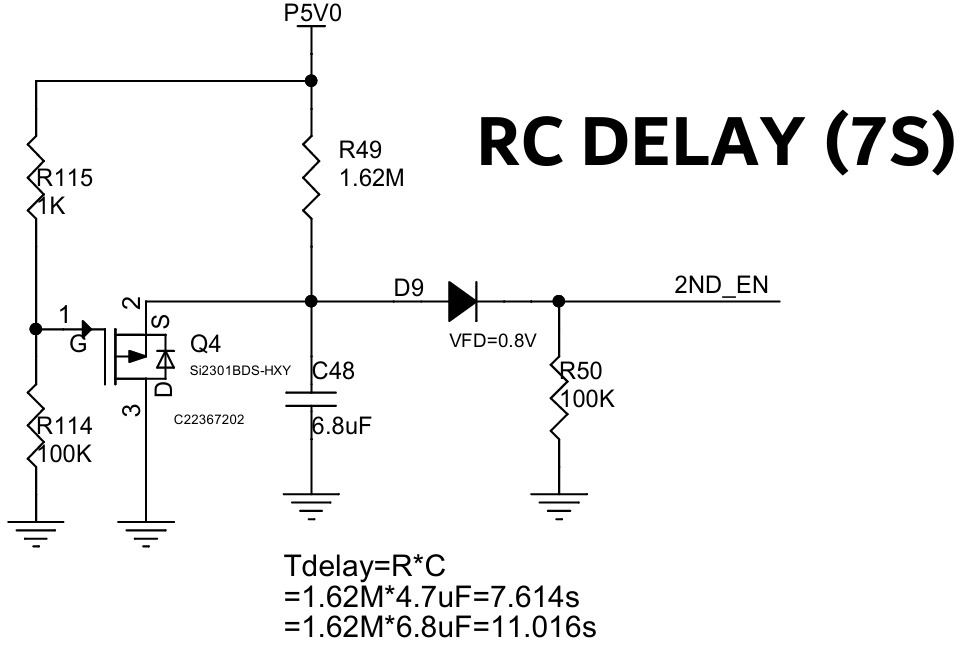
Since Infrared Image Sensor needs 7 seconds to initialize, then it outputs normal data, to minimize the power consumption, we do not start up FPGA during this stage. The 1ST\_EN (The First Enable) signal is issued by hysteresis voltage comparator and gates logic, P5V0 power rail will be established first. We design a special RC delay circuit to output 2ND\_EN (The Second Enable) after 7 seconds approximately. Schematic shows below. The diode is used to level up trigger threshold to smooth noise. The P-MOSFET is used for discharging rapidly for next time. While P5V0 is valid, VG is nearly 5V because of the series resistor network, VS is changing from 0V to 5V, P-MOSFET is OFF. When P5V0 is turned off, VG is pulled down to 0V, Vs remains a high level because of existing of the capacitor, P-MOSFET is turned on, the capacitor is discharged. For AO3401, its datasheet shows the typical VGS(th) is -0.9V, this means the capacitor can be discharged to 0.9V.

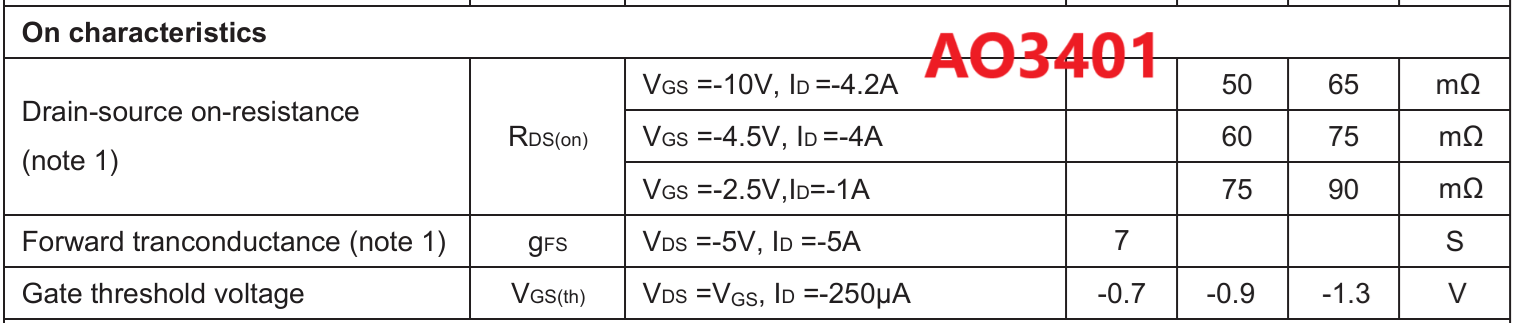
The charging and discharging rate of a series RC network is characterized by its RC time constant, which is calculated by the equation

**Tdelay=R\*C**

where Tdelay is the time constant in second, R is the resistance in OHMS, C is the capacitance in F.

|  |  |  |
| --- | --- | --- |
| Resistance | Capacitance | Time |
| 1M | 10uF | 10s |
| 2M | 4.7uF | 9.4s |
| 1.62M | 4.7uF | 7.614s |
| 1.62M | 6.8uF | 11.016s |





# 4. Image Capture Board

## 4.1 Image Capture Board Block Diagram

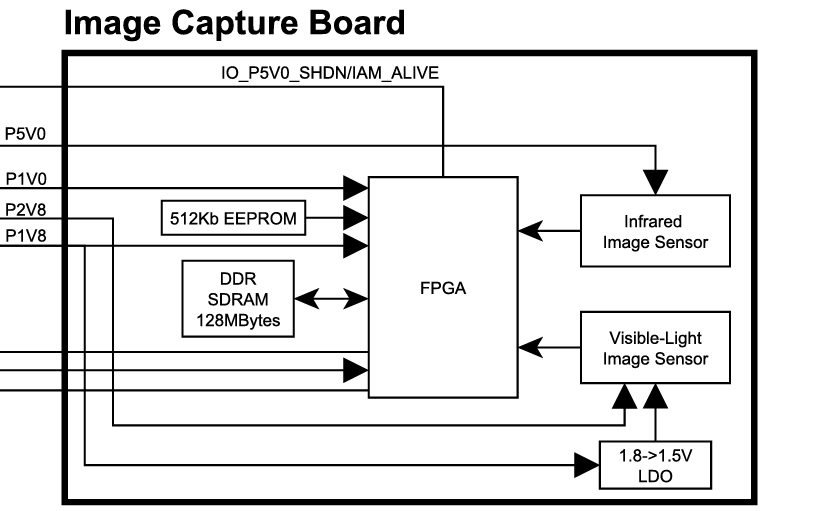


Figure 3. Image Capture Board Block Diagram

## 4.2 Start Up & Sample & Upload

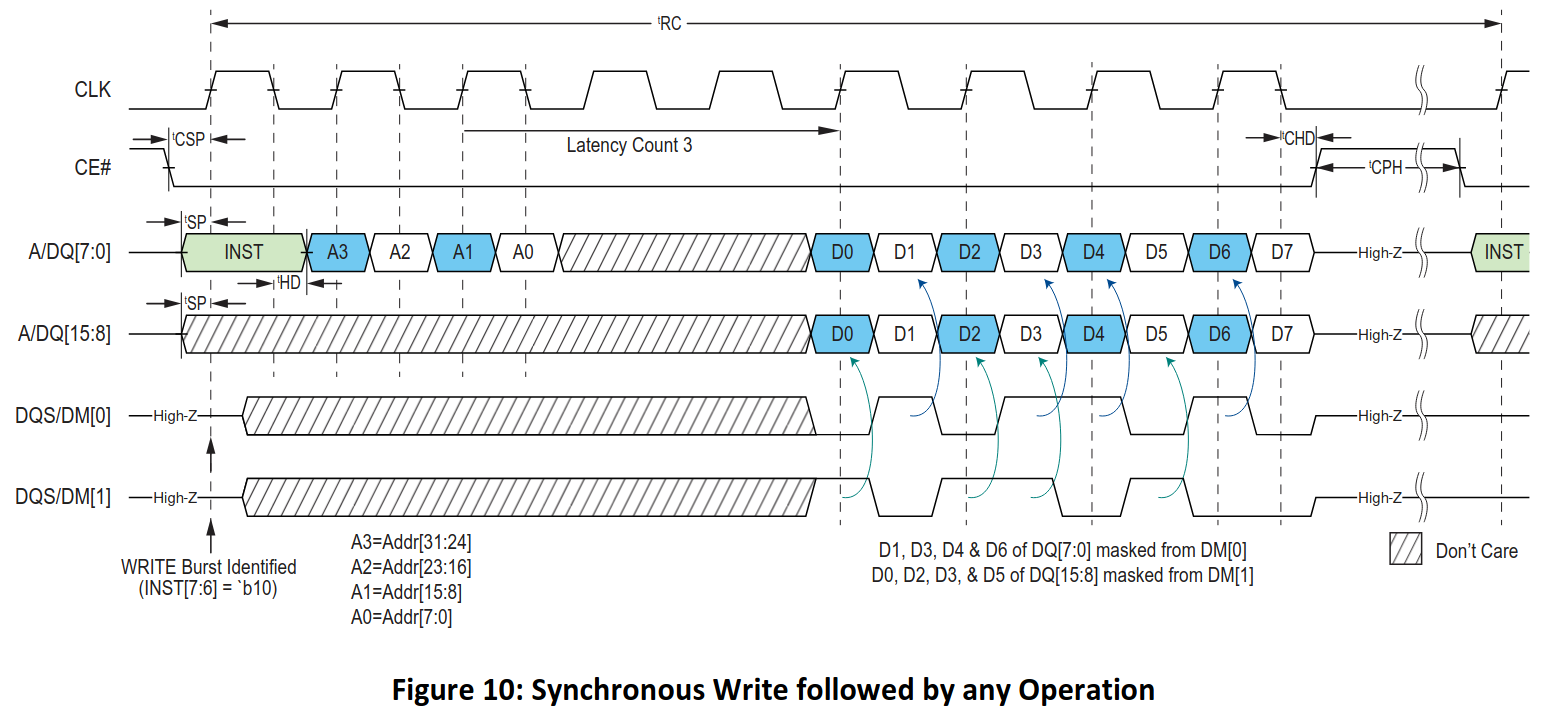
Since the infrared image sensor needs 7 seconds to initialize from cold boot, in our design, P5V0 power rail will be established first, infrared image sensor starts up immediately. Special designed RC delay circuit outputs 2ND\_EN after 7 seconds approximately, then the converters of P2V8, P1V8, P1V0 power rails start to work. This strategy is used to reduce power consumption in maximum, it means FPGA logic does not work in first 7 seconds.

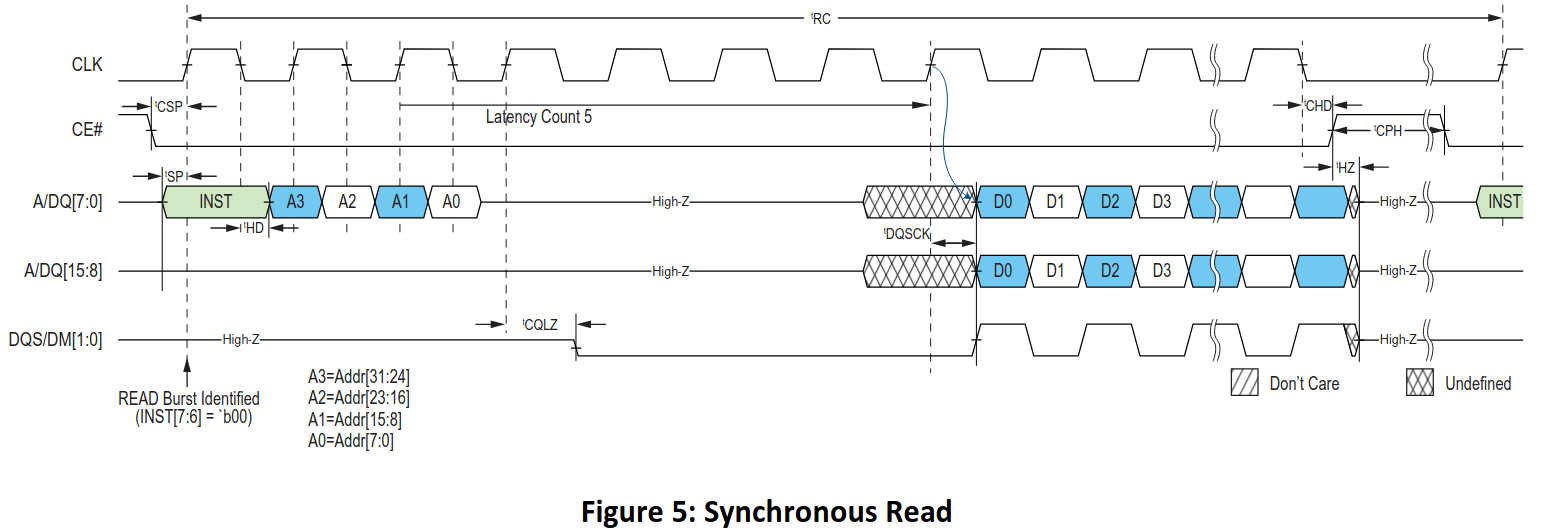
After image sensor initialization, FPGA powers up and drives IAMALIVE to HIGH. Along with the voltage on farad capacitor drops down, CHG\_FULL changes from HIGH to LOW, it becomes invalid. But at this moment, IAMALIVE is HIGH, so PWR\_EN still keeps valid. FPGA configures image sensors, read all pixel data in and write into external DDR SDRAM. In order to reduce current consumption, FPGA cuts off image sensors power supply. FPGA reads data from DDR SDRAM and transmits out via UART. Finally, FPGA commits suicide by issuing IAMALIVE to LOW. CHG\_FULL is LOW and IAMALIVE is low, causes PWR\_EN becomes LOW. Consequently, 1ST\_EN is low, Boost Converter stops. The back-end system powers off completely, it will be launched again after next charging full period.

## 4.3 SPI DDR SDRAM

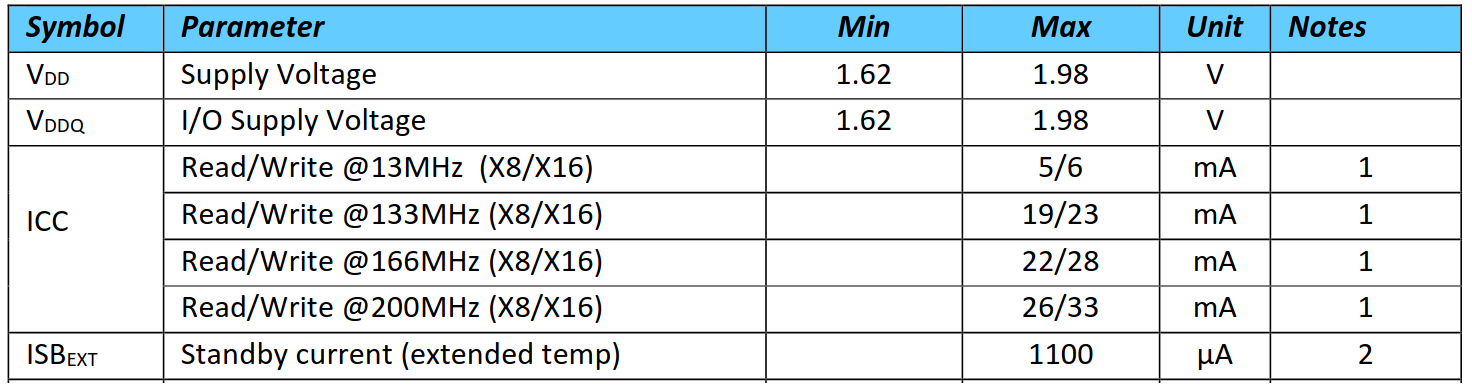
In this design, we use a DDR Octal SPI PSRAM APS25616N-OB9-BG. It has 16 data pins, can transfer two words per clock, self-refreshing, 256Mbits capacity, 32M\*8 and 16M\*16 organization mode, maximum clock frequency is 200MHz. Following table shows if it’s adequate to store one single frame image completely.

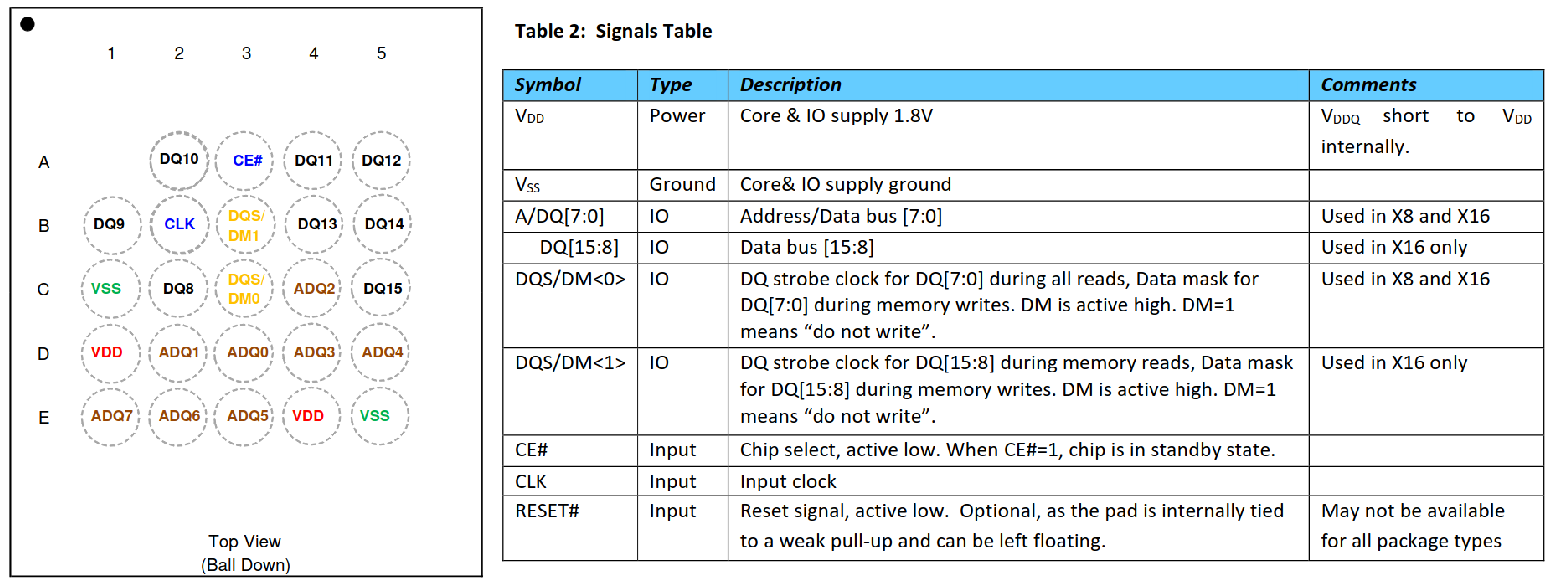
|  |  |  |  |
| --- | --- | --- | --- |
| Type | Resolution | Single Line | Total Size of One Frame |
| Infrared Image | 256\*192 | 256\*2B+256\*2B=1024Bytes | 192KBytes |
| Infrared Image | 640\*512 | 640\*2B+640\*2B=2560Bytes | 1.25MBytes |
| Visible Light Image | 2592\*1944 | 2592\*16bits=5184Bytes | 9.61MBytes |





DC Characteristics Table shows the maximum current is 23mA if it works at the frequency of 133MHz x16. The total power consumption will not exceed 23mA\*1.8V=41.4mW.



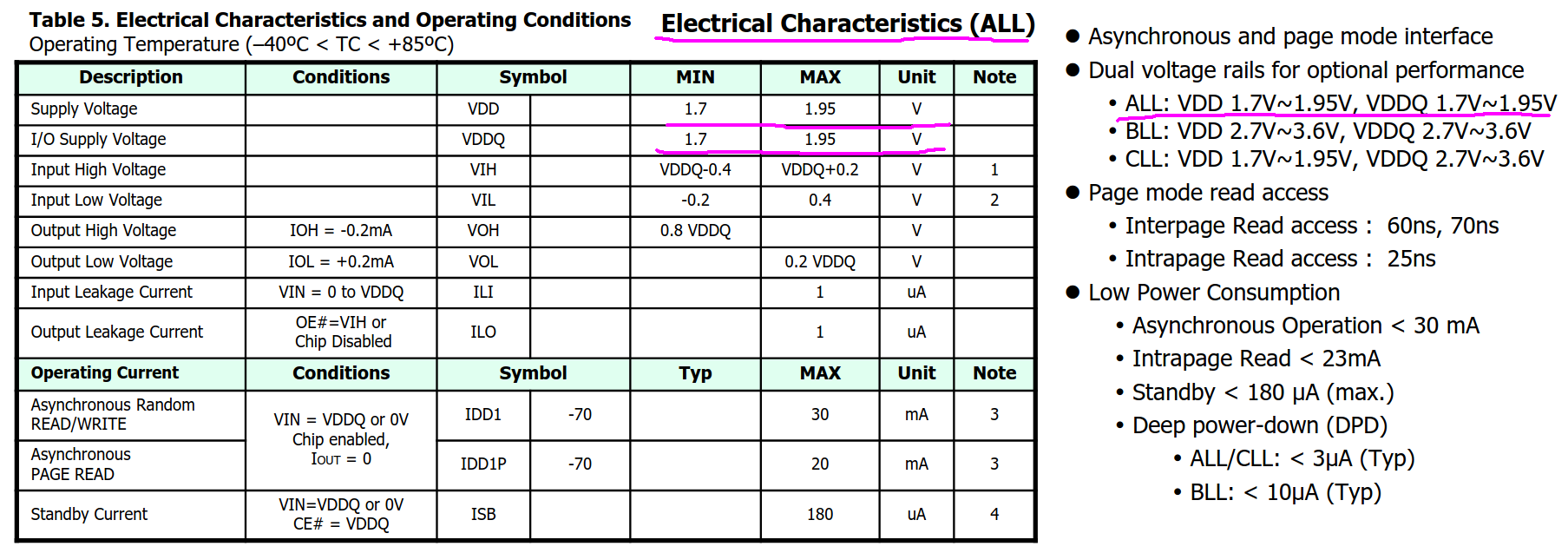


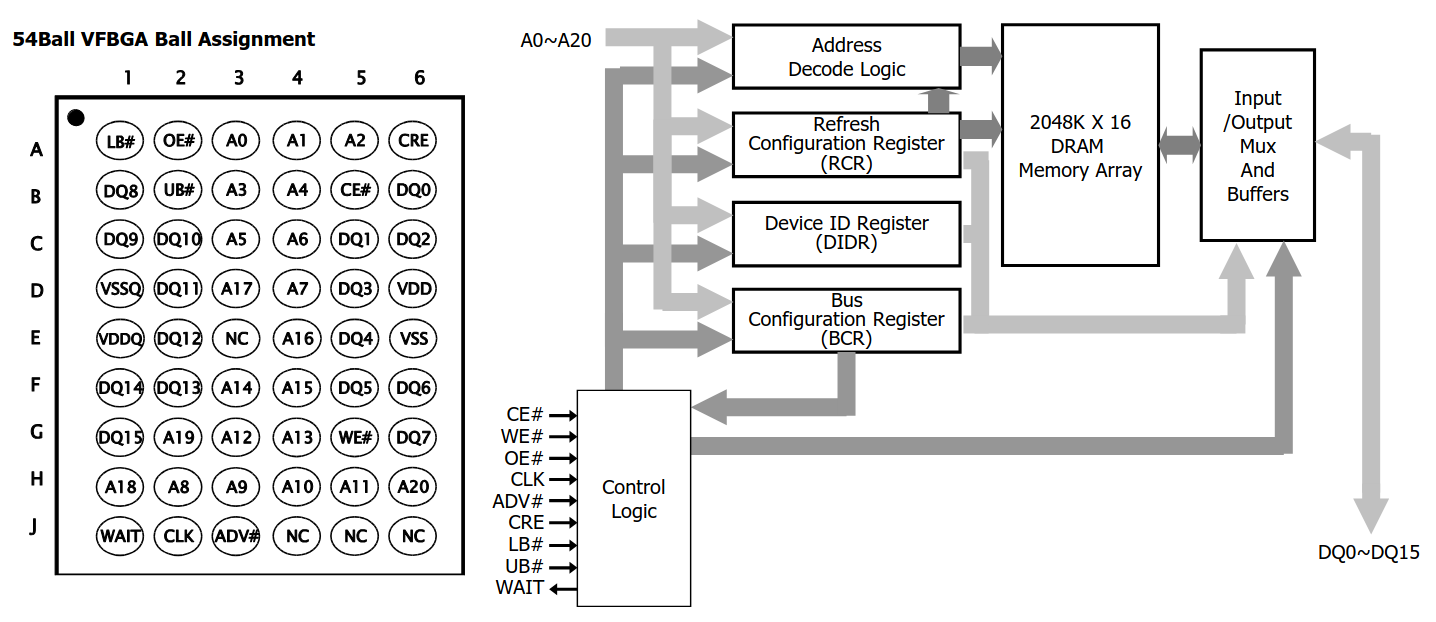
## 4.4 PSRAM Selection

The reason we choose to use Pseudo RAM is its simplification and no refresh periodically needed. SDRAM needs more power to refresh the data.

|  |  |  |  |
| --- | --- | --- | --- |
| No. | Chips |  | Price (CNY) |
| 1 | IS66WVE2M16EALL-70BLI-TR | 32Mbits |  |
| 2 | CY62167EV18LL | 16Mbits | 120.00 |
|  |  |  |  |

IS66WVE2M16EALL-70BLI-TR, 32Mbit Pseudo Static Random Access Memory, Operation Frequency up to 104MHz, Asynchronous Operation < 30 mA, Intrapage Read < 20mA, Burst operation < 45 mA (@104MHz), Operating temperature Range: Industrial -40°C~85°C, Package: 54-ball VFBGA.





## 4.5 Dynamic Power Management of Image Sensors

In order to minimize the total consumption, we use combined strategies. Power supply of image sensors is managed dynamically, sensors power on when needed, power off after working.

For the infrared image sensor, FPGA drives IO\_P5V0\_EN pin to shutdown P5V0 converter.

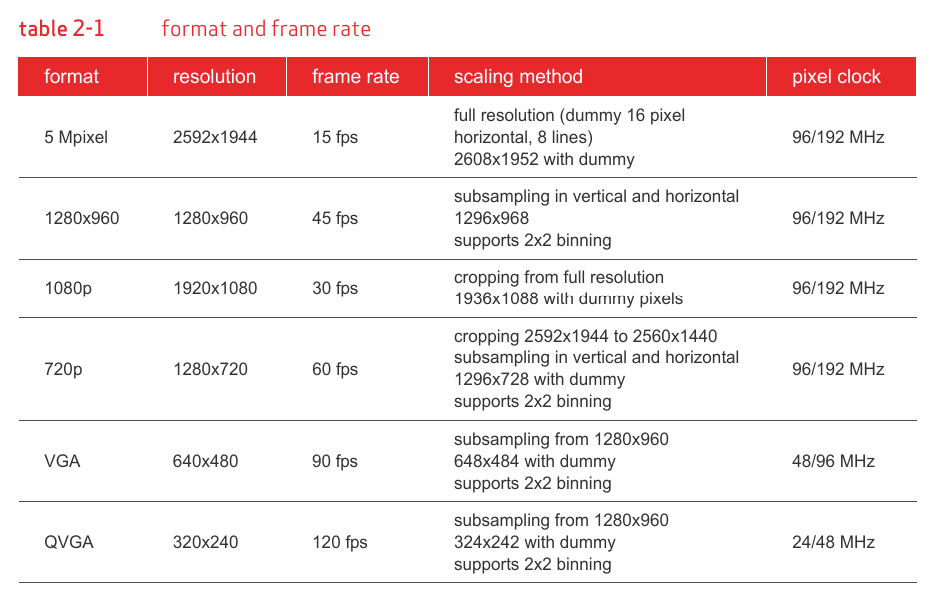
For visible-light image sensor, FPGA drives VL\_PWDN to power down.

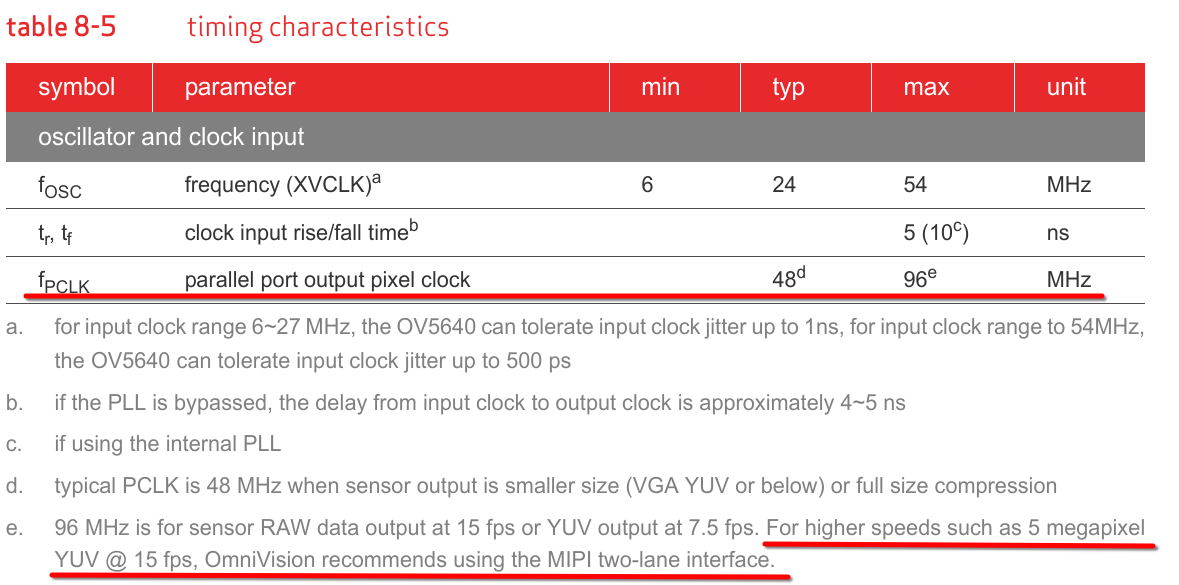
|  |  |  |
| --- | --- | --- |
| 1 | FPGA | VCORE: 1.2V VIO: 1.8V VAUX: 3.3V |
| 2 | DDR SDRAM | VDDQ: 3.3V VIO: 1.8V |
| 3 | Infrared Image Sensor | VDD: 5V VIO: 1.8V |
| 4 | Visible-Light Image Sensor | VCORE: 1.5V VANALOG: 2.8V VIO:1.8V |
| 5 | Laser Diode | VDD: 3.3V |

# 5. Camera Selection

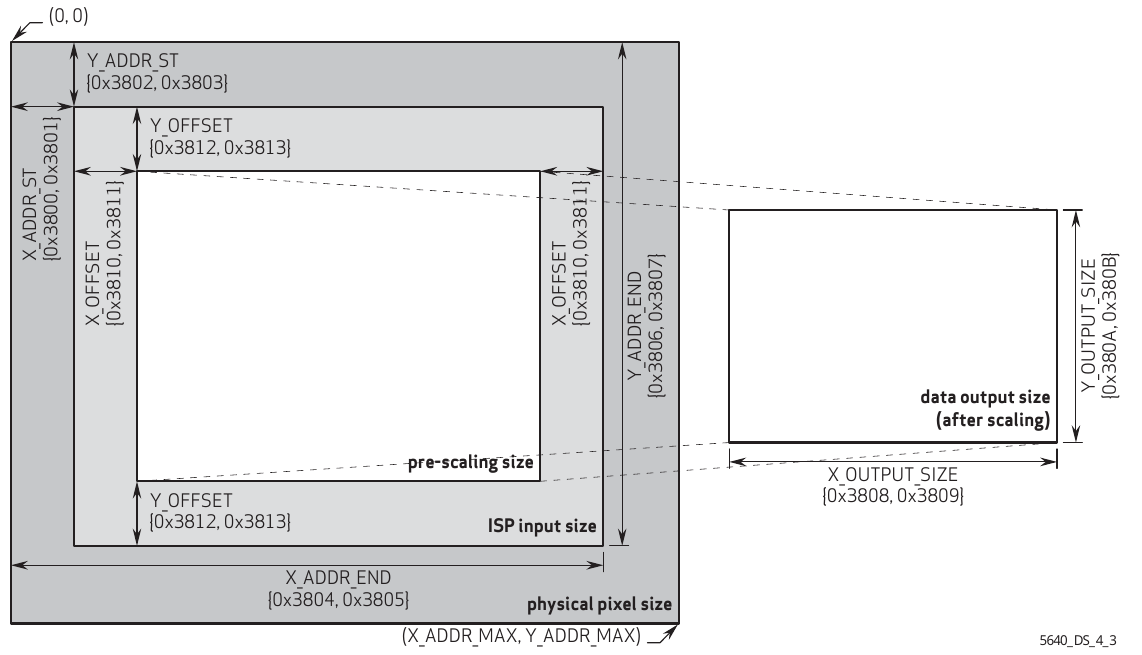
## 5.1 Visible-Light Camera

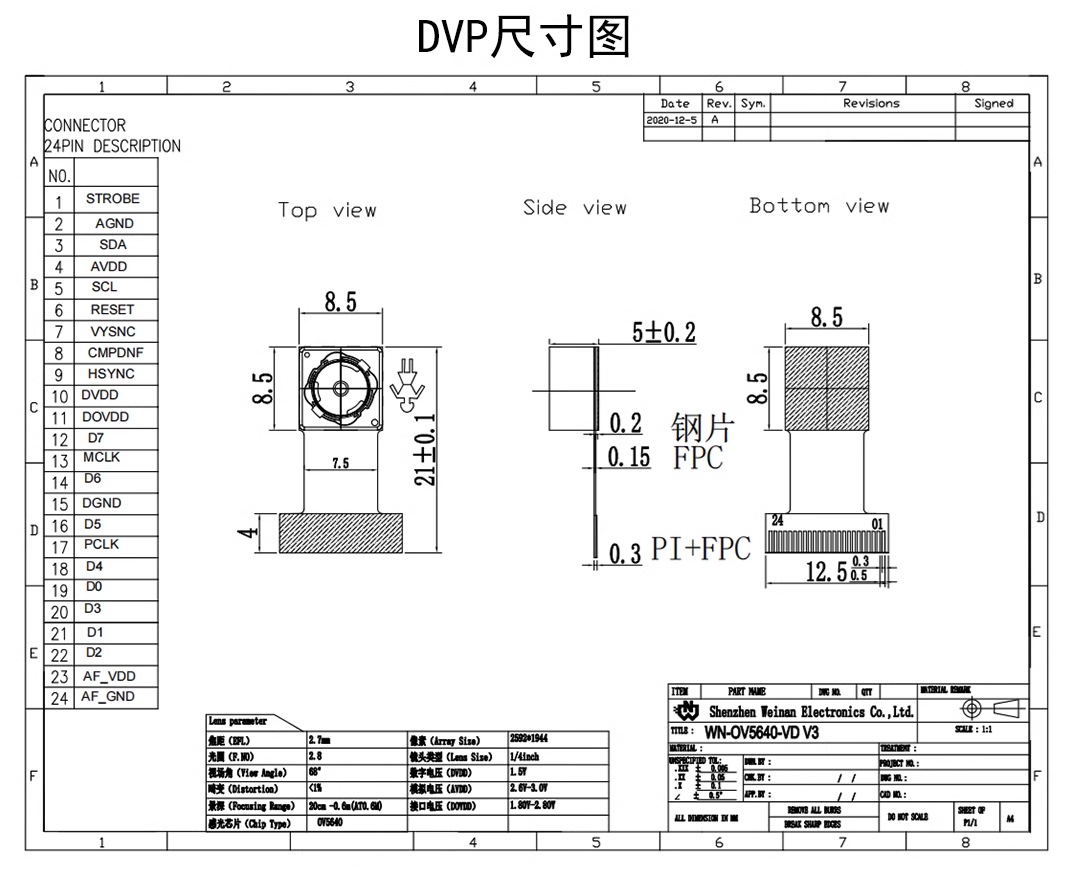
In this design, we choose OV5640 image sensor, it comes from OmniVision Company with 5 megapixel (2592\*1944), up to 15fps, configured with SCCB Interface. It supports DVP(Digital Video Port) Parallel Port and MIPI Port. The OV5640 PLL allows for an input frequency ranging from 6~27MHz and has a maximum VCO frequency of 800MHz. For low frame rates, we use DVP port, but for high resolution, OmniVision recommends to use MIPI port. So in this design, we follow official recommendation.





We can configure image windowing registers to scale images from the full size 2592\*1944 to an expected size.





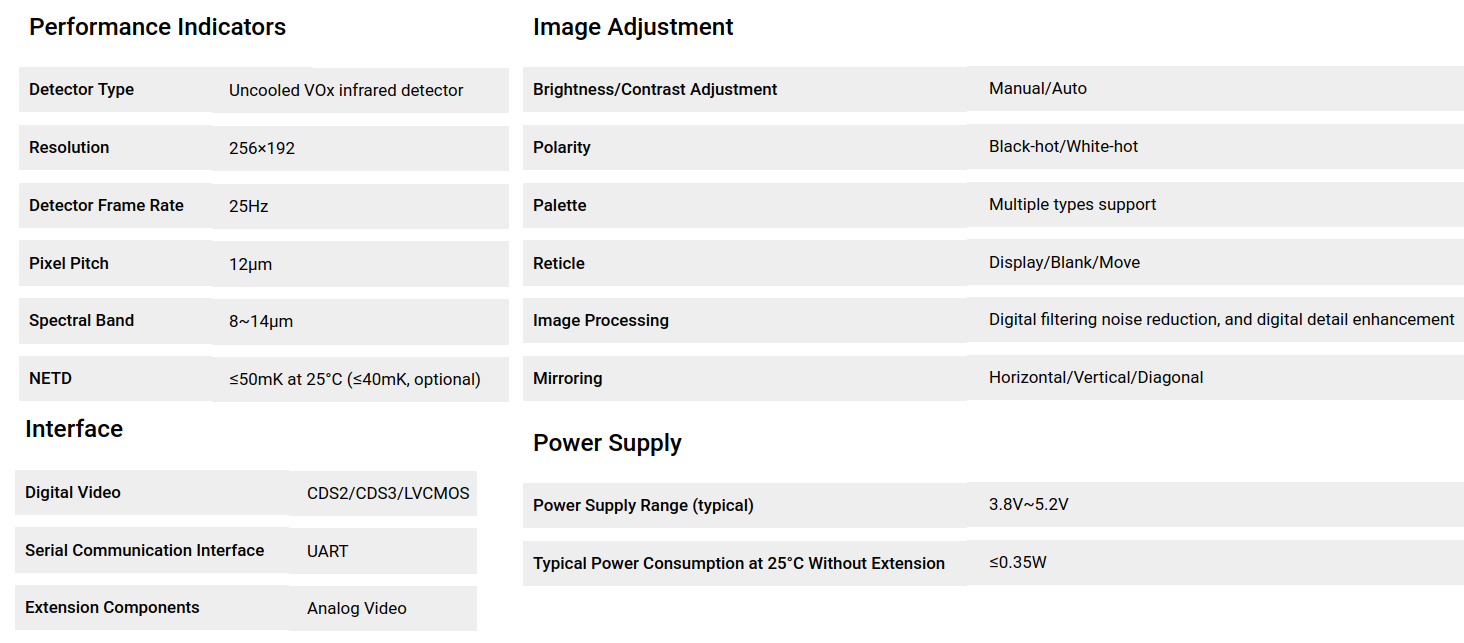


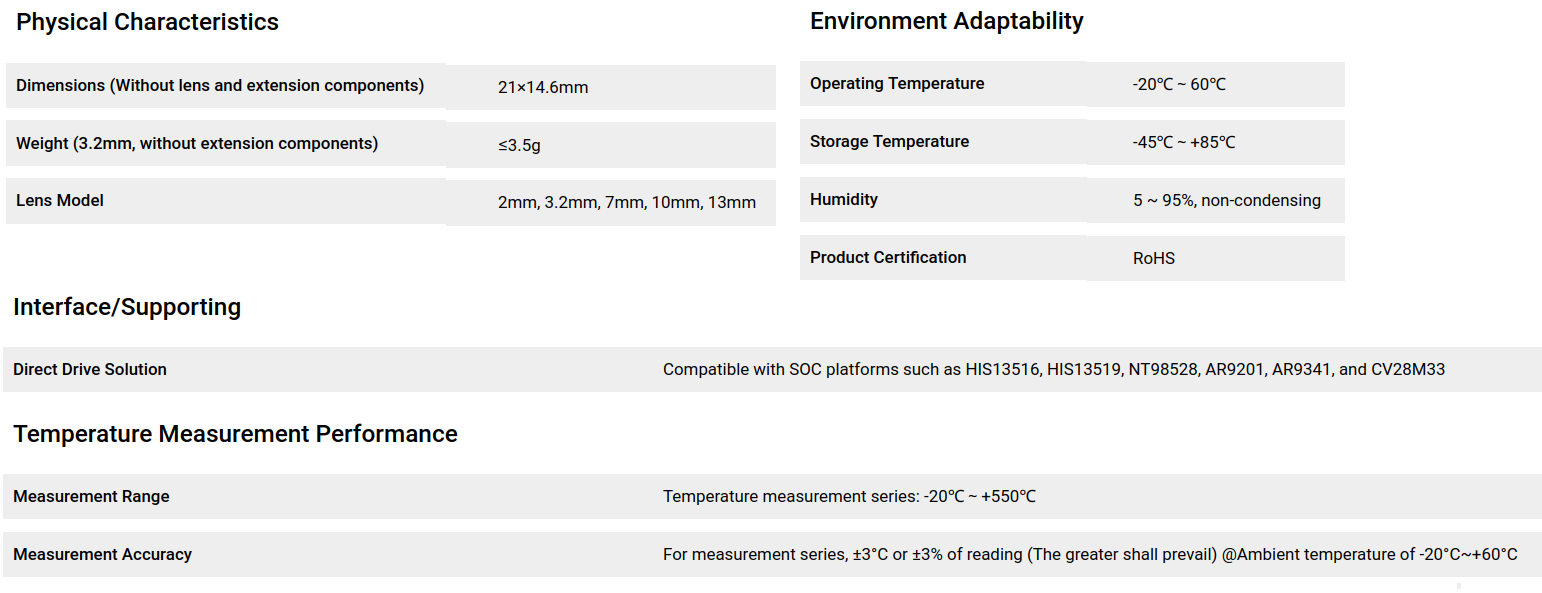
**Power Rail Requirement**

|  |  |  |
| --- | --- | --- |
| AVDD | 2.6V~3.0V | 2.8V |
| DVDD | 1.5V+/-5% | 1.5V |
| AF\_VDD | 2.8V | 2.8V |
| IO VDD | 1.8V/2.8V | 1.8V |
| Power Consumption | [180mW@full](mailto:180mW@full) size(active) |  |

## 5.2 Infrared Image Sensor Selection

In this design, we choose Yantai RayThink Turing C256 Infrared Module. Small size, low power consumption <=350mW, image resolution 256\*192, it supports Parallel Data Output and MIPI interface.





## 5.3 Image Sensor Switching

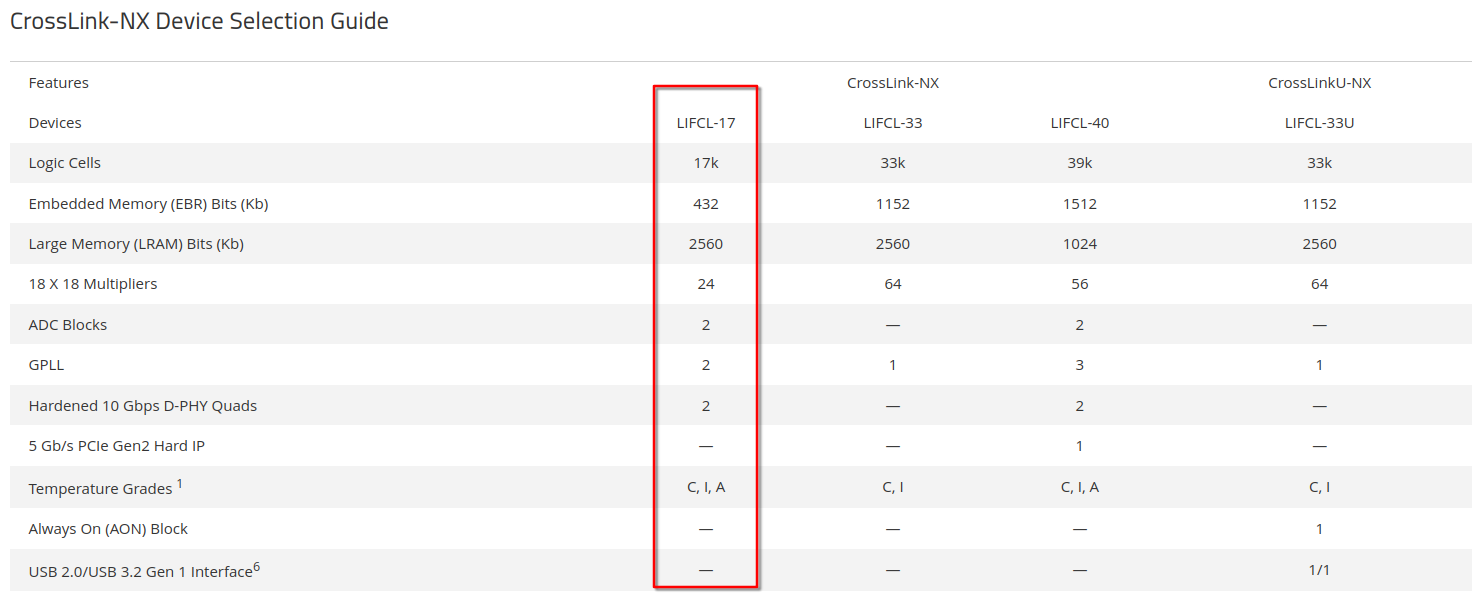
Limited by the farad capacitor stored energy, only one image sensor can be operated at a single time. Which image sensor will be used when the back-end system start up?

We add a light dependent resistor on board to select image sensor dynamically according to ambient light. In daytime, Visible-Light Image Sensor will be used. At night, Infrared Image Sensor will be used.

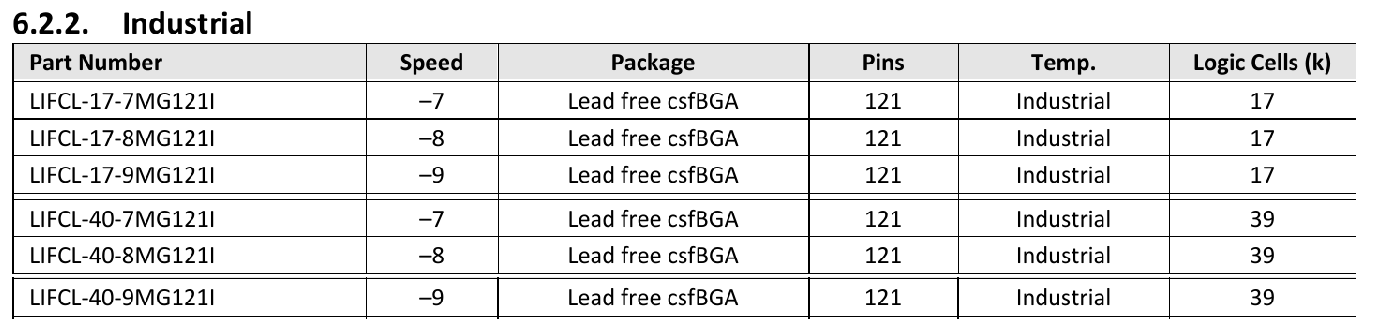
There’s also a SPI EEPROM available on board. We write a flag byte into external EEPROM, 0x7382(‘I’ ‘R’ ASCII Code) for Infrared Image Sensor, 0x8676 (‘V’ ‘L’ ASCII Code) for Visible Light Image Sensor. Each time, the back-end system starts up, it reads EEPROM to determine which image sensor will be used.

# 6. FPGA Selection

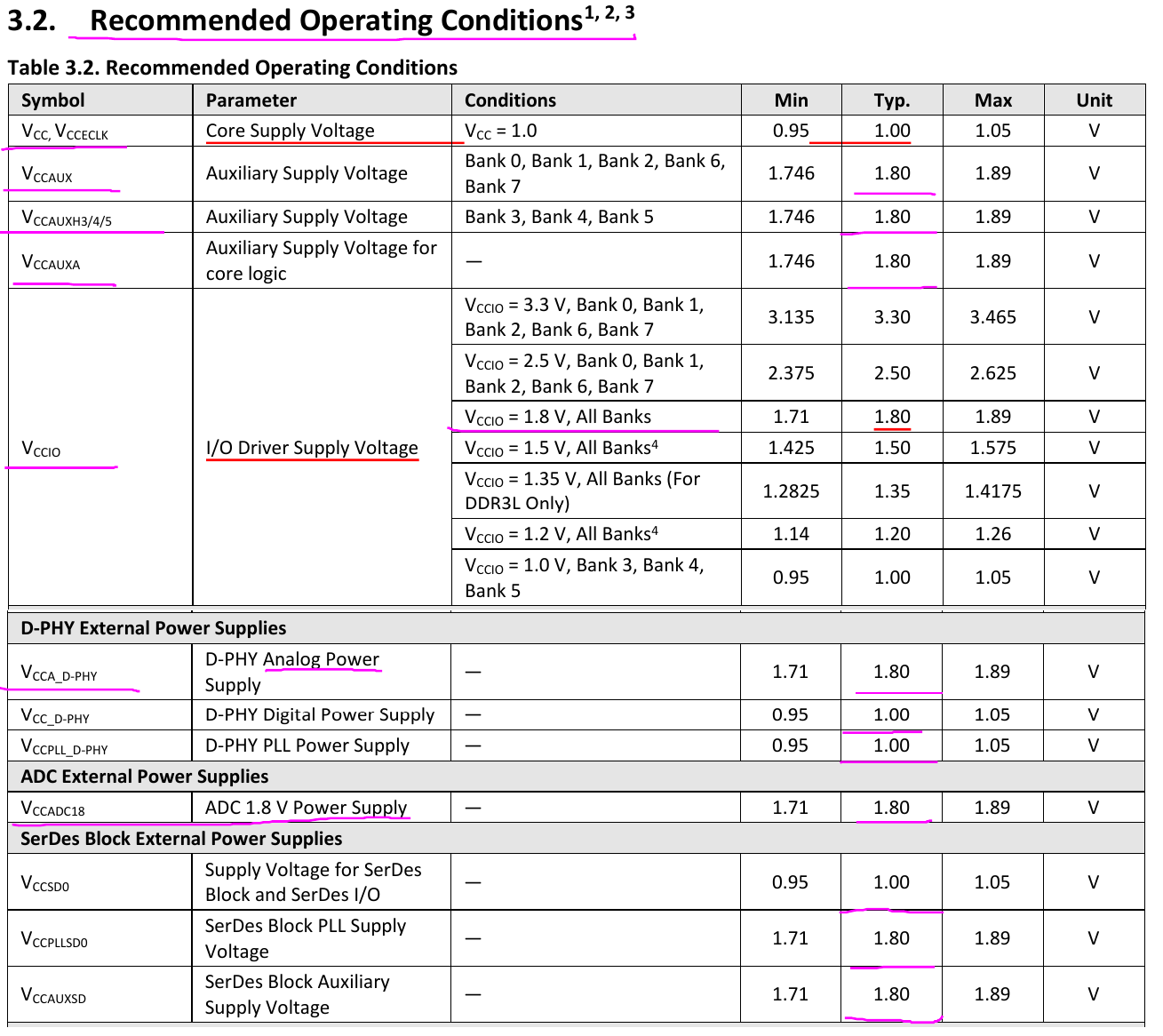
Since the huge different bandwidth between input and output, we need an SDRAM to hold data temporarily, after captured one complete frame, we read from SDRAM and upload data via UART at a low speed. In previous design, we use two chips due to lack of I/O. For future expansion, we choose a big footprint with adequate I/O. MIPI port is used for high resolution image. Considering there are 2 images sensors on board, FPGA must have 2 MIPI D-PHY. Lattice Radiant Software supports CrossLink-NX series, and we have experience of using Radiant.



From the Ordering Table, two types are appropriate for our application. LIFCL is abbreviation for Lattice Family Cross Link. BGA footprint to reduce PCB size, adequate pins for external components connection, commercial, industrial and automotive grades are available. We can use 39k Logic Cells at developing stage, switch to 17k Logic Cells in fabrication stage.

 CrossLink-NX device features two on board oscillator. The low frequency oscillator runs at 128KHz for low power operation. The high frequency oscillator runs at 450MHz, but can be divided down to a range of 256MHz to 2MHz. It also has two Global PLL used to synthesize clock frequeny, the input of GPLL can come from external CLK input pins or from internal routing. Each PLL has 6 clock outputs, can be used to drive the primary clock or edge clock networks.

We also reserve an external oscillator on board at the global clock input pins.

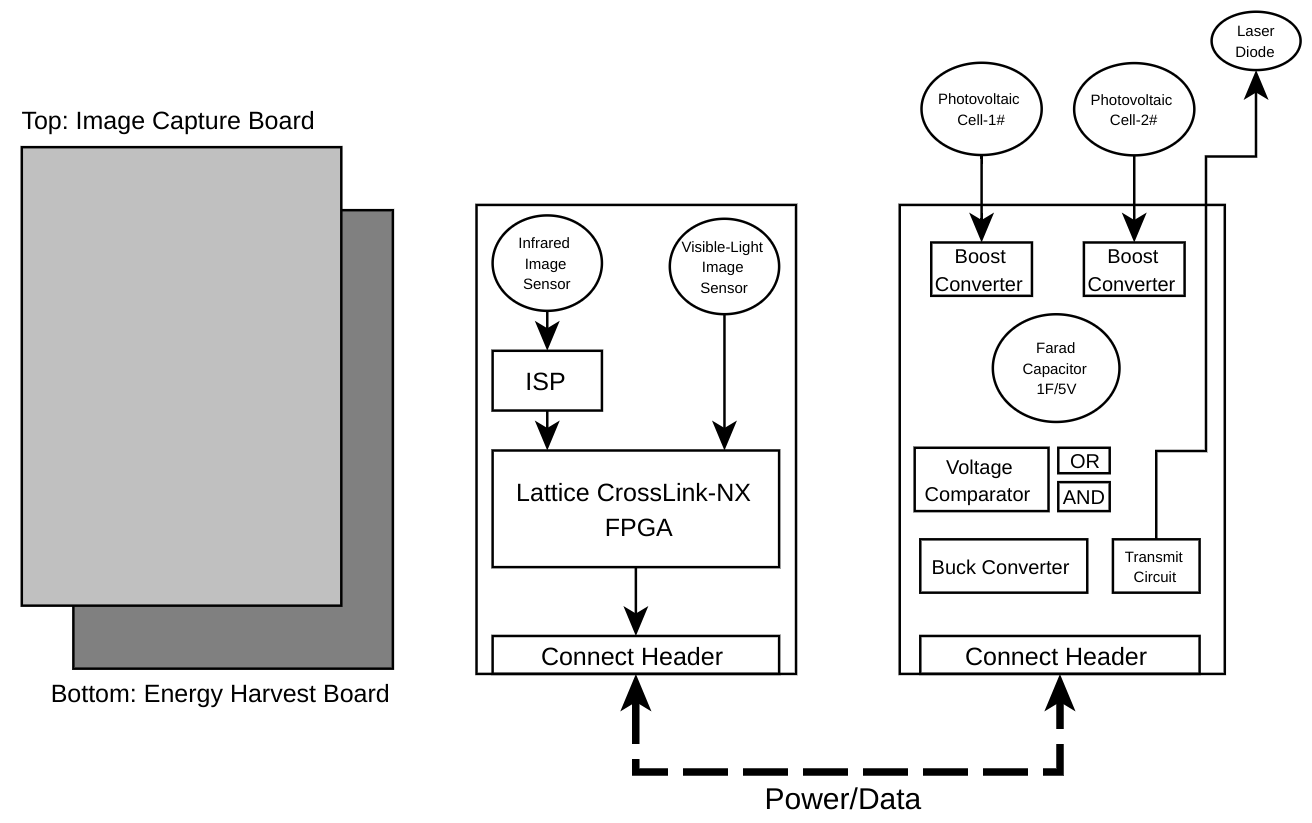
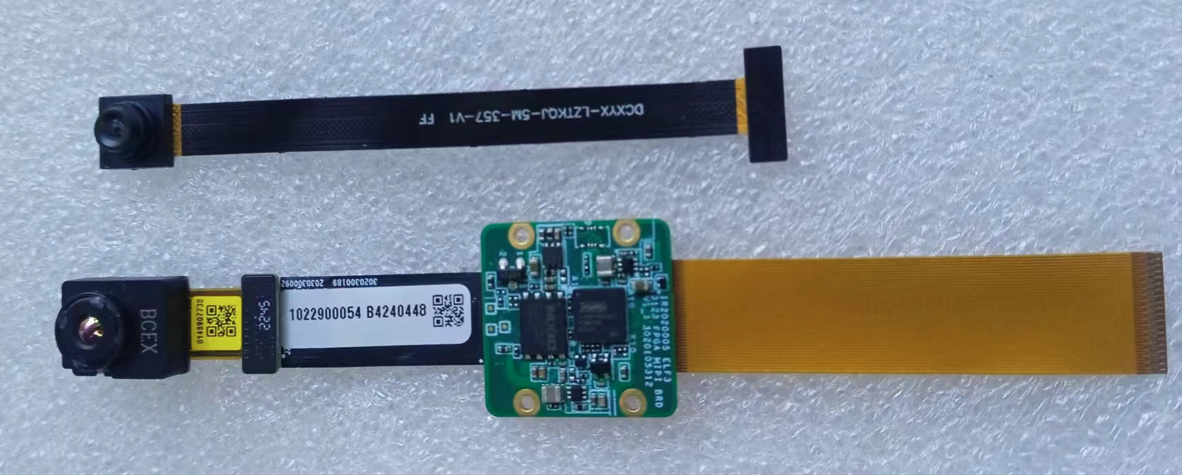
Power rails needed are 1.0V, 1.8V, 3.3V.

Additional Interfaces

1. Dual 12-bits 1MSPS ADC are available in each device.

# 7. Mechanical Installation

We prefer to make this system small as possible as we can. There are some considerations to choose integrated circuits we will use. We limit the FPGA size, select BGA footprint rather than QFP series. And for those buck converter circuit, the inductor is also large. To reduce size taking up on PCB. We split the entire system into 2 PCB, and use vertical installation approach. Image Capture Board is on top layer, two image sensors are aligned horizontally. Energy Harvest Board is on bottom layer, the Farad Capacitor is soldered on board, but two photovoltaic cells and the laser diode do not take up PCB size. These shapes are not standard, not suit to install on board. Two boards use Connect Header to transfer power supply and data in bi-direction.



**/\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\* End of File \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*/**