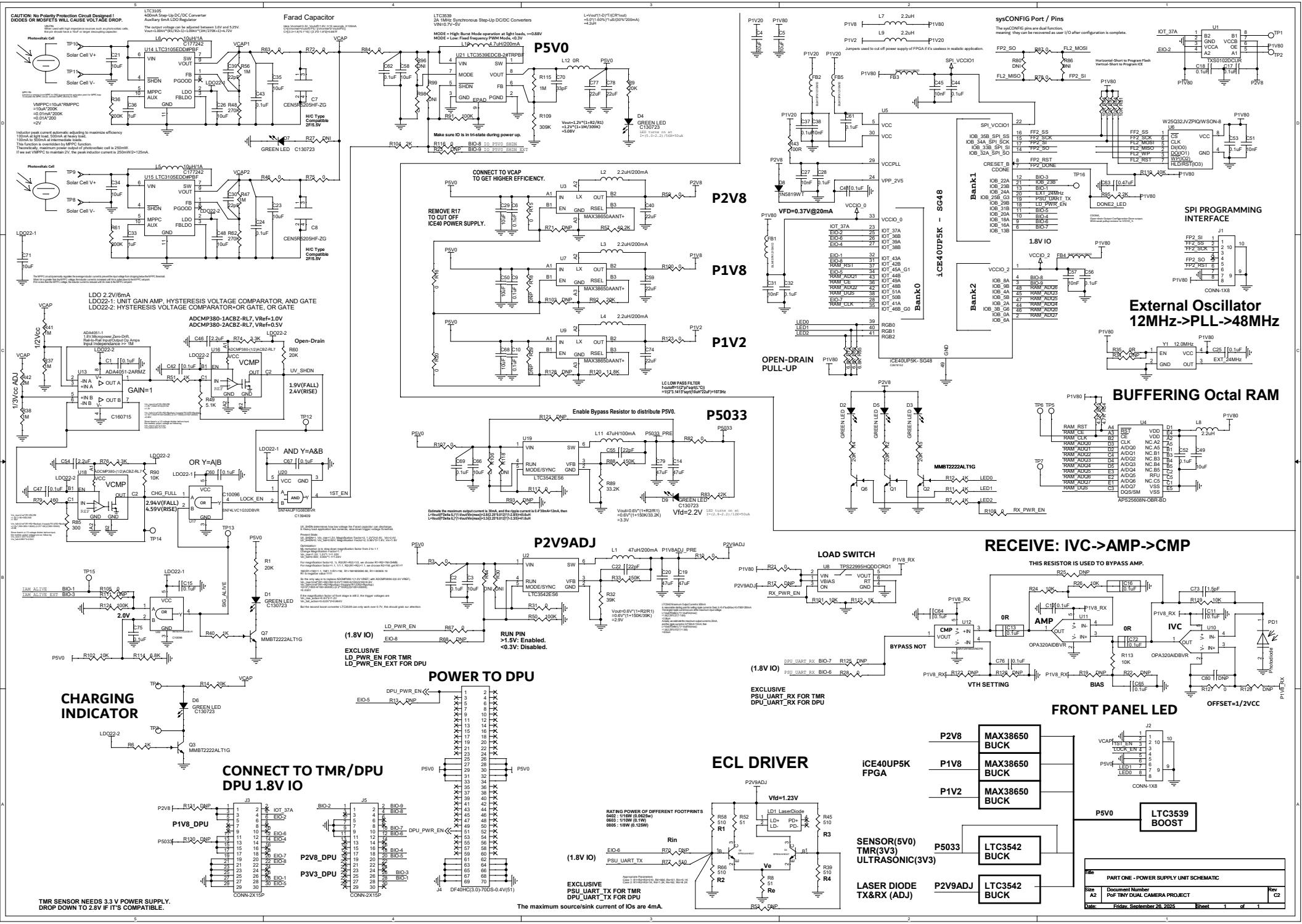
CAUTION: No Polarity Protection Circuit Designed !
DIODES OR MOSFETS WILL CAUSE VOLTAGE DROP.
Photovoltaic Cell
Solar Cell V+
Solar Cell V-
LTC3105
400mA Step-Up DC/DC Converter
Auxiliary 5mA LDO Regulator
U14 LTC3105EDDMPBF
Farad Capacitor
P5V0
LTC3539
2A 1MHz Synchronous Step-Up DC/DC Converters
U21 LTC3539EDCB-2#TRPBF
MODE = High: Burst Mode operation at light loads, >=0.88V
MODE = Low: Fixed frequency PWM Mode, <0.3V
Make sure IO is in tri-state during power up.
GREEN LED C130723
H/C Type Compatible 2F/6.5V
U15 LTC3105EDDMPBF
LDO 2.2V/6mA
LDO22-1: UNIT GAIN AMP, HYSTERESIS VOLTAGE COMPARATOR, AND GATE
LDO22-2: HYSTERESIS VOLTAGE COMPARATOR+OR GATE, OR GATE
ADCMP380-1ACBZ-RL7, VRef=1.0V
ADCMP380-2ACBZ-RL7, VRef=0.5V
ADA4051-1
1.8V Micropower, Zero-Drift, Rail-to-Rail Input/Output Op Amps
Input Independence >> 1M
ADA4051-2ARMZ
GAIN=1
C160715
Open-Drain
VCMP
1.9V(FALL)
2.4V(RISE)
OR Y=A|B
AND Y=A&B
2.94V(FALL)
4.59V(RISE)
CHG_FULL
LOCK_EN
1ST_EN
SIG_ALIVE
IAM_ALIVE
IAM_ALIVE_EXT
2.0V
CHARGING INDICATOR
CONNECT TO TMR/DPU
DPU 1.8V IO
P1V8_DPU
P2V8_DPU
P3V3_DPU
CONN-2X15P
TMR SENSOR NEEDS 3.3 V POWER SUPPLY.
DROP DOWN TO 2.8V IF IT'S COMPATIBLE.
P5V0
CONNECT TO VCAP
TO GET HIGHER EFFICIENCY.
REMOVE R17
TO CUT OFF
ICE40 POWER SUPPLY.
P2V8
VFD=0.37V@20mA
P1V8
P1V2
OPEN-DRAIN
PULL-UP
LC LOW PASS FILTER
P5033
Enable Bypass Resistor to distribute P5V0.
LTC3542ES6
Vfd=2.2V
P2V9ADJ
LOAD SWITCH
TPS22995HQDDCRQ1
RUN PIN
>1.5V: Enabled.
<0.3V: Disabled.
(1.8V IO)
EXCLUSIVE
LD_PWR_EN FOR TMR
LD_PWR_EN_EXT FOR DPU
POWER TO DPU
DPU_PWR_EN
J4 DF40HC(3.0)-70DS-0.4V(51)
The maximum source/sink current of IOs are 4mA.
ECL DRIVER
P2V9ADJ
Vfd=1.23V
LD1 LaserDiode
RATING POWER OF DIFFERENT FOOTPRINTS
0402 : 1/16W (0.0625W)
0603 : 1/10W (0.1W)
0805 : 1/8W (0.125W)
Rin
PSU_UART_TX
EXCLUSIVE
PSU_UART_TX FOR TMR
DPU_UART_TX FOR DPU
sysCONFIG Port / Pins
The sysCONFIG pins are dual function,
meaning they can be recovered as user I/O after configuration is complete.
Jumpers used to cut off power supply of FPGA if it's useless in realistic application.
Horizontal-Short to Program Flash
Vertical-Short to Program ICE
iCE40UP5K - SG48
Bank0
Bank1
Bank2
1.8V IO
SPI PROGRAMMING INTERFACE
External Oscillator
12MHz->PLL->48MHz
BUFFERING Octal RAM
APS25608N-OBR-BD
RECEIVE: IVC->AMP->CMP
THIS RESISTOR IS USED TO BYPASS AMP.
AMP
IVC
OPA320AIDBVR
BYPASS NOT
VTH SETTING
BIAS
OFFSET=1/2VCC
FRONT PANEL LED
P2V8
P1V8
P1V2
iCE40UP5K
FPGA
MAX38650
BUCK
P5V0
LTC3539
BOOST
P5033
LTC3542
BUCK
SENSOR(5V0)
TMR(3V3)
ULTRASONIC(3V3)
LASER DIODE
TX&RX (ADJ)
P2V9ADJ
Title
PART ONE - POWER SUPPLY UNIT SCHEMATIC
Size A2
Document Number
PoF TINY DUAL CAMERA PROJECT
Rev C2
Date: Friday, September 26, 2025
Sheet 1 of 1