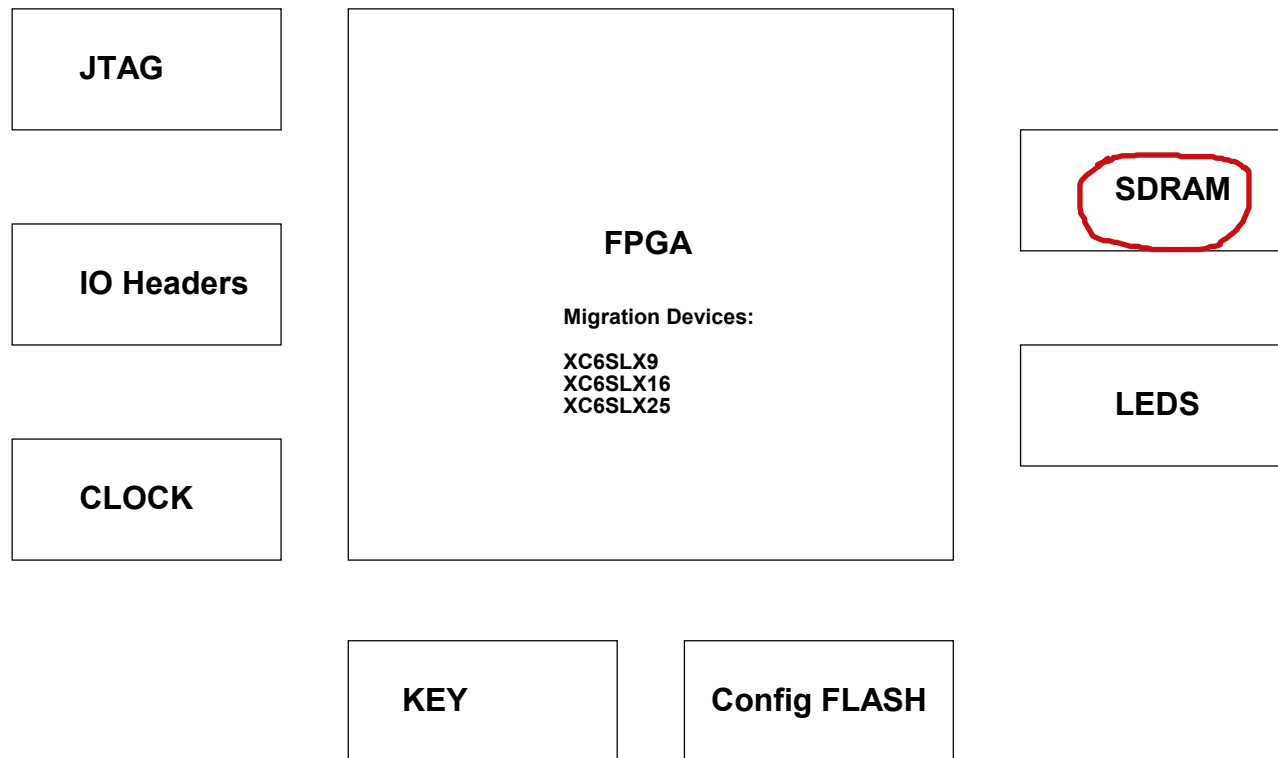


SCHEMATIC PAGE DESCRIPTION :

PAGE01: BLOCK DIAGRAM
PAGE02: POWER DISTRIBUTION
PAGE03: FPGA IO
PAGE04: FPGA CLOCK
PAGE05: FPGA Config
PAGE06: FPGA Power
PAGE07: SDRAM
PAGE08: System Power
PAGE09: Connectors

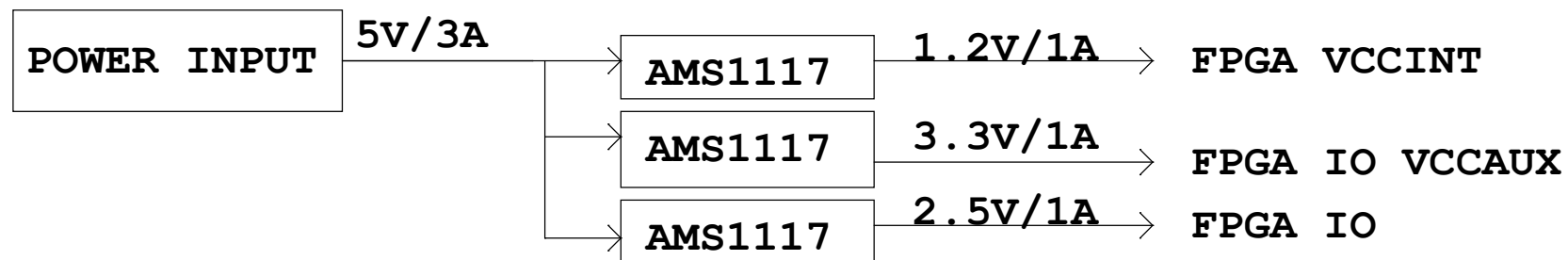
BLOCK DIAGRAM

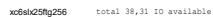
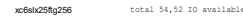


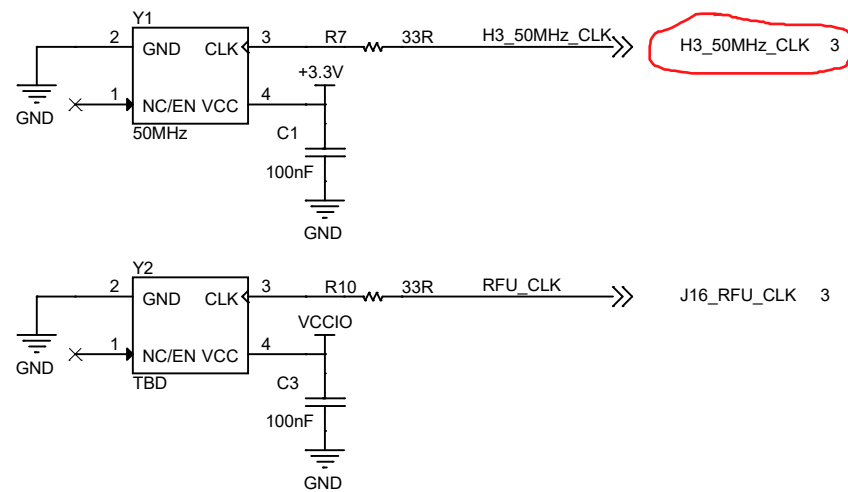
POWER CONSUMPTION

COMPONENTS	VOTAGE&CURRENT						
	1 . 2V	2 . 5V	3 . 3V				
FPGA	TBD	TBD	TBD				

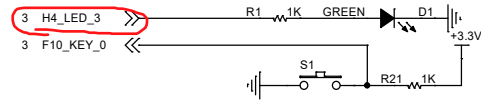
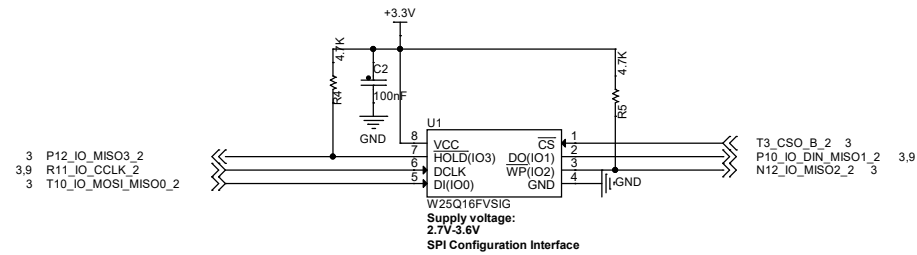
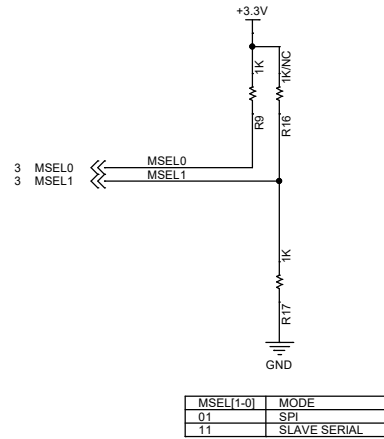
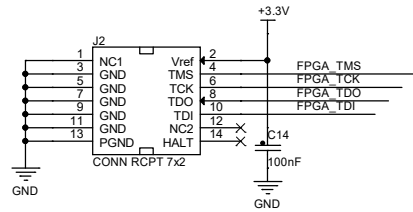
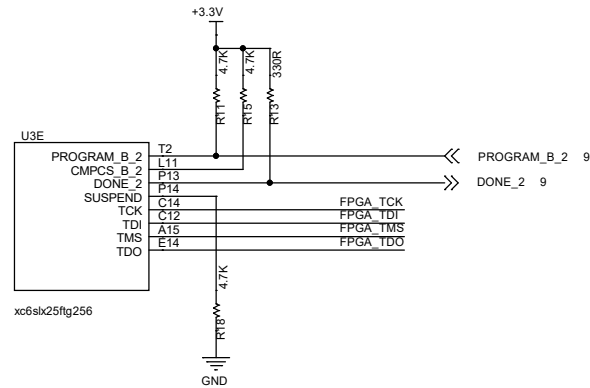
POWER DISTRIBUTION

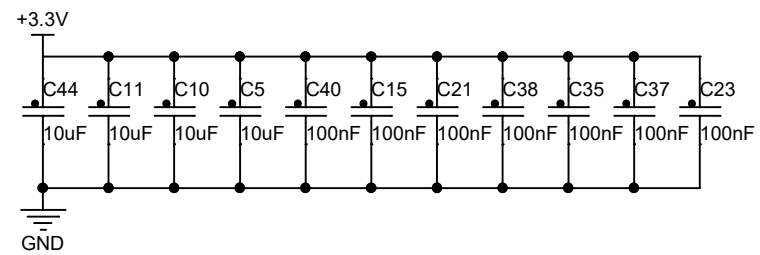
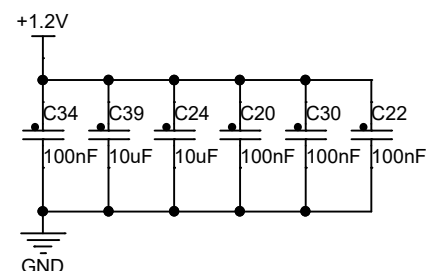
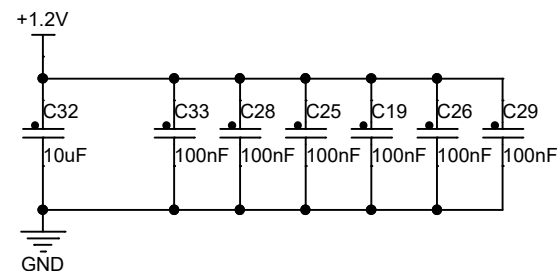
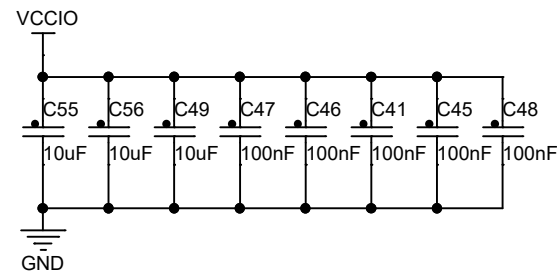
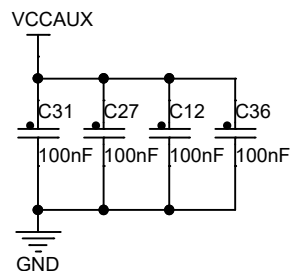
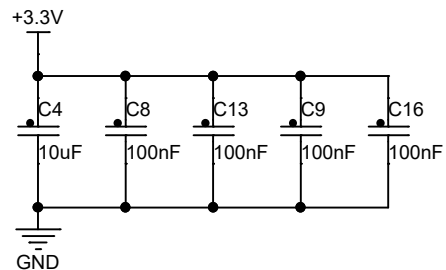
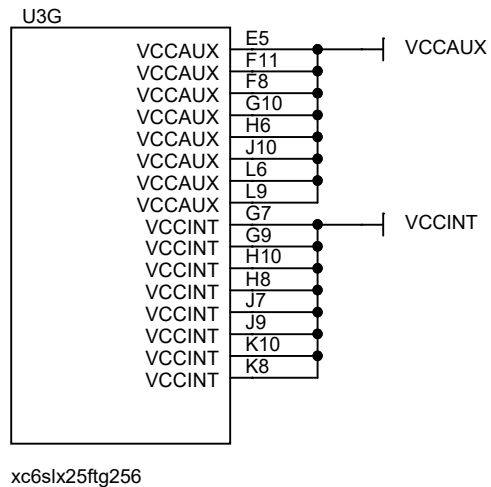
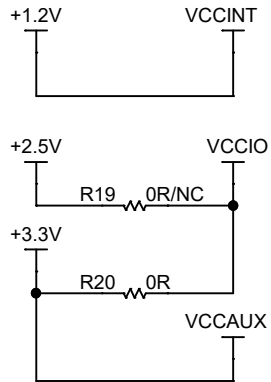
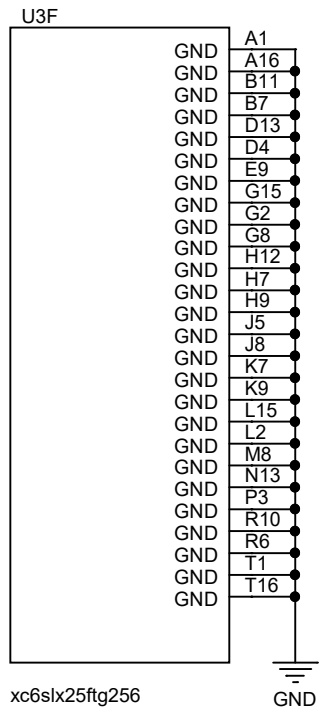




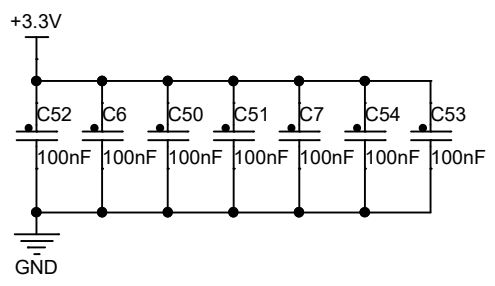
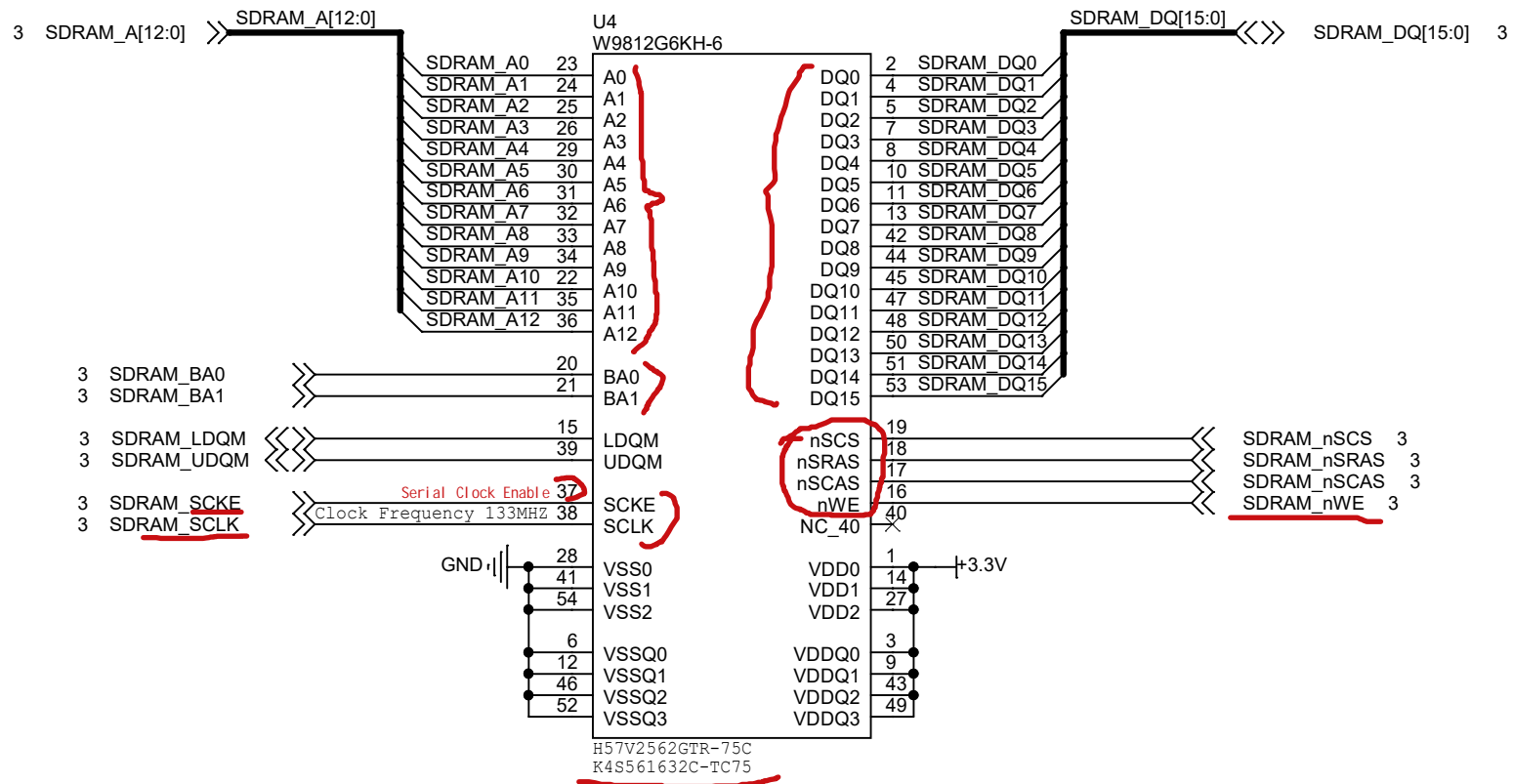


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Title Xilinx Spartan-6 FPGA S604		
Size A4	Document Number FPGA CLOCK	Rev V1.0
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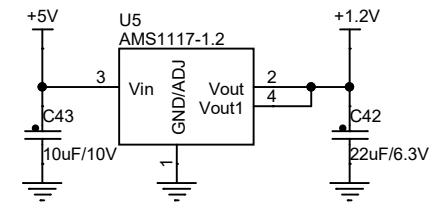
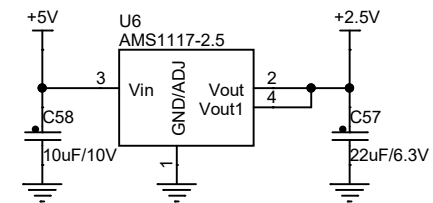
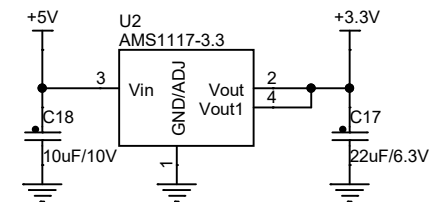
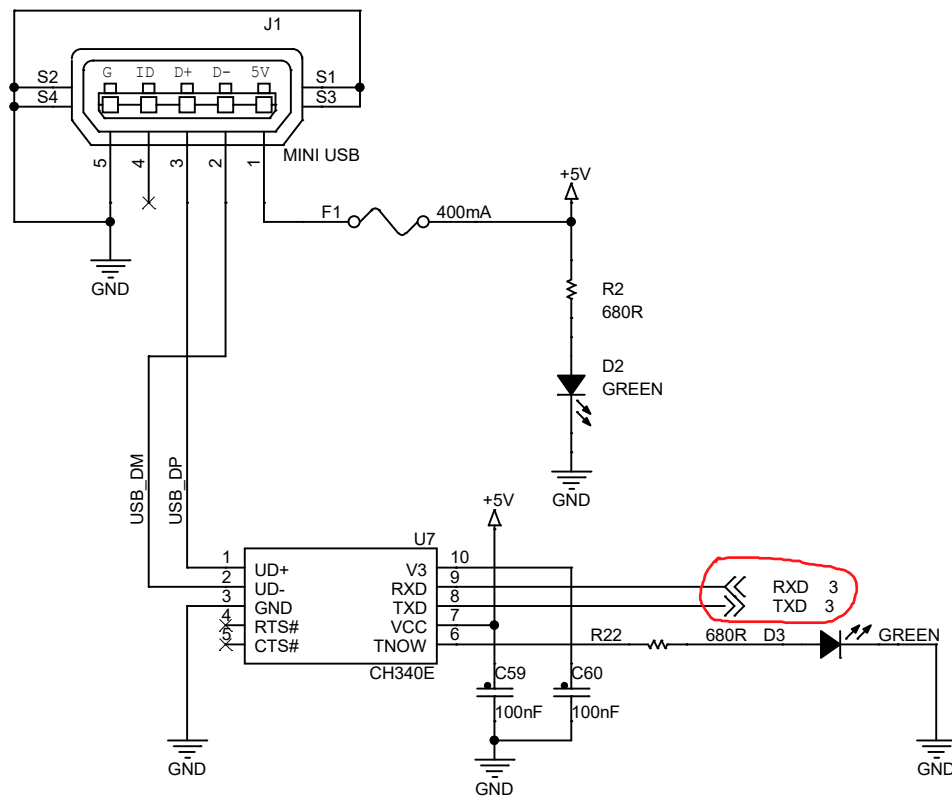




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Xilinx Spartan-6 FPGA S604			
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A	FPGA Power		V1.0
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