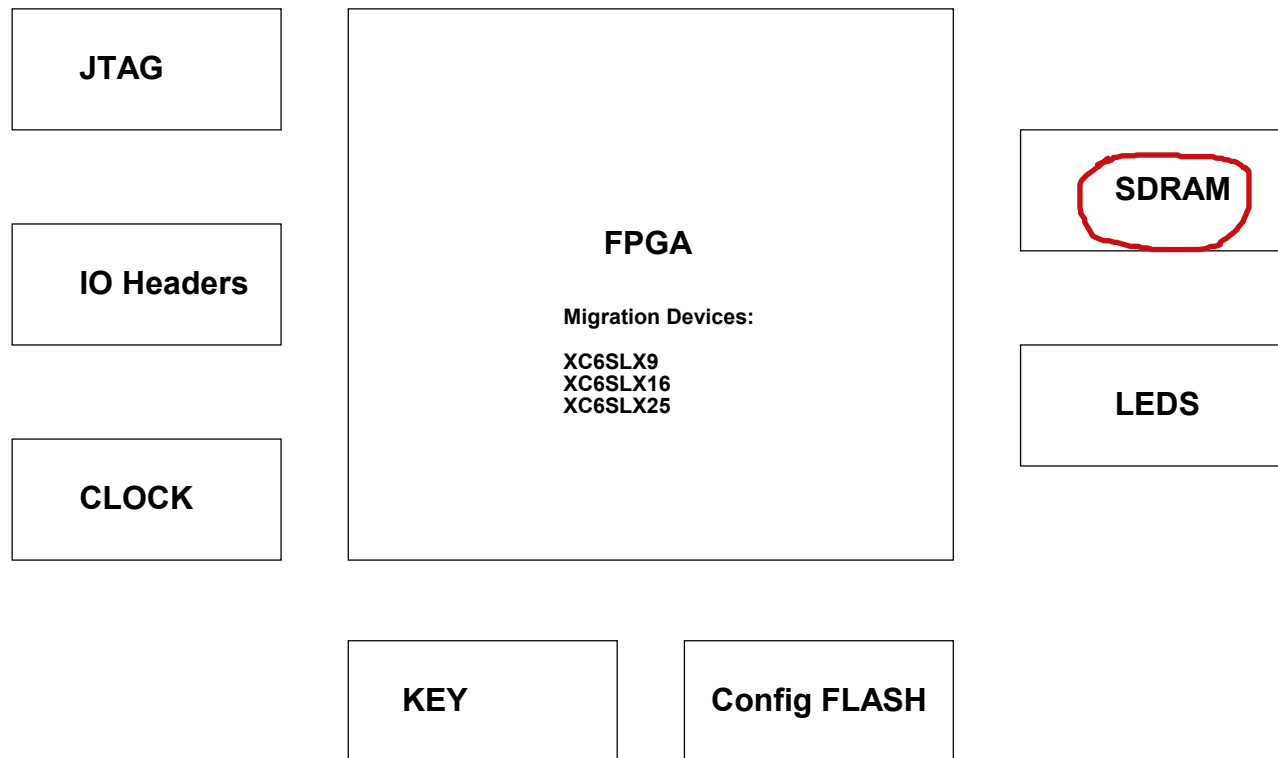


SCHEMATIC PAGE DESCRIPTION :

PAGE01: BLOCK DIAGRAM
PAGE02: POWER DISTRIBUTION
PAGE03: FPGA IO
PAGE04: FPGA CLOCK
PAGE05: FPGA Config
PAGE06: FPGA Power
PAGE07: SDRAM
PAGE08: System Power
PAGE09: Connectors

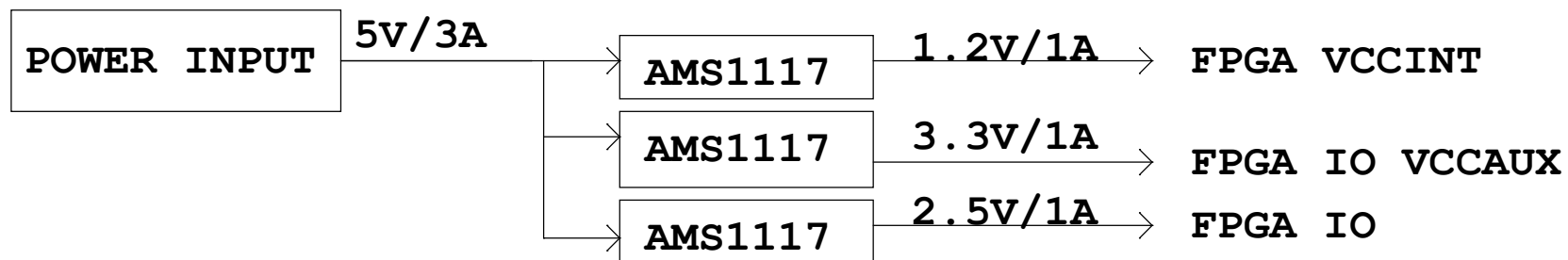
BLOCK DIAGRAM

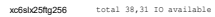
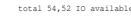
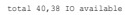


POWER CONSUMPTION

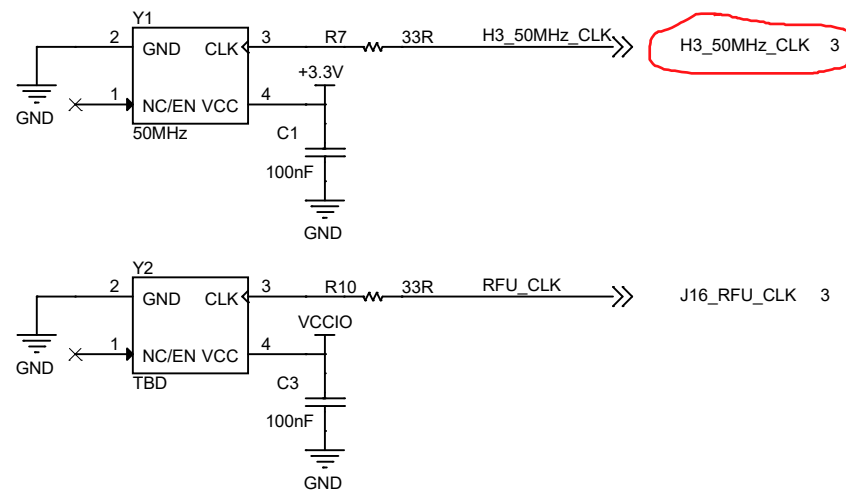
COMPONENTS	VOTAGE&CURRENT						
	1 . 2V	2 . 5V	3 . 3V				
FPGA	TBD	TBD	TBD				

POWER DISTRIBUTION

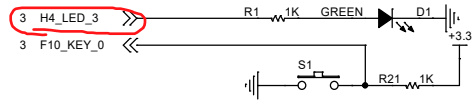
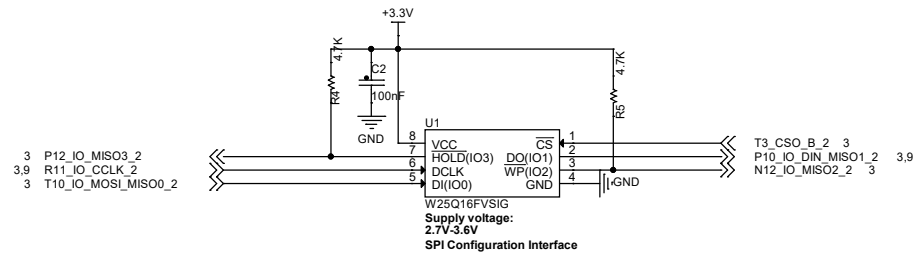
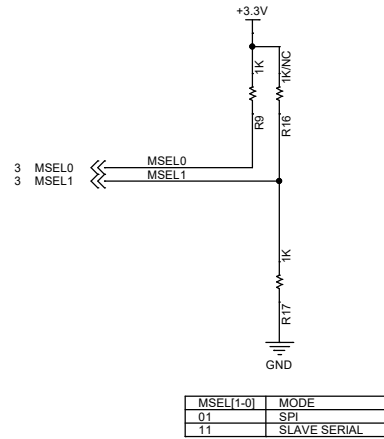
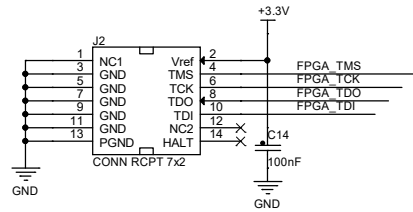
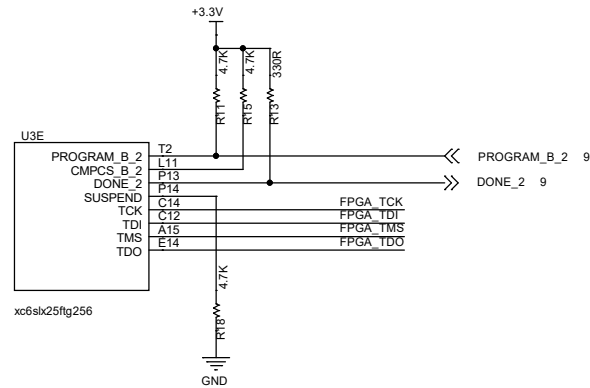


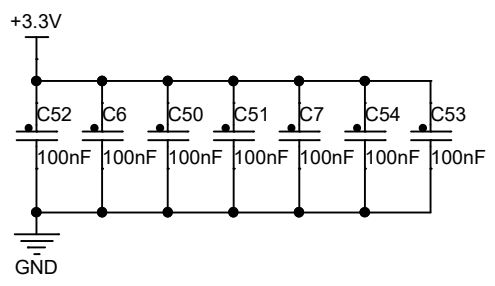
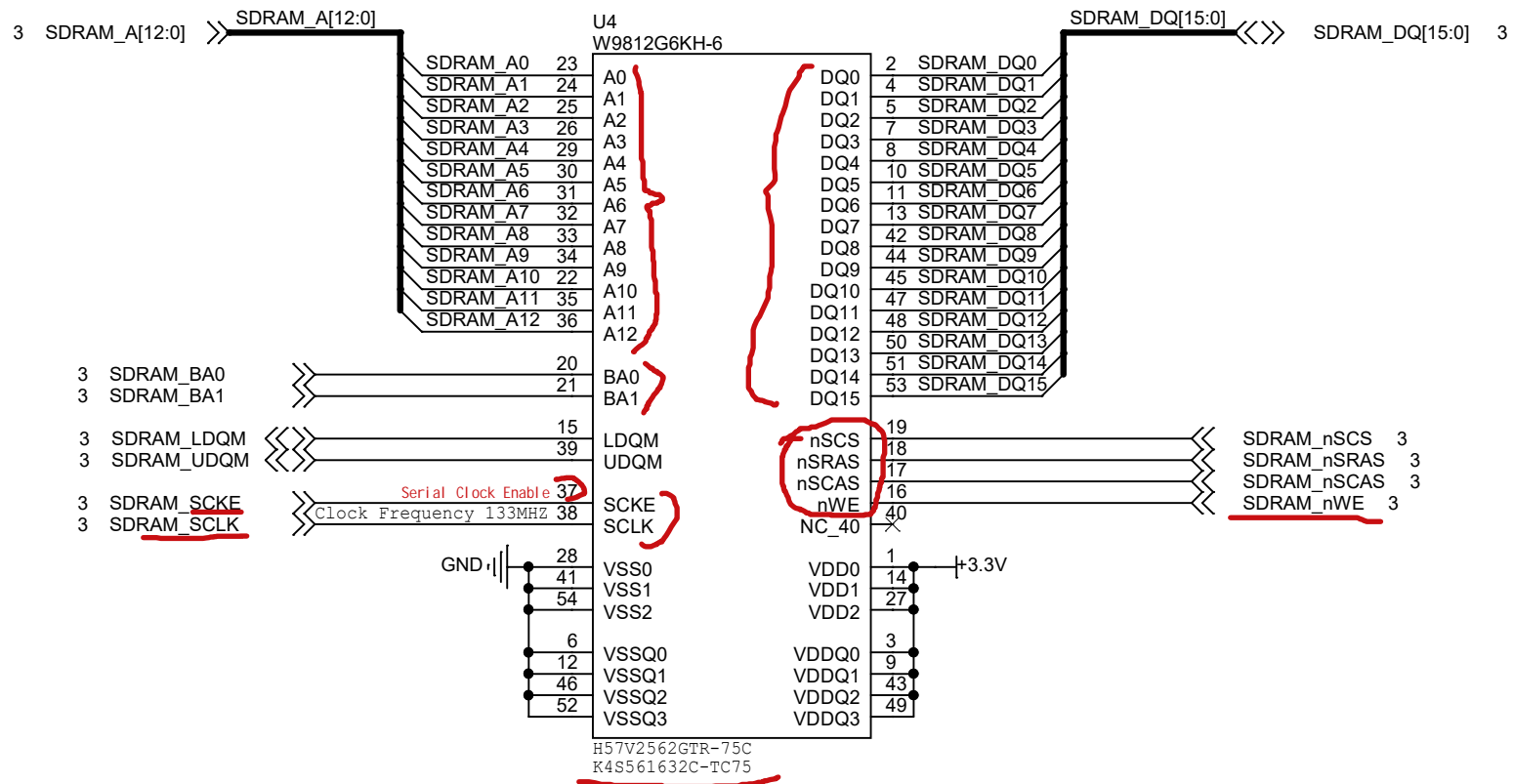


SDRAM_DQ[15:0] <> SDRAM_DQ[15:0] 7

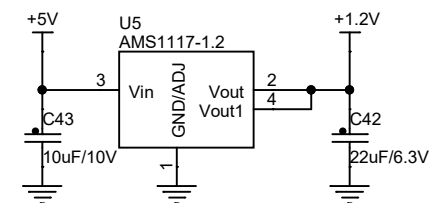
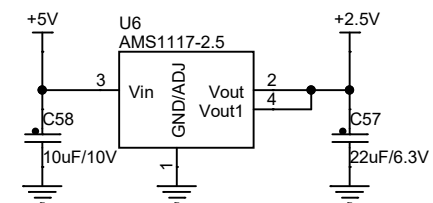
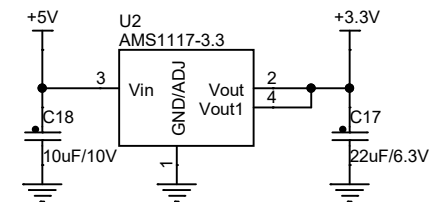
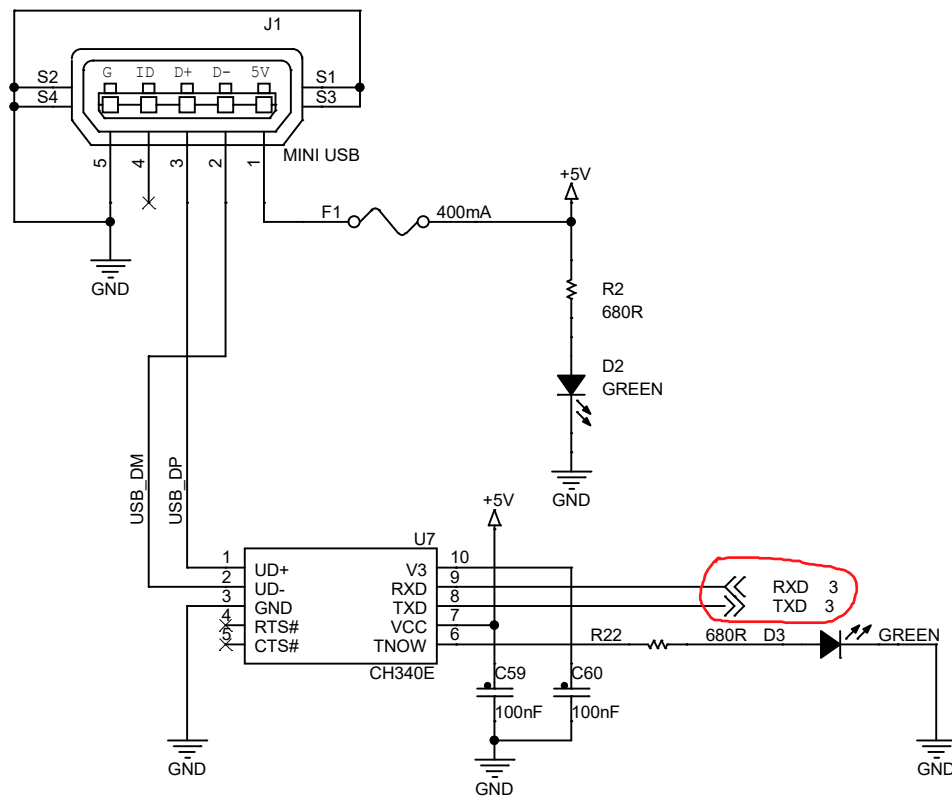


Chengdu black hawk electronic technology co.,Ltd			
Title		Xilinx Spartan-6 FPGA S604	
Size	Document Number		Rev
A4	FPGA CLOCK		V1.0
Date:	Saturday, May 29, 2021		Sheet 4 of 9





Chengdu black hawk electronic technology co.,Ltd			
Title			
Xilinx Spartan-6 FPGA S604			
Size	Document Number		Rev
A	SDRAM		V1.0
Date:	Saturday, May 29, 2021	Sheet	7 of 9



Chengdu black hawk electronic technology co.,Ltd			
Title		Xilinx Spartan-6 FPGA S604	
Size	Document Number		Rev
A4	System Power		V1.0
Date:	Saturday, May 29, 2021		Sheet 8 of 9

