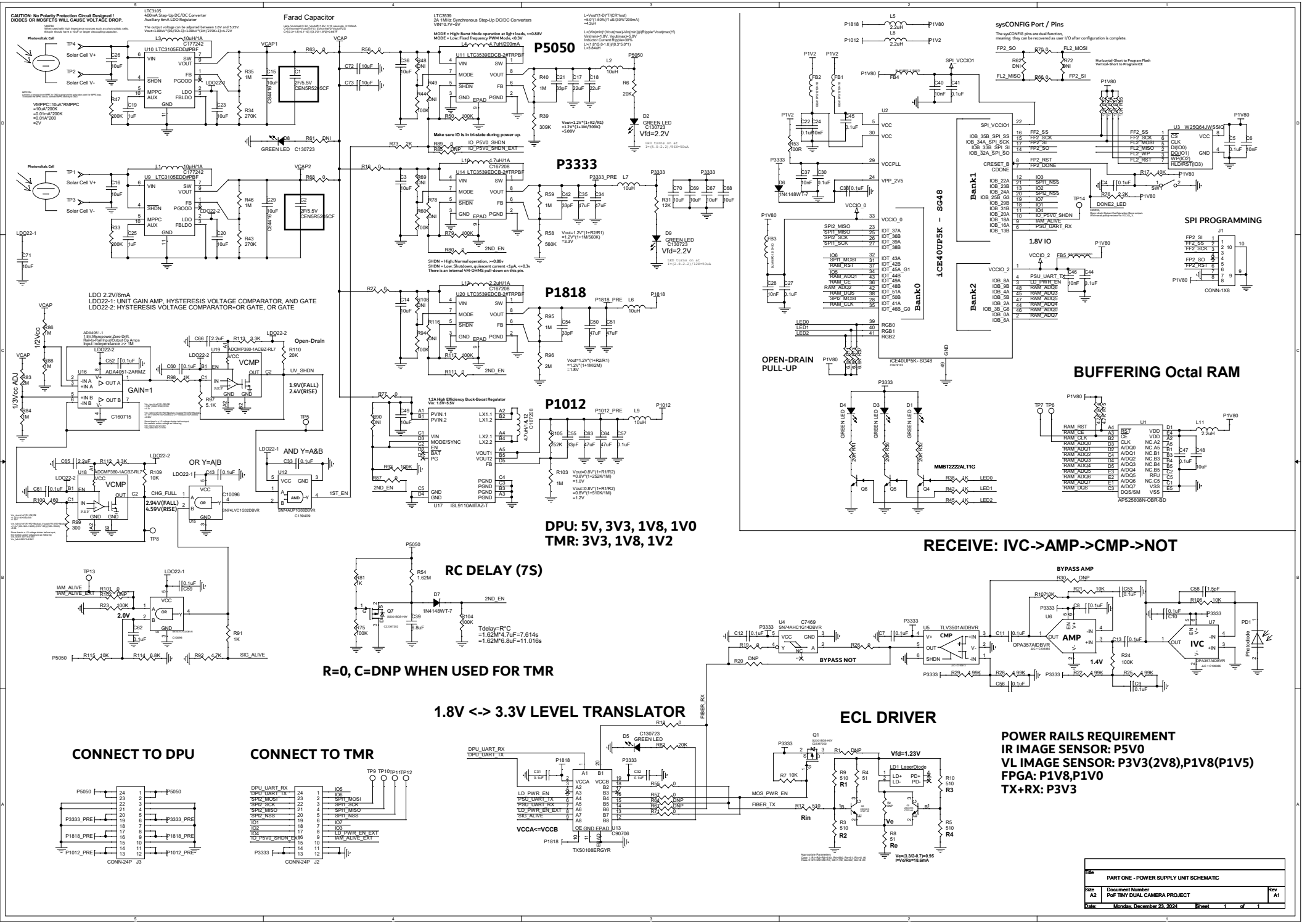
P5050
P3333
P1818
P1012
BUFFERING Octal RAM
RECEIVE: IVC->AMP->CMP->NOT
DPU: 5V, 3V3, 1V8, 1V0
TMR: 3V3, 1V8, 1V2
RC DELAY (7S)
R=0, C=DNP WHEN USED FOR TMR
1.8V <-> 3.3V LEVEL TRANSLATOR
ECL DRIVER
CONNECT TO DPU
CONNECT TO TMR
POWER RAILS REQUIREMENT
IR IMAGE SENSOR: P5V0
VL IMAGE SENSOR: P3V3(2V8),P1V8(P1V5)
FPGA: P1V8,P1V0
TX+RX: P3V3
PART ONE - POWER SUPPLY UNIT SCHEMATIC
Date: Monday, December 23, 2024