Application Note

Cell Balancing With BQ769x2 Battery Monitors

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ABSTRACT

The BQ769x2 battery monitor family (which includes the BQ76952, BQ76942, and BQ769142) features a cell-balancing function that can run autonomously or can be controlled by a host. This document describes how to use the cell-balancing feature of the device in a battery pack application. Increasing the current capability of the IC using external FETs and BJTs is described. The algorithm for balancing in stand-alone mode is described as well as considerations for implementing a host-controlled balancing algorithm which avoids damage to the IC.

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Trademarks

1 Introduction

Cells are usually matched during the manufacturing of a battery pack. Over time, an imbalance in the state of charge may develop between cells and reduce the overall capacity of the pack. Cell balancing that equalizes the cells allows the pack to operate longer.

The BQ769x2 supports passive cell balancing by bypassing the current of selected cells during charging or at rest, using either integrated bypass switches between cells, or external bypass FET switches. The device incorporates a voltage-based balancing algorithm which can optionally balance cells autonomously without requiring any interaction with a host processor. Or if preferred, balancing can be entirely controlled manually from a host processor.

Due to the current that flows into the cell input pins on the BQ769x2 device while balancing is active, the measurement of cell voltages and evaluation of cell voltage protections by the device is modified during balancing. Balancing is temporarily disabled during the regular measurement loop while the actively balanced cell is being measured by the ADC, as well as when the cells immediately adjacent to the active cell are being measured. Similarly, balancing on the top cell is disabled while the stack voltage measurement is underway. This occurs on every measurement loop, and so can result in significant reduction in the average balancing current that flows. In order to help alleviate this, additional configuration bits are provided which cause the device to slow the measurement loop speed when cell balancing is active. The BQ769x2 device will insert current-only measurements after each voltage and temperature scan loop to slow down voltage measurements and thereby increase the average balancing current.

2 Cell Balancing Circuit Considerations

Cell balancing of a particular cell consists of enabling an integrated FET switch across the cell. The balancing current is determined by value of the input filter resistors selected when using internal balancing. FETs or BJTs can be used to increase the balance current in applications where the internal balancing current may not be sufficient. The next sections will discuss circuit design considerations for internal balancing, external balancing with N-channel FETs, external balancing with P-channel FETs, and external balancing with BJTs. Considerations for power dissipation and timing will also be discussed.

2.1 Internal Cell-Balancing Circuit Design

When one of the internal balance FETs is enabled, the internal FET will pull the pins for that cell together drawing current through the input resistors for that cell. The recommended minimum value of the input filter resistors when using internal balancing is 20 Ω. This value maximizes the balance current while keeping it well within the absolute maximum cell balancing current over the internal FET $R_{DS(ON)}$ range. The maximum recommended value for the input filter resistors is 100 Ω.

The typical internal cell balancing resistance ($R_{DS(ON)}$ for the internal FET) is 25 Ω. For a typical lithium ion cell with a full charge voltage of 4.2 V, this results in a balancing current of approximately 65 mA. This is the DC current if the switch was on continuously, so the average balancing current will be lower. The duty cycle is determined by a multiple factors is discussed in more detail in Section 5.

$I\_Balance = VCell / (2 \times R_n + R_{CB}) = 4.2\ V / (2 \times 20 + 25) \sim= 65\ mA$

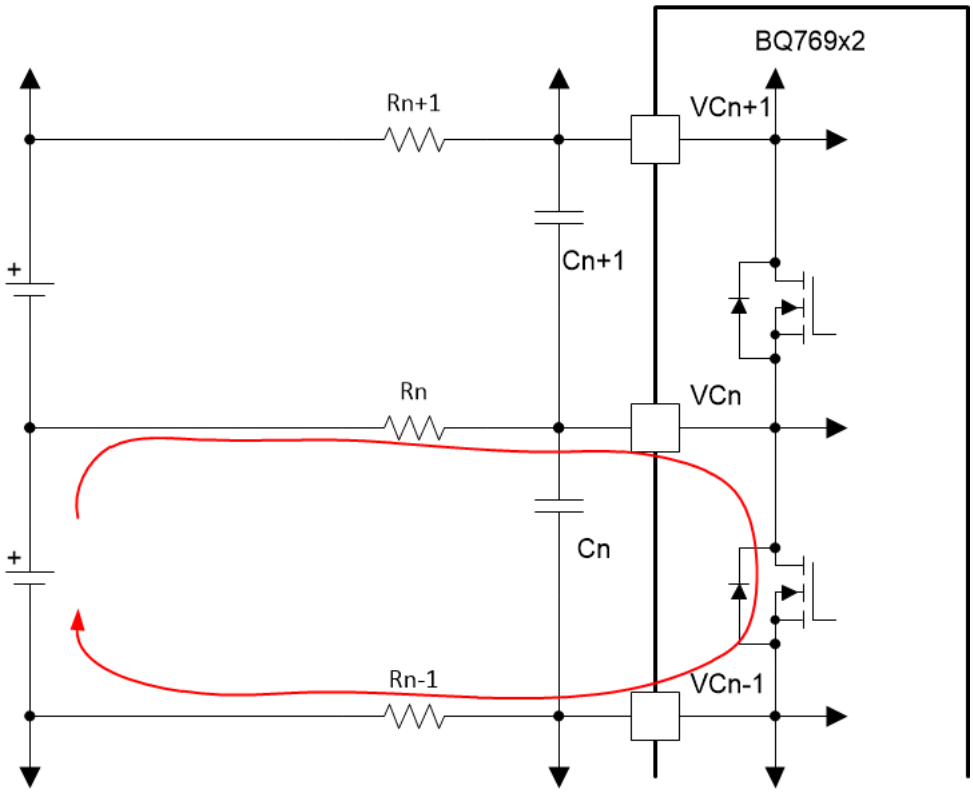

Figure 2-1. Application Circuit for Internal Balancing

For many applications, the internal balancing current for the device is sufficient and additional external components are not required. However, one must consider the power dissipation and the resulting impact on the device temperature. For example 65 mA into 25 Ω results in about 0.1 W. The junction to ambient thermal resistance for the device is 66 °C/W. If 5 cells are balancing at the same time, this can result in a junction temperature rise of 33 °C.

There are multiple ways to avoid excessive power dissipation. The maximum number of cells allowed to balance simultaneously can be limited by setting ***Settings: Cell Balancing Config: Cell Balance Max Cells***. There are also parameters to control when balancing is allowed based on the cell temperature or the internal temperature of the device. These parameters are available to control power dissipation and temperature in autonomous mode. The cell input resistors values can also be increased to reduce balancing current which will also reduce power dissipation.

2.2 External Cell-Balancing Circuit Design Using N-Channel FETs

For applications that need higher cell balancing current, external FETs are often used. When using external FETs, the cell input resistors can be increased to the maximum recommended value of 100 Ω. Increasing the resistor size will help to provide enough voltage across the gate of the FET. In Figure 2-2, as the internal FET is turned on inside the device, the current flowing through R_{n-1} provides the V_{GS} for the external FET.

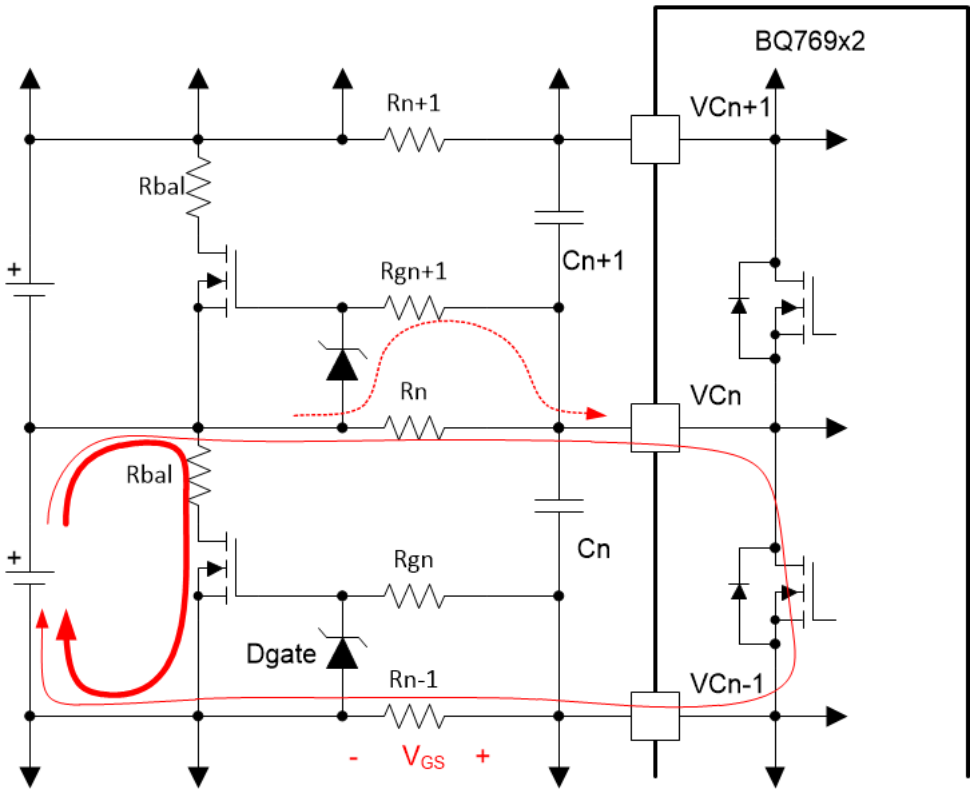

Figure 2-2. Balancing Circuit Using External N-channel FETs

Care must be taken to select an external FET with a low R_{DSON} defined at low V_{GS}. For example, the default balancing minimum voltage defined by the parameter ***Cell Balance Min Cell V*** is 3900 mV. The external FET should have an R_{DSON} defined at or below 3.9V x 100 / (100 + 100 + 25) = 1.73 V.

A Zener diode is needed to protect the external FET gate from pack transients. For example, in the event of a short across the pack in a 10-cell battery, Cell 10 would have approximately 40V across R_n during the event and the opposite transient at the release of the short circuit. The gate voltage should be connected through a resistor to limit the current when the diode conducts. (During normal operation the Zener will not conduct).

For the waveform captured below, the circuit was designed with an R_n of 100 Ω and R_{gn} of 1k Ω. The R_{bal} resistor is set to 50 Ω for a balance current of 80 mA through the external FET at 4V. At this cell voltage, an additional ~16 mA of current flows through the internal FET of the device for a total balancing current of close to 96 mA. An N-channel MOSFET was selected with an R_{DSON} defined for low V_{GS} down to 1.4V.

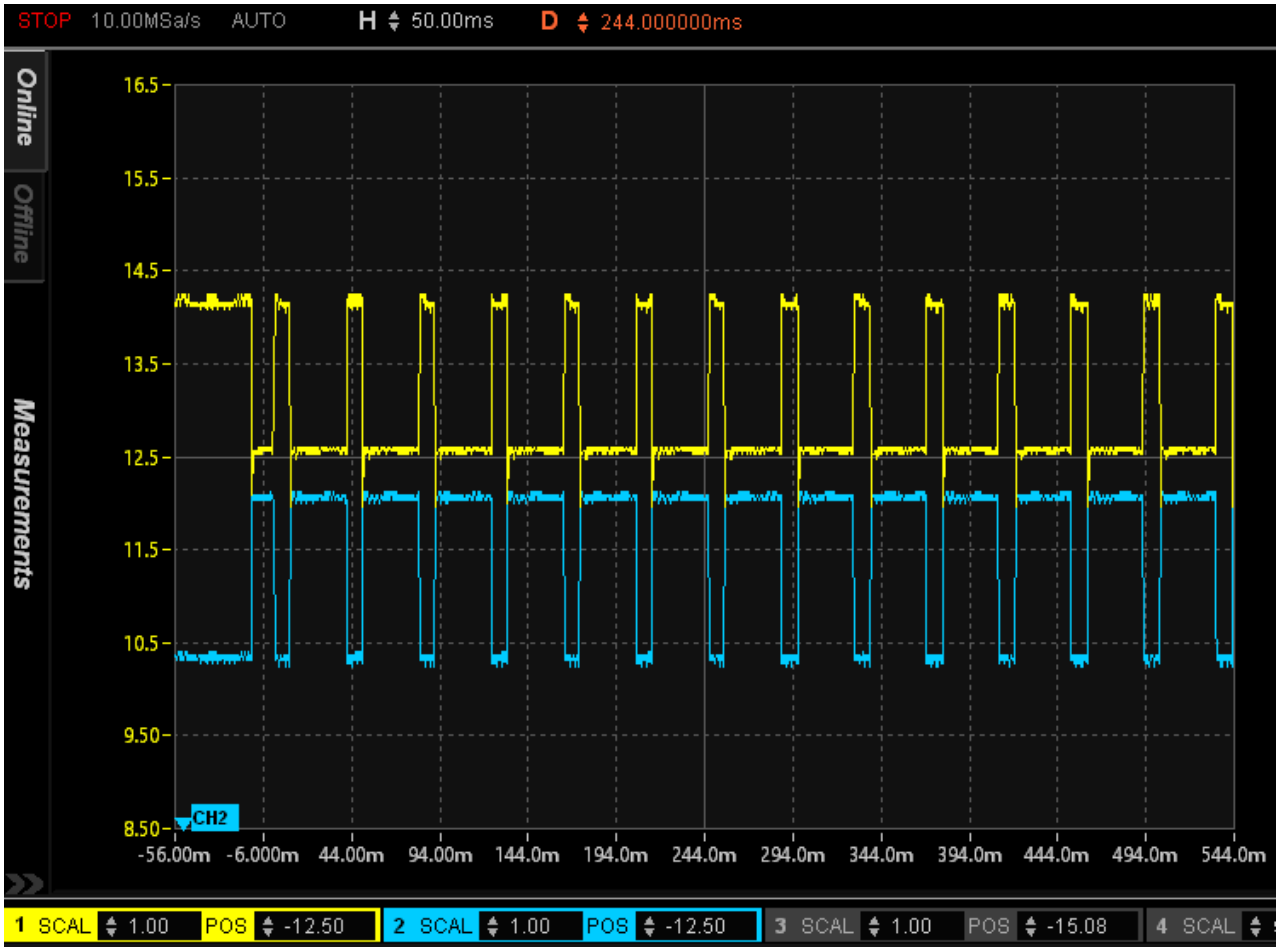

Figure 2-3. BQ76942 Cell Balancing With N-Channel FET, Cell 4 (yellow) = 3.7 V, Cell 3 (blue) = 3.5 V

2.3 External Cell-Balancing Circuit Design Using P-Channel FETs

P-channel FETs can similarly be used for external balancing. When using P-channel FETs, V_{GS} is generated on the top input resistor for each cell.

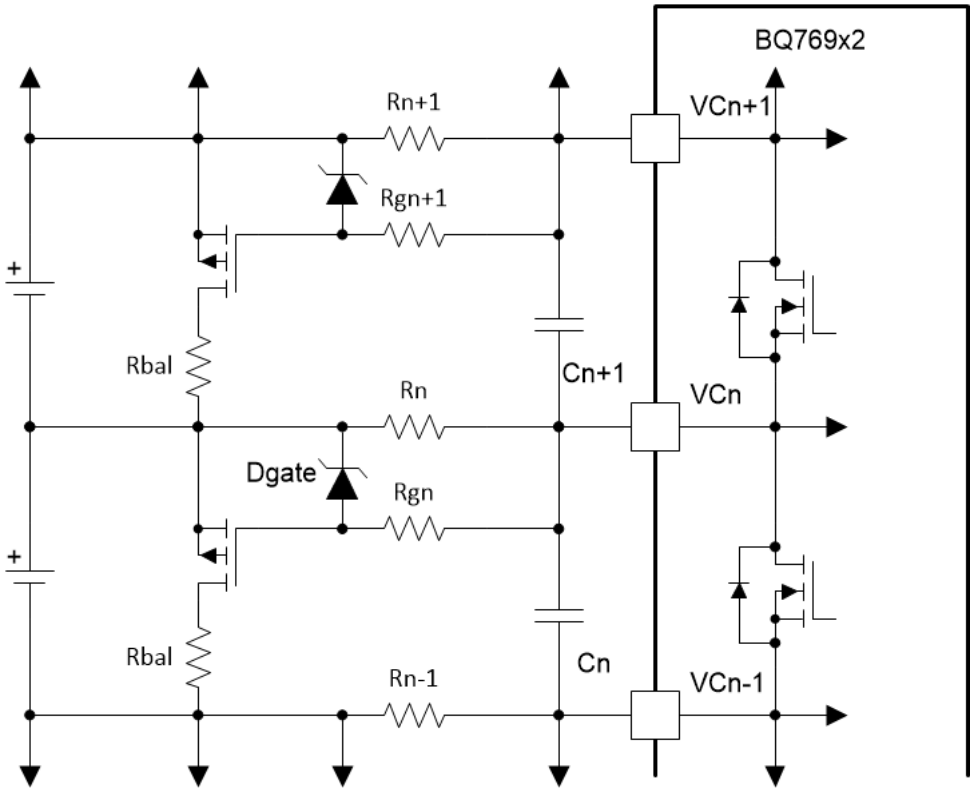

Figure 2-4. Balancing Circuit Using External P-Channel FETs

2.4 External Cell-Balancing Circuit Design Using BJTs

External FETs work well for most applications with typical 4.2 V lithium ion cells since balancing is most commonly done at higher voltages during charge. For applications that need higher balancing current than the internal balancing can provide but also need to balance at lower cell voltages, external BJTs may be considered. The balancing current for an external BJT can be controlled by selecting the appropriate balance resistor (R_{bal}) and base resistor (R_{bn}). In Figure 2-5, as the internal FET is turned on inside the device, the current flowing through R_{bn} puts the NPN transistor into saturation.

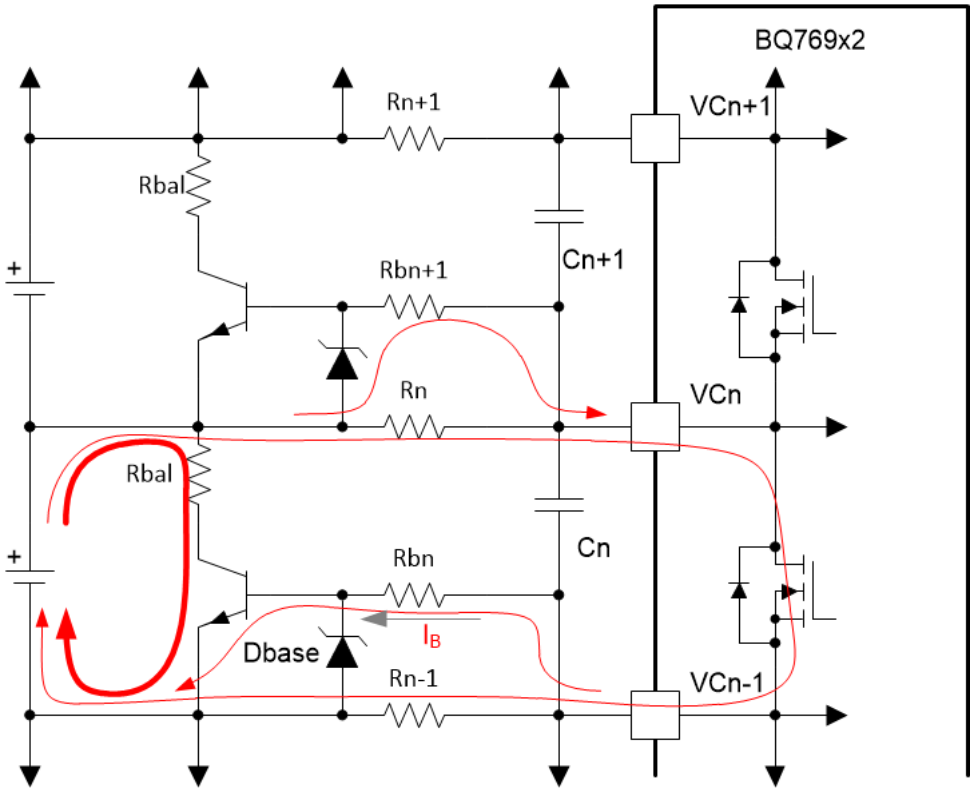

Figure 2-5. Balancing Circuit Using External BJTs

A Zener diode is also used in this circuit to protect from pack transients similar to the FET circuits. A standard diode is also suitable to use instead of a Zener when using BJTs because it is the forward voltage of the Zener that protects the transistor. The base-emitter diode (or emitter-base diode for a PNP) will conduct in the reverse direction which will prevent the Zener from conducting.

For the waveform captured below, the circuit was designed with an R_n of 100 Ω and R_{gn} of 240 Ω. The R_{bal} resistor is set to 50 Ω for a balance current of 80 mA through the BJT at 4 V. At this cell voltage, an additional ~22 mA of current flows through the internal FET of the device for a total balancing current of close to 102 mA. An NPN transistor was selected with hFE of 30 at IC = 100 mA. With this component selection, I_B is approximately 4.5 mA when the cell voltage is 4 V.

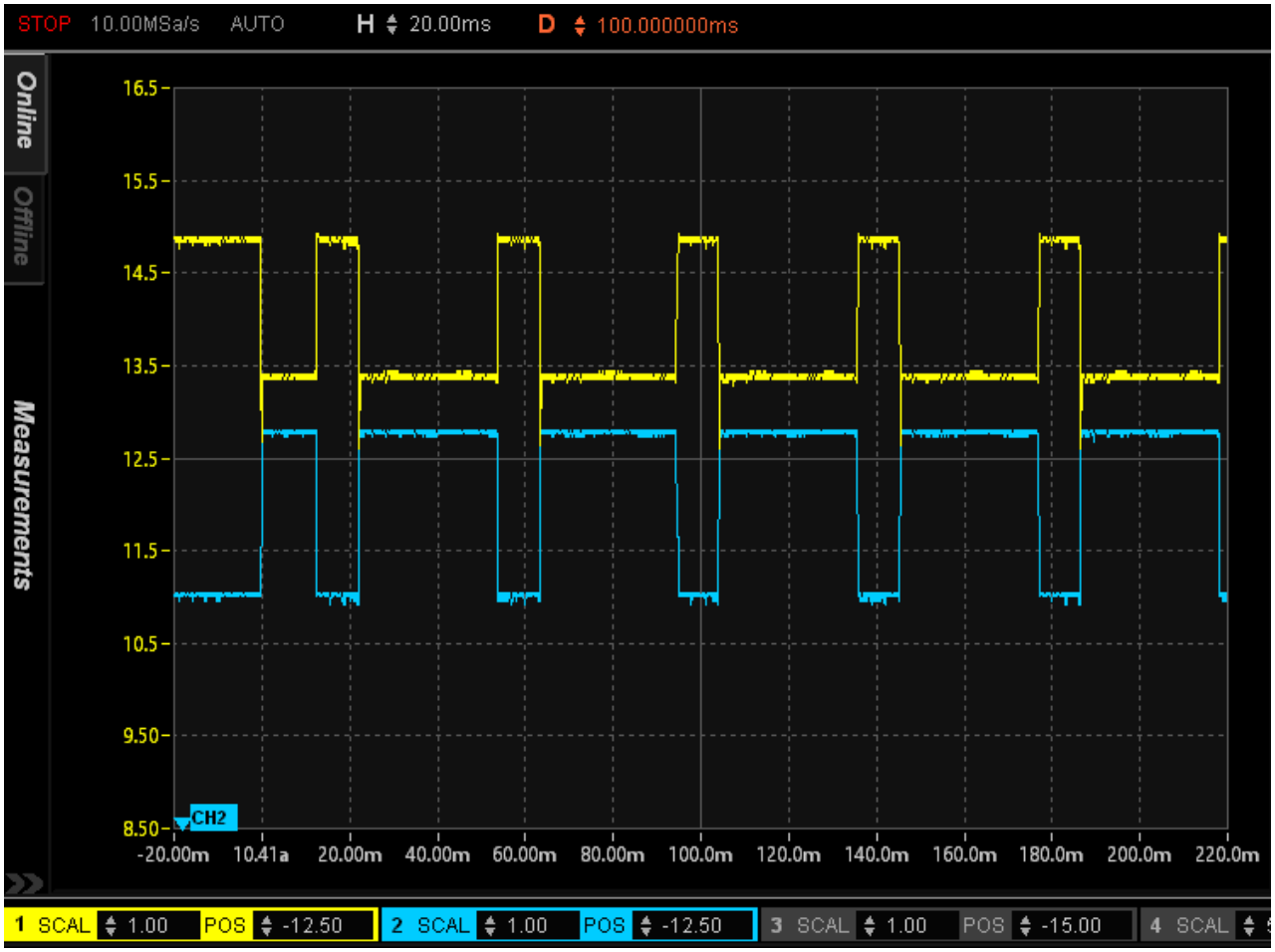

Figure 2-6. BQ76942 Cell Balancing With NPN BJT, Cell 4 (yellow) = 3.8 V, Cell 3 (blue) = 3.7 V

2.5 Voltage Measurement Accuracy During Balance

Voltage measurements are generally very accurate while cell balancing is active, but there are some important factors to be aware of and to consider in the system design. Two things that should be considered are the time constant of the selected cell input filter components and the IR drop across the top cell input resistor that may impact the accuracy of the top cell measurement.

Time Constant of Filter Components: Voltage accuacy deviation during balancing should be minimal when the external cell input resistance and input capacitance are selected within the datasheet recommended values. Cell voltage is meausured during a 3ms interval and a small RC time constant will have very little impact. If larger component values are selected resulting in a large time constant, the voltage may not settle sufficiently during the mesaurement windows and a lower voltage will be measured.

IR Drop Across Top Cell Input Resistor: When cell balancing is active, there is additional current flow into the top cell input (VC16 for the BQ76952 for example), for each cell that is balancing. This additional current flow results in a small IR drop across the cell input resister of the top cell which results in a lower voltage reading during balancing. For example, if 8 cells are balancing simultaneously and 20 cell input resistors are used, this would result in a VC16 voltage measurement of 5mV lower than the actual cell voltage (35 uA * 20 Ω * 8 cells). The IR drop can be reduced by limiting the maximum number of cells allowed to balance simultaneously (***Settings: Cell Balancing Config: Cell Balance Max Cells***). The IR drop affects only the top cell measurement. If larger cell input resistors are used (like in the case using external balancing transistors where the maximum input resistor value of 100 Ω is advised), it may be good to use a smaller input resistor like 20 Ω on the VC16 pin to reduce the IR drop while using 100 Ω on the other pins.

Measurement Disturbance During COV/CUV Checks: Another potential cause of voltage measurement error during balancing is a disturbance to the voltage during periodic over-voltage and under-voltage checks. Every one second, cell balancing is disabled for ~20 ms to all COV and CUV checks to run on all cells. This disabling of the balancing is not synchronized to the cell measurement timing, so occasionally this can occur during the measurement of a nearby cell. This event generates a transient response that couples through the cell RC input network and can result in a measurement error of several mV lower than the actual voltage. This event occurs with low probability so it may typically only be observed once every several hundred seconds. One possible solution to work around this would be to filter a single measurement that differs from the measurement immediately before and after.

3 Stand-Alone Balancing Algorithm and Settings

The BQ769x2 devices have cell balancing disabled and autonomous mode is selected by default. Figure 3-1 shows the Balancing Configuration register in the Battery Management Studio software. To enable stand-alone cell balancing, the ***[CB_CHG]*** or ***[CB_RLX]*** bits can be set.

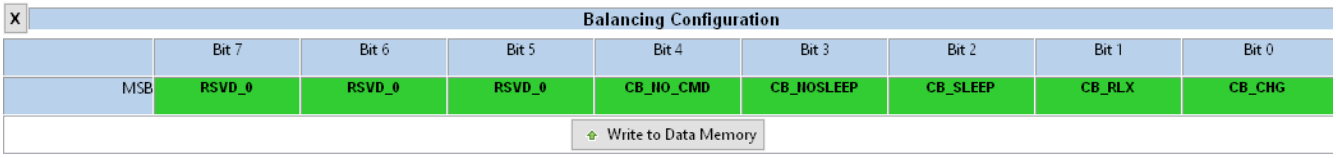

Figure 3-1. Balancing Configuration Register

Charge versus Relax - autonomous balancing can be allowed during charging by ***[CB_CHG]***, or in a relaxed condition by setting ***[CB_RLX]***, or both. If ***[CB_CHG]*** is set, autonomous balancing is allowed while the CC1 Current is above ***Settings:Current Thresholds:Chg Current Threshold***. If ***[CB_RLX]*** is set, autonomous balancing is allowed while the current is below ***Settings:Current Thresholds:Chg Current Threshold*** and above the negative of ***Settings:Current Thresholds:Dsg Current Threshold***. The device evaluates the conditions for continuing balancing every ***Cell Balance Interval***. For example, if the device is configured to avoid balancing during charge, and while balancing the pack begins charging, balancing will continue until the interval timer expires before it is disabled.

There are multiple parameters shown in the Battery Management Studio Data Memory window below. The temperature parameters ***Min Cell Temp***, ***Max Cell Temp***, and ***Max Balance Current*** set allowable temperature limits for cell balancing. The device will disable balancing (both autonomous and host-controlled) if the temperatures violate the limits set by these parameters. ***Cell Balance Max Cells*** limits the number of cells that can be balanced simultaneously in autonomous mode (this parameter is ignored in host-controlled mode). This can be very helpful to limit the power dissipation during balancing.

Cell Balancing Config		
Balancing Configuration	00	Hex
Min Cell Temp	-20	°C
Max Cell Temp	60	°C
Max Internal Temp	70	°C
Cell Balance Interval	20	s
Cell Balance Max Cells	1	s
Cell Balance Min Cell V (Charge)	3900	mV
Cell Balance Min Delta (Charge)	40	mV
Cell Balance Stop Delta (Charge)	20	mV
Cell Balance Min Cell V (Relax)	3900	mV
Cell Balance Min Delta (Relax)	40	mV
Cell Balance Stop Delta (Relax)	20	mV

Figure 3-2. Default Cell Balancing Config Settings in BQStudio

If autonomous balancing during charge is enabled, the device will allow balancing if the minimum cell voltage is above ***Cell Balance Min Cell V (Charge)*** and the difference between the maximum and minimum cell voltages is greater than ***Cell Balance Min Delta (Charge)***. Similarly, if autonomous balancing during relax is enabled, the device will allow balancing if the minimum cell voltage is above ***Cell Balance Min Cell V (Relax)*** and the difference between the maximum and minimum cell voltages is greater than ***Cell Balance Min Delta (Relax)***. While balancing during relax, when the device re-evaluates the cell status at the end of each timer interval, it will cease balancing if all cell voltages are within ***Cell Balance Stop Delta (Relax)*** of the minimum cell voltage. This ***Cell Balance Stop Delta*** reduces the risk of overbalancing a higher voltage cell to slightly below the minimum voltage cell, and thereby slowly draining the pack. Operation while balancing during charge is similar, instead using the ***Cell Balance Stop Delta (Charge)*** configuration value. The ***Cell Balance Stop Delta*** parameters should be set to a slightly lower level than the ***Cell Balance Min Delta*** parameters, then the device will have a hysteresis that delays restarting balancing until the level of imbalance again exceeds the higher ***Cell Balance Min Delta*** level.

Let's look at a simple example with 4 cells where cell balancing is enabled during charge (***[CB_CHG]*** is set). If ***Cell Balnance Min Cell V (Charge)*** = 3900 mV, ***Cell Balance Min Delta (Charge)*** = 40 mV, and ***Cell Balance Stop Delta (Charge)*** = 20 mV. As the cells charge, we reach a point where Cell1 = 3900 mV, Cell2 = 3940 mV, Cell 3 = 3910 mV, and Cell 4 = 3930 mV. At this point, balancing will start because Cell2 is above the ***Cell Balance Min Delta*** and all cells are above the ***Cell Balnance Min Cell V***. Once balancing starts, Cell 4 will also balance because it is above the ***Cell Balance Stop Delta***.

NORMAL versus SLEEP Mode - The BQ769x2 device can also be configured to avoid autonomous balancing while in SLEEP mode by clearing the ***Balancing Configuration[CB_SLEEP]*** configuration bit. The device can also be prevented from entering SLEEP mode while balancing if the ***Balancing Configuration[CB_NOSLEEP]*** bit is set. The functionality based on these bits is described in the table below.

Table 3-1. Cell Balancing CB_SLEEP and CB_NOSLEEP Configuration Settings

CB_SLEEP	CB_NOSLEEP	Description
0	0	Cell balancing is not allowed to occur while in SLEEP mode. If balancing were active when the device entered SLEEP mode, balancing would stop at the end of the present ***Cell Balance Interval*** and could not restart until the device returned to NORMAL mode.
0	1	This setting is not allowed. When CB_NOSLEEP is set, CB_SLEEP should also be set.
1	0	Cell balancing is allowed to begin and continue while the device is in SLEEP mode
1	1	If the device is in SLEEP mode and cell balancing is deemed necessary, the device will exit SLEEP mode to begin balancing. The device is prevented from re-entering SLEEP mode while balancing is active.

4 Considerations for a Host-Balancing Algorithm

CAUTION
Improper setting of the cell-balancing control bits may damage the IC.

Host-controlled balancing can be controlled using specific subcommands sent by the host, these subcommands are also accessible in SEALED mode, to avoid the need for the pack to be unsealed in operation in order to initiate balancing. If host-controlled balancing will not be used, access to these subcommands can be disabled by setting the ***Balancing Configuration[CB_NO_CMD]*** configuration bit. The subcommands used by the host to control cell balancing are described below.

Table 4-1. Host-Controlled Cell Balancing Subcommands

Subcommand	Description
0x0083 CB_ACTIVE_CELLS()	When read, reports a bit mask of which cells are being actively balanced. When written, starts balancing on the specified cells. Write 0x0000 to turn balancing off.
0x0084 CB_SET_LVL()	When written with a 16-bit cell voltage threshold in mV, the device begins balancing one or more of the highest voltage cells if above the written threshold. When read, returns the threshold.

The device also returns status information regarding how long cells have been balanced through the subcommands described below. When writing to the host-controlled balancing commands, it is necessary to write the checksum and length to registers 0x60/0x61 for the values to be written successfully. Refer to the TRM or BQ769x2 Software Development Guide for information on writing the checksum and length.

Table 4-2. Cell Balancing Status Subcommands

Subcommand	Description
0x0085 CBSTATUS1()	When read, returns the 16-bit time in seconds that balancing has been active.
0x0086 CBSTATUS2()	When read, returns a block containing the 32-bit cumulative balancing times in seconds for each of cells 1 - 8. These values will reset if a device reset occurs, or the device enters CONFIG_UPDATE mode.
0x0087 CBSTATUS3()	When read, returns a block containing the 32-bit cumulative balancing times in seconds for each of cells 9 - 16. These values will reset if a device reset occurs, or the device enters CONFIG_UPDATE mode.

When host-controlled balancing is initiated using the subcommands above, the device starts a timer and will continue balancing until the timer reaches a value of ***Settings:Cell Balancing Config:Cell Balance Interval***, or a new balancing subcommand is issued (which resets the timer). This is included as a precaution, in case the host processor initiated balancing but then stopped communication with the BQ769x2 device, so that balancing would not continue indefinitely.

Note on Adjacent Cell Balancing: Care should be taken when using host-controlled balancing to ensure the power dissipation is at safe levels. Adjacent cell balancing is not possible in autonomous mode, but can be done in host-controlled mode. Adjacent cell balancing should only be used is special cases after careful consideration. Care must be taken to not exceed the abs max 100 mA cell balancing current limit or the abs max VC0 input voltage limit.

5 Timing Information

Due to the current that flows into the cell input pins on the BQ769x2 device while balancing is active, the measurement of cell voltages and evaluation of cell voltage protections by the device is modified during balancing. Balancing is temporarily disabled during the regular measurement loop while the actively balanced cell is being measured by the ADC, as well as when the cells immediately adjacent to the active cell are being measured. Similarly, balancing on the top cell is disabled while the stack voltage measurement is underway. This occurs on every measurement loop, and so can result in significant reduction in the average balancing current that flows. In order to help alleviate this, the ***Settings:Configuration:Power Config[CB_LOOP_SLOW_1:0]*** configuration bits cause the device to slow the measurement loop speed when cell balancing is active, as shown below. The BQ769x2 devices will insert current-only measurements after each voltage and a temperature scan loop to slow down voltage measurements and thereby increase the average balancing current.

Table 5-1. Cell Balancing Loop Slow-Down Settings

CB_LOOP_SLOW_1	CB_LOOP_SLOW_0	Description
0	0	Measurement loop runs at full speed during balancing.
0	1	Measurement loop runs at half speed during balancing.
1	0	Measurement loop runs at quarter speed during balancing.
1	1	Measurement loop runs at eighth speed during balancing.

In order to avoid the balancing current causing a protection alert or fault, the device modifies the timing on the CUV check on an actively balanced cell and the COV checks on adjacent cells, disabling balancing briefly every 1-sec to allow these checks to occur. If a CUV or COV alert is detected at the 1-sec check, balancing is immediately disabled. Note: the device will therefore have a different delay (≈1-sec) in triggering a CUV or COV alert or fault on these cells while balancing is active. Timing for CUV and COV on other cells besides these being actively balanced or adjacent are not modified.

The device includes an internal die temperature check, to disable balancing if the die temperature exceeds a programmable threshold. However, the customer should still carefully analyze the thermal effect of the balancing on the device in system. Based on the planned ambient temperature of the device during operation and the thermal properties of the package, the maximum power should be calculated that can be dissipated within the device and still ensure operation remains within the recommended operating temperature range. The cell balancing configuration can then be determined such that the device power remains below this level by limiting the maximum number of cells that can be balanced simultaneously, or by reducing the balancing current of each cell by appropriate selection of the external resistance in series with each cell.

While autonomous cell balancing is underway, the conditions related to continuing or stopping balancing are re-evaluated at each ***Cell Balance Interval***. During SLEEP mode, this re-evaluation is done using the data available at the time, which is only updated every ***Power:Sleep:Voltage Time***. Thus, there may be some delay related to these settings before balancing is changed based on the data.

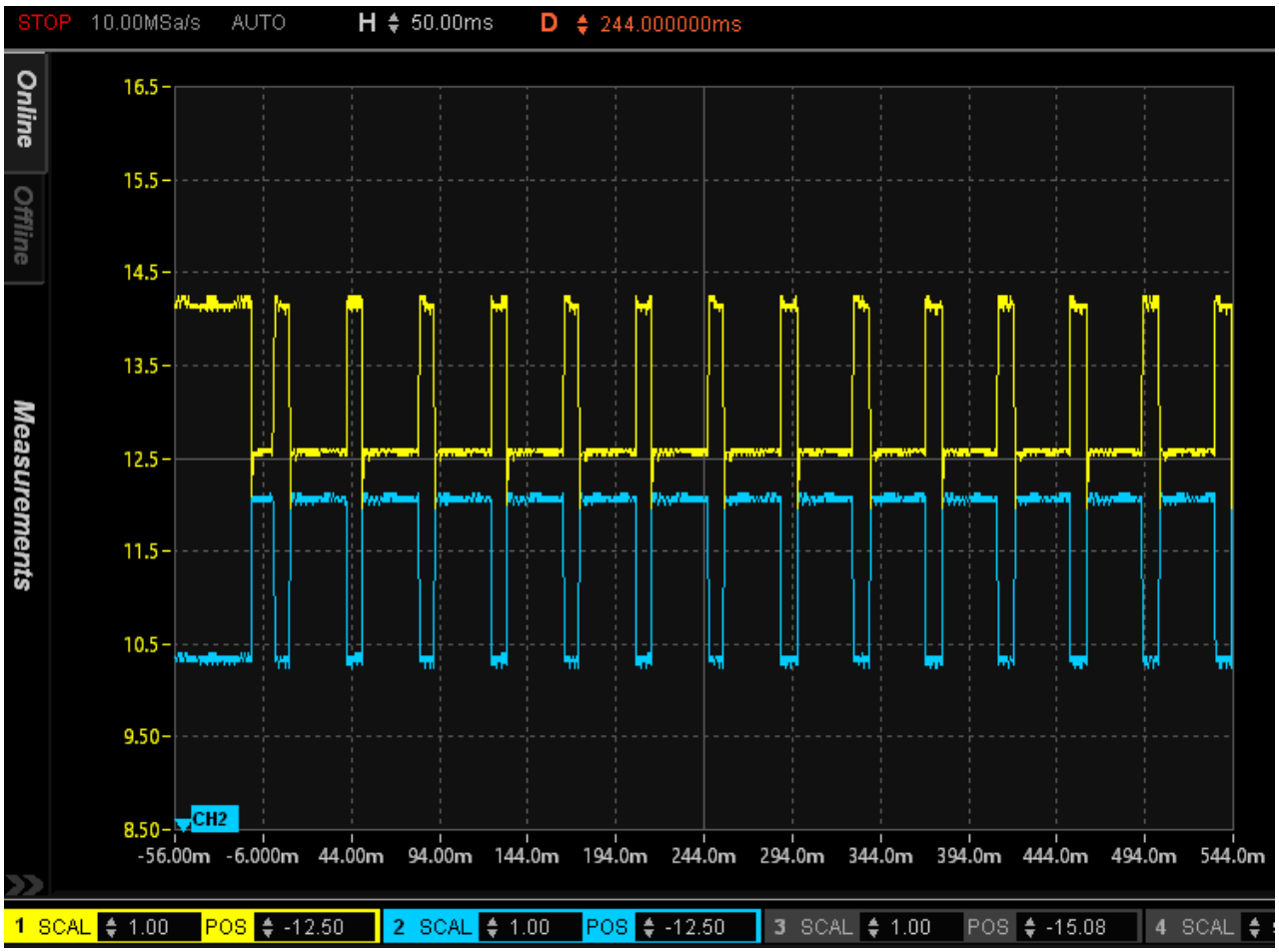

Figure 5-1. Cell Balancing With CB_SLOW = 0x00, Cell 4 (yellow) = 3.7 V, Cell 3 (blue) = 3.5 V

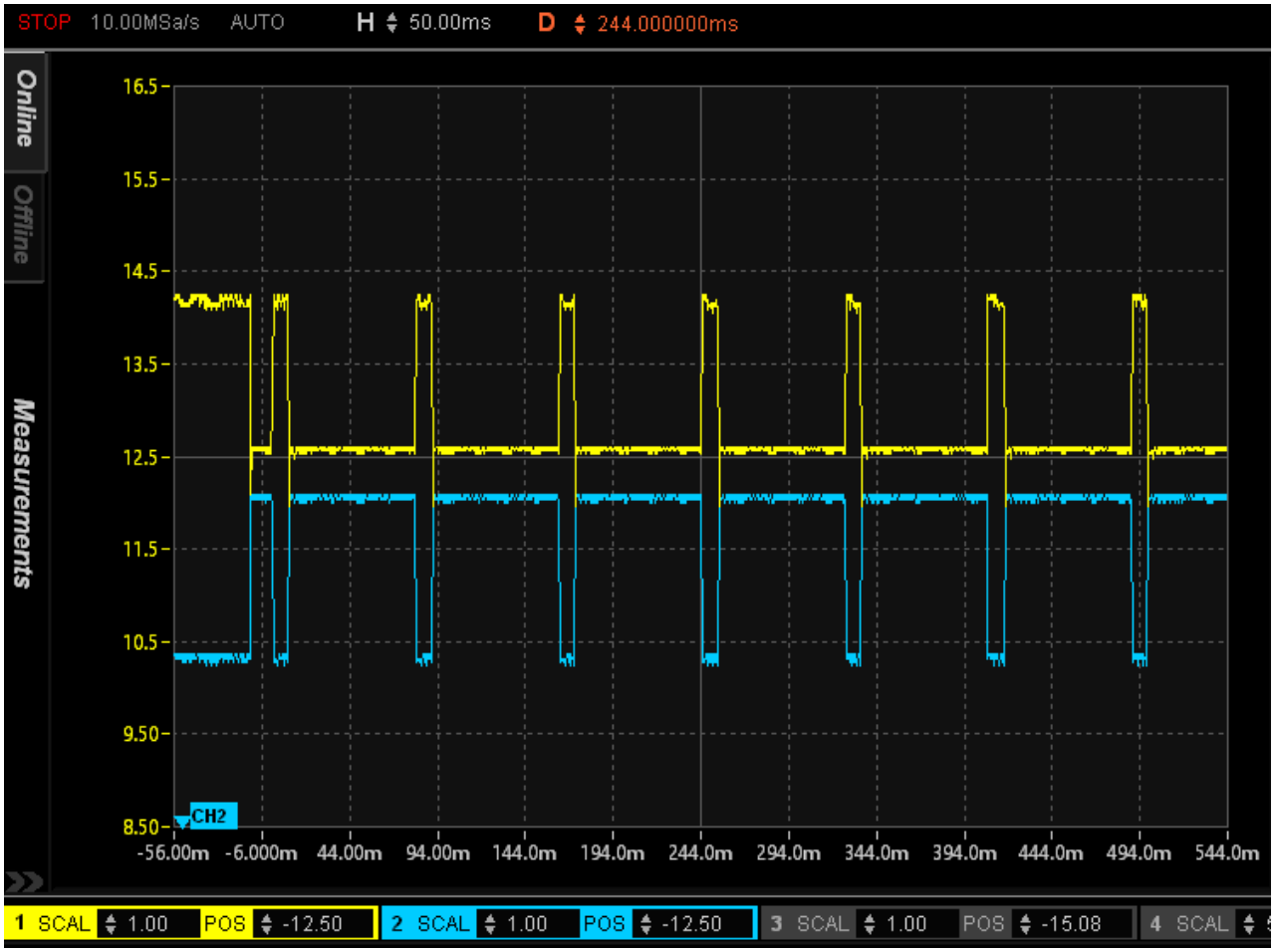

Figure 5-2. Cell Balancing With CB_SLOW = 0x01, Cell 4 (yellow) = 3.7 V, Cell 3 (blue) = 3.5 V

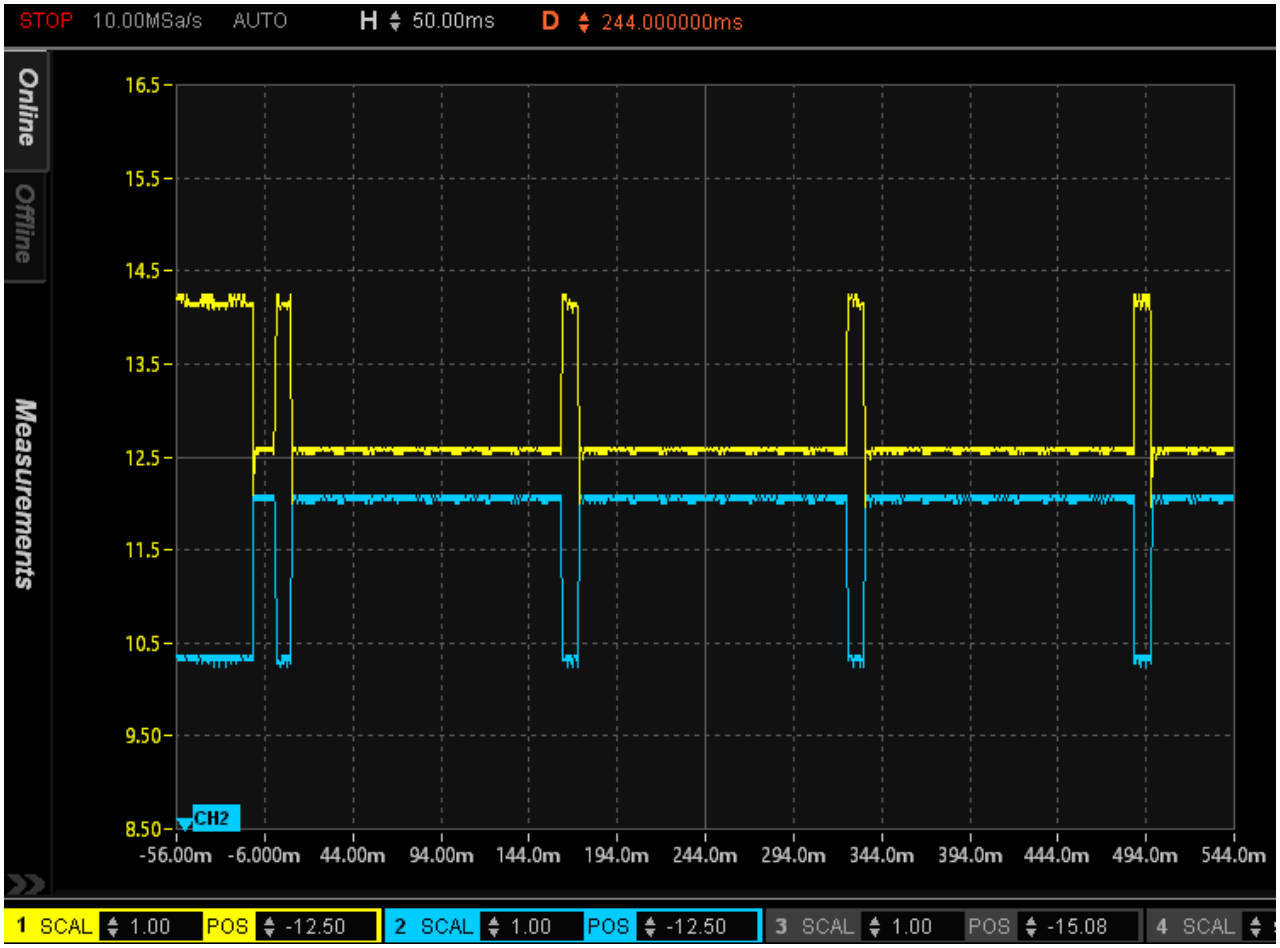

Figure 5-3. Cell Balancing With CB_SLOW = 0x10, Cell 4 (yellow) = 3.7 V, Cell 3 (blue) = 3.5 V

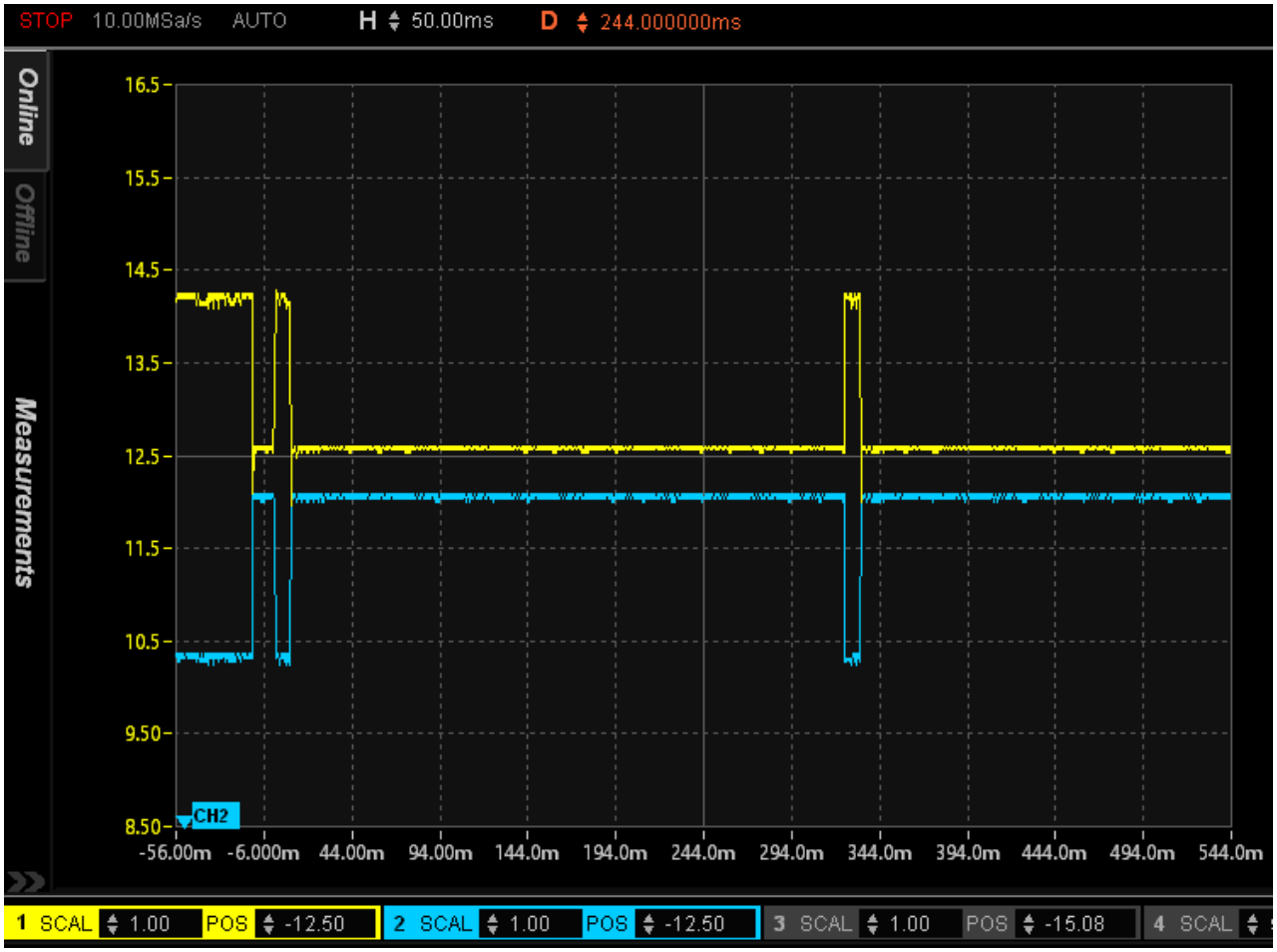

Figure 5-4. Cell Balancing With CB_SLOW = 0x11, Cell 4 (yellow) = 3.7 V, Cell 3 (blue) = 3.5 V

6 Debugging Common Issues With Cell Balancing

6.1 Using a Resistor Divider as a Cell Simulator

When testing the cell balancing feature with a power supply and resistor divider to simulate cells, this will often trigger the over-voltage protection which may be observed in the ***Safety Alert A*** register. This is because the resistor divider will pull on the voltages of the other cell inputs when cell balancing starts on one of the cells. This causes the voltages to become instable which triggers the over-voltage condition. Any time an over-voltage condition occurs, cell balancing is immediately disabled.

The best way to test the cell balancing feature is with real cells. One of the cells can be charged slightly higher or discharged slightly lower to initiate cell balancing. If real cells are not available, another option is to use a resistor divider with a second power supply connected across one of the cells. For example, if the main supply and resistor divider are set to provide 3.9 V on each cell input, a second supply set to 3.9 V can be connected across one of the cell inputs. Then the supply can be adjusted to 3.95 V to enable cell balancing.

7 References

- Texas Instruments, *BQ76952 Technical Reference Manual*
- Texas Instruments, *BQ76942 Technical Reference Manual*
- Texas Instruments, *BQ769142 Technical Reference Manual*

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (October 2021) to Revision A (February 2022)	Page
• Update was made in the Abstract of this document	1
• Updated the numbering format for tables, figures and cross-references throughout the document	2
• Update was made in Section 2.4	7
• Update was made in Section 2.5	8
• Update was made in Section 4	10
• Added new Section 6	15

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