Project Report

Title TAPERED LINES Sec 450

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Submitted to

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Preface

This report is prepared as part of the Microwave Engineering (01205322) course. The objective of this report is to present the design, simulation, implementation, and analysis of a symmetric two-port tapered microstrip line transformer, which focuses on impedance matching techniques in microwave frequency applications. The project covers the theoretical background, design methodology, simulation procedures, and the results obtained from both electromagnetic simulation and practical fabrication.

The author would like to express sincere gratitude to Asst. Prof. Dr.Denchai Worasawate ,Ph.D. for his valuable knowledge, guidance, and continuous support throughout the course.

Furthermore, the author hopes that this report will be beneficial to students and readers who are interested in microwave engineering, particularly in the design and implementation of tapered transmission line transformers. Any suggestions, comments, or feedback for improvement are warmly welcomed, and the author apologizes in advance for any unintentional errors or omissions in this report.

Prepared by

~~Group 1~~

Our group

Project Procedures

This project was carried out by following a structured microwave engineering design workflow, starting from the problem definition and ending with physical PCB implementation. The complete process includes conceptual design, circuit-level modeling, electromagnetic simulation, transmission-line realization, PCB layout, and preparation for fabrication and measurement.

1. Project Specification and Problem Definition

The project requirement, shown in **Figure 1**, specifies the design of a symmetric two-port tapered-line transformer. At Port 1, a taper converts a 50-Ω impedance to 100-Ω. Instead of terminating the line with a 100-Ω load, an identical mirrored taper is connected, which transforms the impedance back from 100-Ω to 50-Ω at Port 2. As a result, the overall structure can be represented as a **50 Ω ⟶ 100 Ω ⟶ 50 Ω** network.

The most important design constraint is that the **first null of the reflection coefficient (S_{11})** must occur at **3 GHz**, indicating good impedance matching at the target frequency.

Class project:
"The structure is a symmetric two-port tapered-line transformer. At Port 1, a taper converts 50 Ω to 100 Ω. Instead of a 100-Ω load, the line is connected to another identical taper that converts the 50-Ω impedance at Port 2 up to 100 Ω. The two tapers meet at their 100-Ω ends, so the overall network is a 50-Ω–to–100-Ω taper cascaded with a 100-Ω–to–50-Ω taper."
The 1st null of S11 is at 3GHz.

Figure 1: Project specification showing the symmetric tapered-line transformer structure.

2. Hanning-Windowed Multisection Transmission-Line Design

After understanding the specification, a multisection tapered transmission-line approach was selected instead of a stepped transformer. A tapered structure provides a gradual impedance transition, significantly reducing reflections and improving bandwidth.

To achieve controlled sidelobe behavior and smooth impedance variation, the multisection transmission-line network was designed to behave like a **Hanning-windowed transformer**. The Hanning window is commonly used in signal processing to suppress sidelobes, and the same concept can be applied to microwave impedance matching by properly shaping the impedance profile along the line.

In this design, the characteristic impedance increases gradually from 50 Ω toward 100 Ω near the center of the structure and then decreases symmetrically back to 50 Ω. The impedance values follow an exponential taper modified by Hanning weighting, ensuring smoother transitions near the input and output ports and stronger variation near the center.

Element	Nodes	Description
Net	1 21	Main Network
TLIN	1 2	Z=50.8 E=36.0 F=4.0
TLIN	2 3	Z=53.25 E=36.0 F=4.0
TLIN	3 4	Z=58.3 E=36.0 F=4.0
TLIN	4 5	Z=65.85 E=36.0 F=4.0
TLIN	5 6	Z=74.0 E=36.0 F=4.0
TLIN	6 7	Z=82.35 E=36.0 F=4.0
TLIN	7 8	Z=89.9 E=36.0 F=4.0
TLIN	8 9	Z=95.5 E=36.0 F=4.0
TLIN	9 10	Z=98.45 E=36.0 F=4.0
TLIN	10 11	Z=99.65 E=36.0 F=4.0
TLIN	11 12	Z=99.65 E=36.0 F=4.0
TLIN	12 13	Z=98.45 E=36.0 F=4.0
TLIN	13 14	Z=95.5 E=36.0 F=4.0
TLIN	14 15	Z=89.9 E=36.0 F=4.0
TLIN	15 16	Z=82.35 E=36.0 F=4.0
TLIN	16 17	Z=74.0 E=36.0 F=4.0
TLIN	17 18	Z=65.85 E=36.0 F=4.0
TLIN	18 19	Z=58.3 E=36.0 F=4.0
TLIN	19 20	Z=53.25 E=36.0 F=4.0
TLIN	20 21	Z=50.8 E=36.0 F=4.0

Figure 2: Multisection transmission-line impedance profile designed to behave as a Hanning-windowed transformer.

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3. Circuit-Level Simulation and Ideal Transformer Verification

Once the Hanning-windowed multisection impedance profile was defined, the circuit-level model was constructed using a Sonnet netlist. Each section was modeled using a TLIN element with a specific characteristic impedance and a short electrical length.

The reflection coefficient $|S_{11}|$ was simulated to verify that the multisection network behaves similarly to an ideal Hanning-windowed transformer. The simulation results show a smooth reflection response with suppressed sidelobes and a **first null occurring at approximately 3 GHz**, satisfying the project requirement.

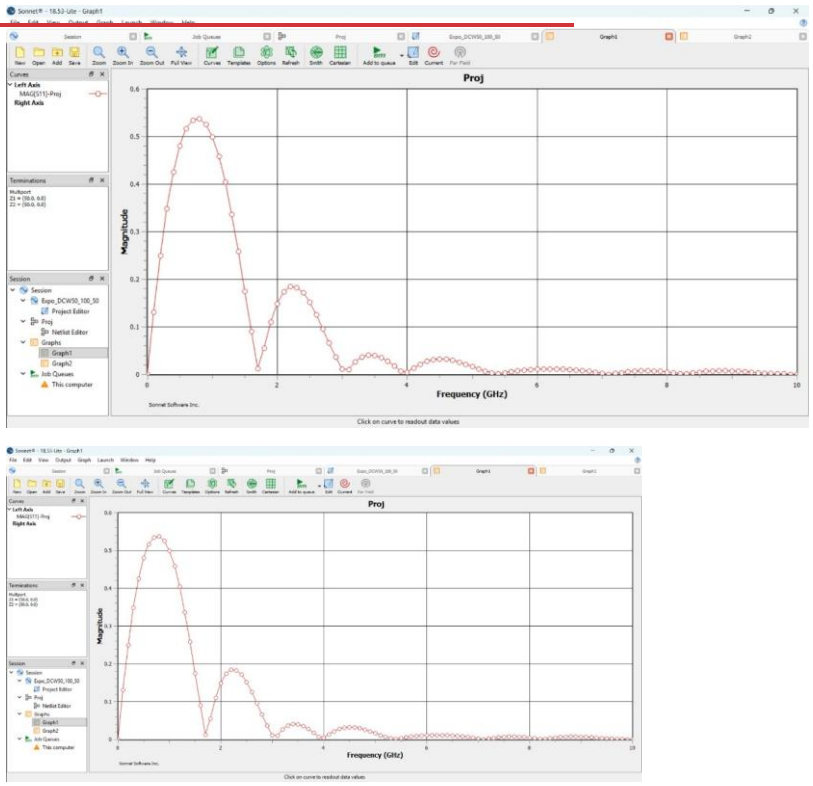


Figure 3: Circuit-level Sonnet simulation showing $|S_{11}|$ response consistent with an ideal Hanning-windowed transformer.

4. Conversion from TLIN Model to Microstrip Implementation

After confirming correct behavior at the circuit level, the TLIN parameters (characteristic impedance Z, electrical length E, and frequency F) were converted into a physical microstrip implementation. This step is necessary to realize the design on a practical PCB.

Using the TXLINE tool, each TLIN section was translated into a corresponding microstrip line based on the chosen substrate parameters. An FR-4 substrate was selected with a relative permittivity of approximately 4.4, substrate thickness of 1.6 mm, and copper thickness of 0.035 mm.

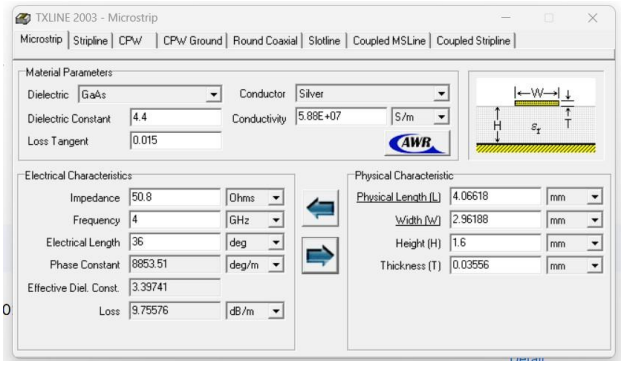


Figure 4: TLIN-to-microstrip conversion using TXLINE.

5. Calculation of Physical Length and Width of Each Section

TXLINE was used to calculate the **physical length and width** of each microstrip section corresponding to the designed characteristic impedance values. Lower-impedance sections resulted in wider microstrip traces, while higher-impedance sections resulted in narrower traces.

Each section was assigned an electrical length of **36 degrees at 4 GHz**, which is sufficiently short to approximate a continuous taper while keeping the total number of sections manageable.

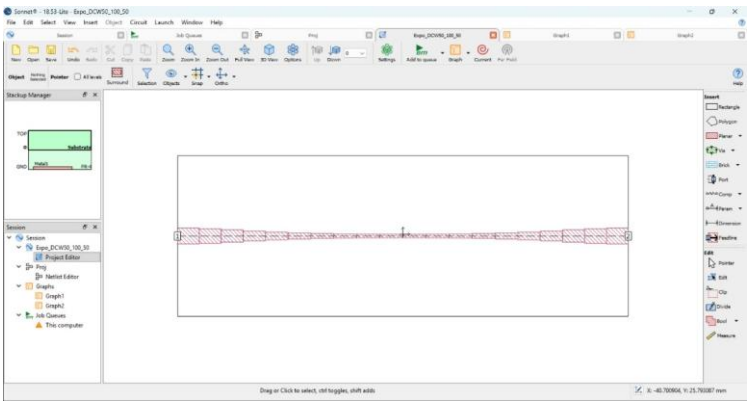
1	4.06618	2.96188
2	4.08282	2.73028
3	4.1154	2.3196
4	4.16002	1.83576
5	4.20325	1.43691
6	4.24259	1.12238
7	4.2743	0.898954
8	4.2959	0.762527
9	4.30675	0.699094
10	4.31107	0.674795
11	42.05828	15.44218
12	LENGTH	WIDTH

Figure 5: Calculated physical length and width of each microstrip section.

6. Electromagnetic Layout in Sonnet

Using the calculated dimensions, the complete tapered microstrip structure was drawn in Sonnet's EM layout environment. The layout preserves symmetry about the center of the structure and accurately represents the Hanning-weighted impedance profile using discrete microstrip sections.

A full electromagnetic simulation was performed to account for fringing fields, coupling, and parasitic effects that are not captured in circuit-level models.



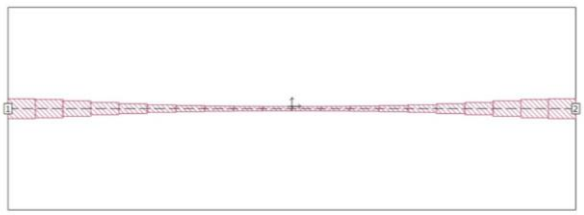


Figure 6: Full electromagnetic layout of the symmetric tapered microstrip transformer in Sonnet.

7. Export to EasyEDA and PCB Implementation

After completing EM verification, the layout was exported to EasyEDA for PCB design. The PCB layout includes SMA connectors at both ports, a continuous ground plane on the bottom layer, and a symmetric tapered microstrip line on the top layer.

Special care was taken to maintain symmetry, ensure smooth transitions between sections, and avoid sharp corners to improve manufacturability and RF performance.

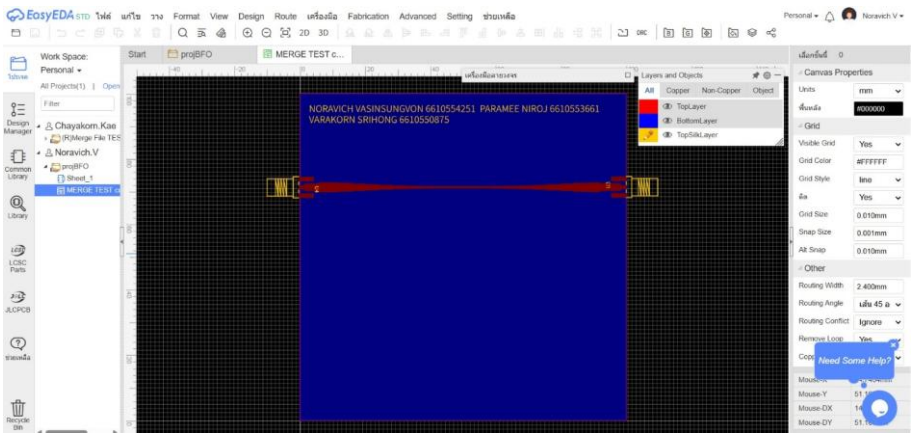


Figure 7: PCB layout of the symmetric tapered transformer implemented in EasyEDA.

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8. Final PCB Simulation and Fabrication Preparation

The final PCB design was simulated in its physical form to verify real-world behavior. The design was then prepared for fabrication by generating Gerber files suitable for a standard two-layer FR-4 manufacturing process.

The fabricated boards are intended for experimental verification using a Vector Network Analyzer (VNA) to measure S-parameters and confirm agreement with simulation results.

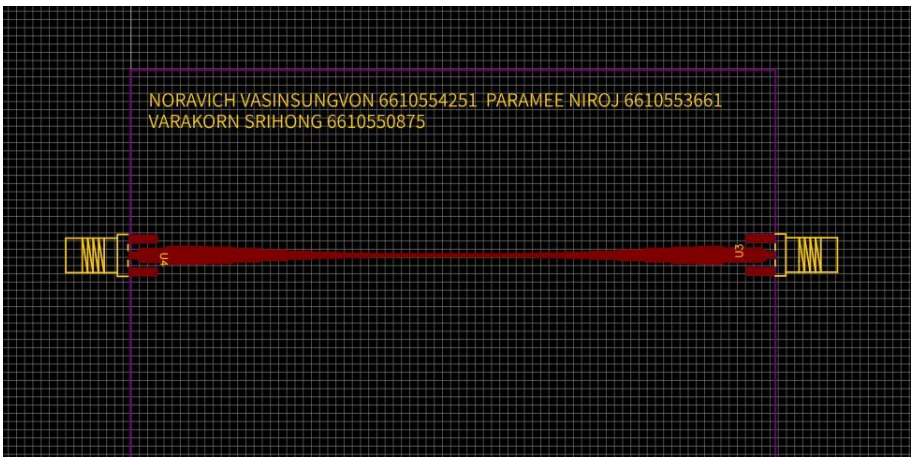
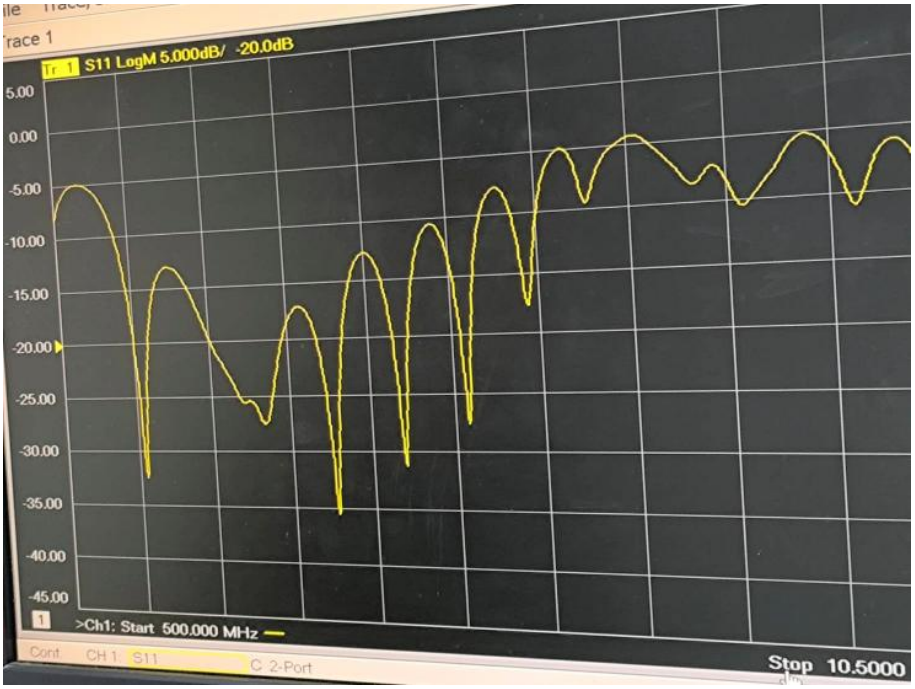


Figure 8: Final PCB realization of the symmetric tapered microstrip transformer.

9. Testing


Trace 1
Tr 1 S11 LogM 5.000dB/ -20.0dB
5.00
0.00
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-10.00
-15.00
-20.00
-25.00
-30.00
-35.00
-40.00
-45.00
>Ch1: Start 500.000 MHz
Cont CH 1: S11 C 2-Port
Stop 10.5000