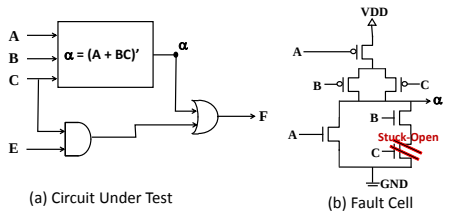
National Tsing Hua University, Taiwan
EE-6250 超大型積體電路測試(VLSI Testing)
(Closed-Book) Midterm Exam., Fall Semester, 2019 (Nov. 6, 2019)

1. (20%) Answer the following questions.
   (a) The quality of an IC is often measured by its DPPM. What does **DPPM** stand for? (請說明 DPPM 代表那些英文字即可) (5%) → Defective Parts Per Million
   (b) An electronic device operating in the field may tend to have a higher and higher failure rate over time due to the ageing effects. Try to name one possible **ageing effect**. (除了縮寫外，也說明縮寫所代表的英文字) (5%) → NBTI (Negative Biased Temperature Instability), HCI (Hot Carrier Injection), TDDB (Time-Dependent Dielectric Breakdown), or Electro-Migration
   (c) In order to combat the cloning or IP theft, a PUF circuit might be inserted into an IC design so that a random yet unique and lifetime-invariant identifier (ID) can be produced for each manufactured IC. What does **PUF** stand for? (請說明 PUF 代表那些英文字即可) (5%) → Physically Unclonable Function
   (d) An IO pad could be damaged due to the ESD effect (靜電放電效應). Thus, during the manufacturing test, we need to test an IC's ESD ability as well, e.g., by applying ±4KV, Human Body Mode ESD test, among others. What does **ESD** stand for? (請說明 ESD 代表那些英文字即可) (5%) → Electro-Static Discharge

2. (10%) Answer the following questions regarding **9-valued ATPG algorithm**.
   (a) Logic symbol 'u/1' corresponds to two 5-valued symbols in {0, 1, X, D, D'}. One of them is '1'. What is the other? (5%) → D' (or 0/1)
   (b) Consider the fault propagation across a D-frontier NAND gate with the inputs {$x1$, $x2$} and the output {y}. Assume that a fault effect D' (0/1) is now at $x1$, we want to propagate it to y. What signal requirement is needed at the side-input $x2$? → 'u/1'

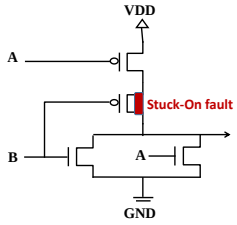
3. (10%) Answer the following questions regarding **Boolean Difference**.
   (a) Consider a Boolean function $f(x_1, x_2, x_3)$. Denote the **Boolean Difference** $\boldsymbol{df/dx_2}$ as a Boolean expression in terms of $f(x_1, x_2=0, x_3)$ and $f(x_1, x_2=1, x_3)$. (5%)
   → $f(x_1, x_2=0, x_3) \oplus f(x_1, x_2=1, x_3)$
   (b) If the above Boolean Difference characterizes an input vector $(x_1, x_3)=(1, 1)$. Then, what is the test vector for $x2$ sa-1 fault? (5%) → $(x_1, x_2, x_3)=(1, 0, 1)$.

4. (10%) Consider a faulty circuit shown below with a logic cell harboring a **transistor stuck-open** fault. We need a two-pattern test <v1, v2>, where v1 is an initialization vector, and v2 a detection vector.
   (a) The first vector v1 needs to initialize the output of the faulty cell to logic '1'. All input vectors satisfying the above initialization requirement can be expressed by two 3-valued pattern, one is (A, B, C, E) = (0, 0, X, X). What is the other? (5%) → (A, B, C, E) = (0, X, 0, X)
   (b) The second vector is to activate the fault and propagate the fault effect to the output signal F. Derive the only test vector satisfying the above requirement. (5%) → (A, B, C, E) = (0, 1, 1, 0)

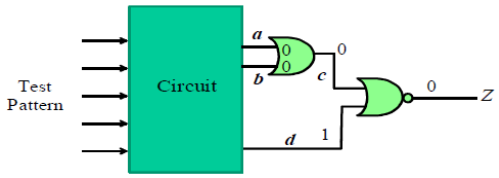


(a) Circuit Under Test (b) Fault Cell

5. (10%) Answer the following questions about the **testing of a transistor stuck-ON fault**.
   (a) When a transistor in a logic cell has a stuck-ON fault, IDDQ test might be an effective test method. Please explain why? (Hint: it is relevant to the short-circuit current). (5%) → A stuck-ON fault could cause excessive short-circuit current (or called leakage current), flowing from VDD to GND under some test vector during the idle mode, and thus that effect can be detected by measuring the QUIESENT CURRENT at some VDD/GND pin.
   (b) Consider a logic cell shown below, with a *stuck-ON* fault occurring to the pMOS controlled by input signal B. Please derive the test pattern in terms of the cell's input signals {A, B}, so that the IDDQ test can be effective. → (A, B) = (0, 1), to cause short-circuit current from VDD to GND.

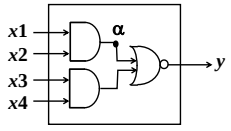


6. (10%) Complete the **deductive fault simulation** as indicated in the figure below to derive the final detected faults by the current test pattern. The fault-free values are {a=0, b=0, c=0, d=1, Z=0}.The fault lists at signals a, b, and d are denoted as La, Lb, and Ld, respectively. Express your answer of the final detected faults as a symbolic formula in terms of La, Lb, Ld and some union, complement, or intersession operators as discussed in class. Note that a fault not contained in any of La, Lb, Ld need not be considered. → (La + Lb)'•Ld = (La)' •(Lb)'•Ld (兩個答案都可以)



7. (15%) Answer the following questions related to the *equivalence* and *dominance relationships* among stuck-at faults.
   (a) Assume that a stuck-at-fault α dominates another stuck-at-fault β. What is the relationship between their test sets, denoted as Test(α) and Test(β), respectively? (5%) → Test(α) ⊇ Test(β)
   (b) Consider an AND cell in a circuit, with the two inputs denoted as {$x1$, $x2$}, and the output denoted as y. List the two stuck-at faults at the inputs dominated by y-stuck-at-1 fault. (5%) → {$x1$-stuck-at-1, $x2$-stuck-at-1}
   (c) Consider a AOI cell below with the output function represented by y=($x1x2$+$x3x4$)'. Prove that $x1$-stuck-at-1 fault is dominated by output y-stuck-at-0 fault. (5%) →{Test($x1$-sa-1) ⊆ Test(α-sa-1), Test(α-sa-1) ≡ Test(y-sa-0)} → so Test($x1$-sa-1) ⊆ Test(y-sa-0)，即 $x1$-sa-1 is dominated by y-sa-0. 得證

An AOI (AND-OR-Invert) Cell y=($x1x2$+$x3x4$)'



8. (15%) Answer the following questions about *test time*.
   (a) Why is test time an essential issue in VLSI testing? (5%) → Longer test time implies higher test cost.
   (b) Consider the full-scan methodology for a circuit with 99 flip-flops. A combinational ATPG program produces 123 vectors to fully test the logic. Compute the number of clock cycles needed to apply

these vectors, assuming that the system clock and test clock are the same and there is only one scan chain. (Note: each vector requires a scan-in operation through the SI pin, followed by one clock cycle for capturing the responses at the peudo-primary-outputs (PPOs) back into the flip-flops, and then followed by a scan-out operation to shift out the final response through the SO pin). But it is required that the **scan-in operation and scan-out operation are overlapped whenever applicable** to reduce the test time. In this calculation, we ignore the time for applying the PI sub-vectors and the time for observing the PO sub-vectors.) (10%) → 123*(99+1) + 99 = 12399 (Each vector requires its own scan-in time (99) plus the response-capture time (1). But the scan-out time for the 122 vectors are shadowed by their respective next vector's scan-in time, except the last vector, which requires an extra scan-out time (99)).