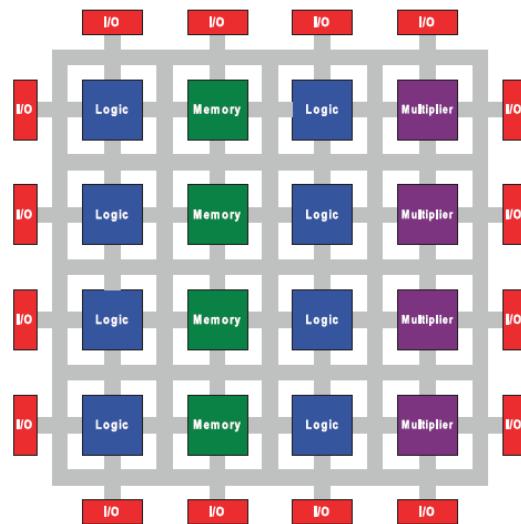


# *Classification and Evolution of Field Programmable Logic Devices*

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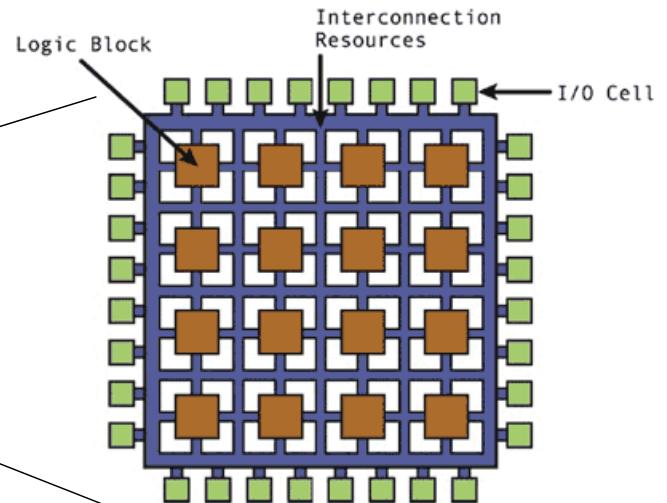
## Topics

- Distinction from ASIC
- Classification & evolution of FPLDs
- FPLD markets



2

# Field-Programmable Gate Array (FPGA)



3

## Field-Programmable Devices

- *User-configurable* ICs.
- They are standard parts, not designed for any particular application.
- Unlike traditional ASIC, logic function is specified by the user *after* the device is manufactured.
- They are programmed/configured by the users to implement their designs *at their own sites*.
- *Instant configuration* (in minutes) at users' site.



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# Advantages of Field-Programmable Logic Devices

- Short turnaround time for new designs
- Low startup cost
- Low inventory cost
- Low risk
- Allow easy design changes



5

How to make a chip that can realize different circuits and configurable?

What are the essential elements that make up any circuit?

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# What do you expect within a FPLD?

logic gate

FF

wire

1. Substantial amounts of uncommitted combinational logic.
2. Contain flip-flops/latches.
3. Programmable interconnections between the combinational logic, flip-flops, and chip input/outputs.

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## Types of Field-Programmable Devices

- *Simple Programmable Logic Devices (SPLDs)*
- *Complex Programmable Logic Devices (CPLDs)*
- *Field-Programmable Gate Arrays (FPGAs)*

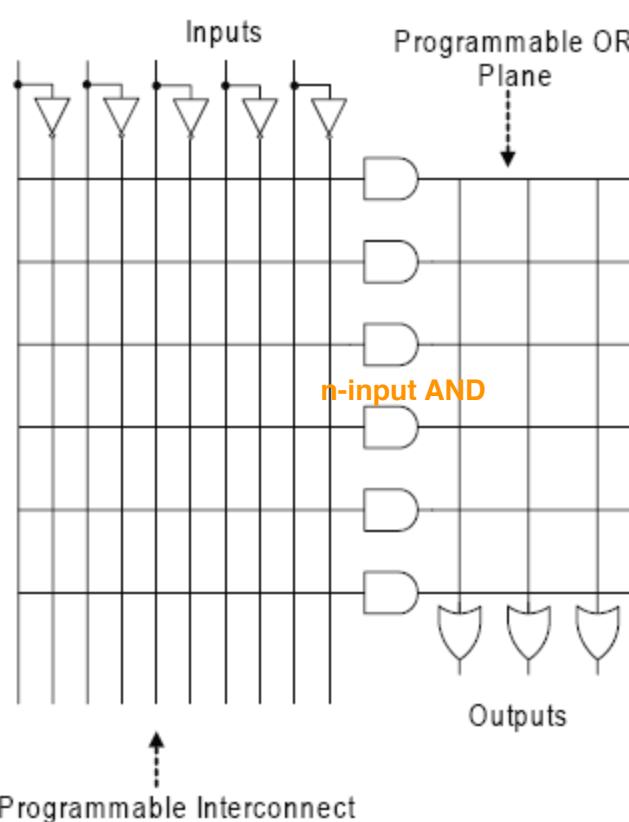
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# Programmable Logic Array (PLA)

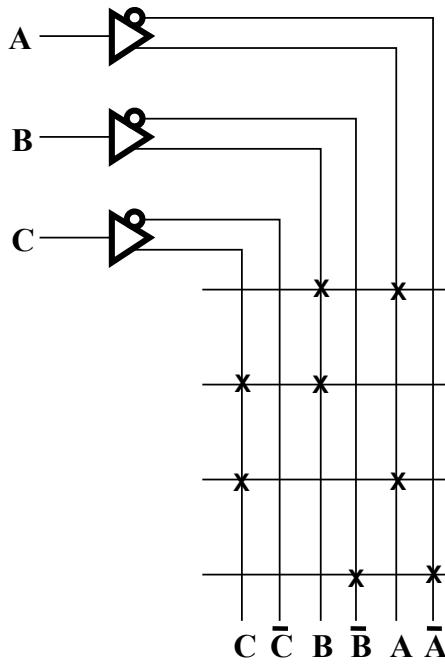
- A simple programmable logic device (SPLD).
- The first programmable logic device introduced in the early 1970s by Philips.
- Use a *2-level logic* structure to implement programmed logic.
- Based on idea that logic functions can be realized in *sum-of-products* form.
- A programmable array of AND gates feeding a programmable array of OR gates.

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## PLA Structure



# Function Implementation by PLA



- What are the equations for  $F_1$  and  $F_2$ ?
- Could the PLA implement the functions without the XOR gates?

NO  
4個and 最多4個product term  
但 $F_1 F_2$ 共有5個product term

所以最後的xor很重要  
就算今天某  $F$  是由很多個product組成  
我們仍能用4個product和xor表示

$\times$  Fuse intact  
 $+$  Fuse blown  
 $F = m_0 + m_2 + m_3 + m_4 + m_5 + m_6$   
 $= !(m_1 + m_7)$

$m_0 = !A!B!C$   
 $m_1 = !A!BC$   
 $\dots$

$m_7 = ABC$

$AB+BC+AC$   
 $AB+!(A)!(B)$

$0$   
 $1$   
 $AB+BC+AC$

$F_1$

$F_2$

$!(AB+!(A)!(B))=!(A)B+A!(B)$

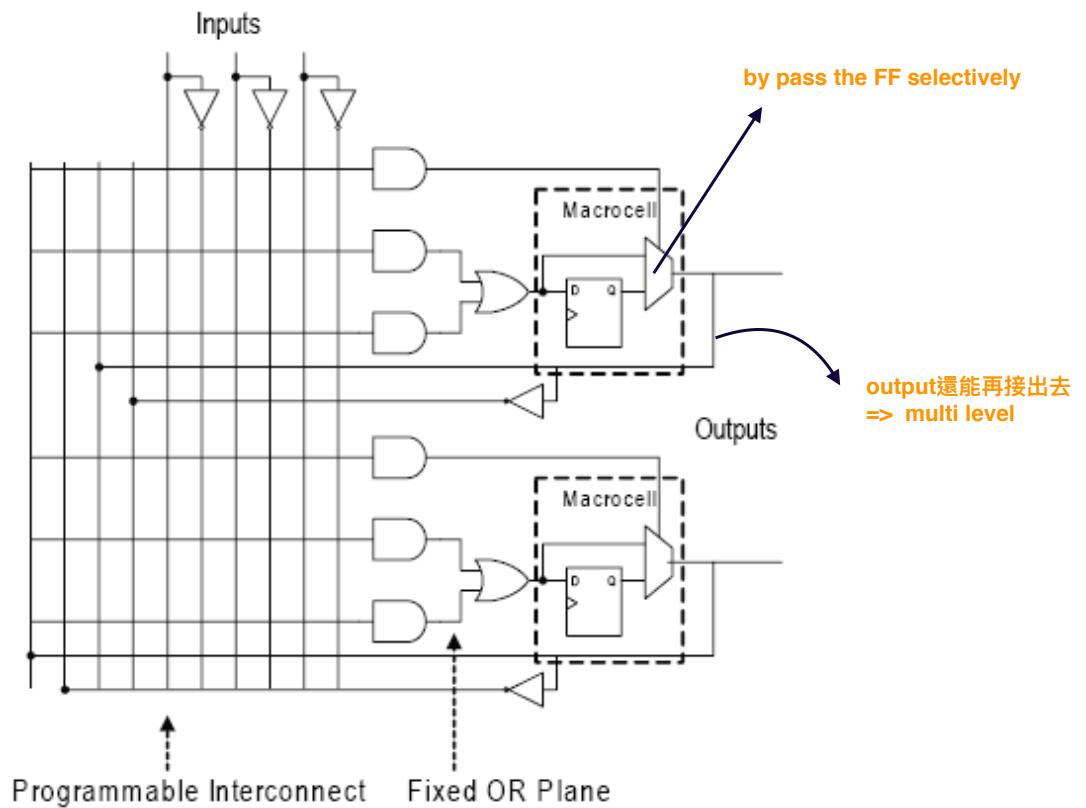
Adapted from Logic and Computer Design Fundamentals. Copyright Prentice Hall.

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## Programmable Array Logic (PAL)

- Introduced to overcome the weaknesses of PLAs (programmable switches were hard to fabricate correctly and introduced significant propagation delays).
- A programmable array of AND gates feeding a fixed array of OR gates.
- PAL usually contains flip-flops connected to the OR gate outputs to implement sequential circuits.  
(Macrocell: an OR gate combined with a flip-flop and extra circuitry in a PAL.)
- PLAs and PALs are useful for implementing small digital circuits, typically  $\leq 32$  combined inputs and outputs.

# PAL Structure



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## Function Implementation by PAL

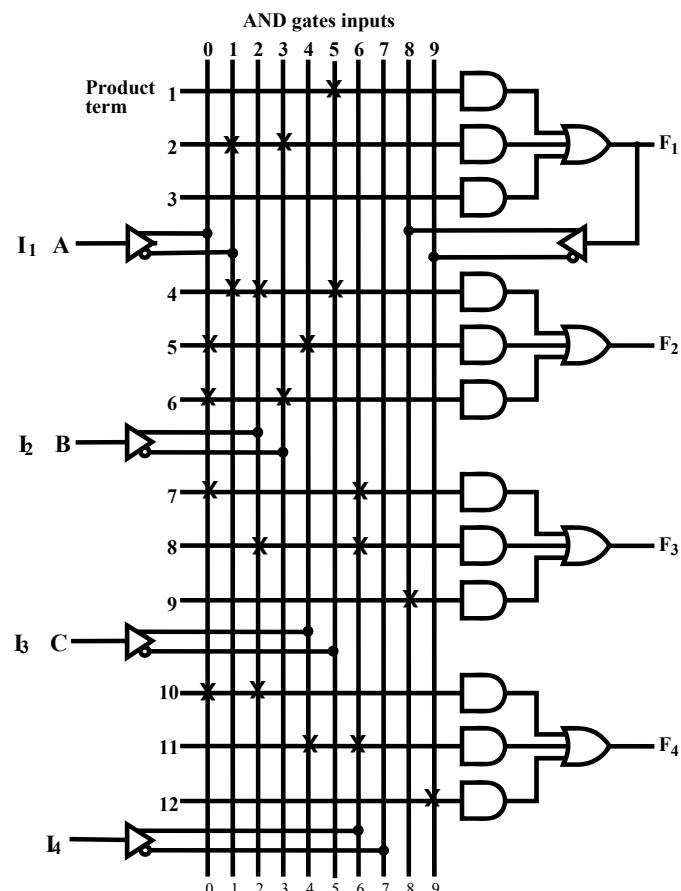
- 4-input, 4-output PAL with fixed, 3-input OR terms
- What are the equations for F1 through F4?

$$F_1 = \overline{A} \overline{B} + \overline{C}$$

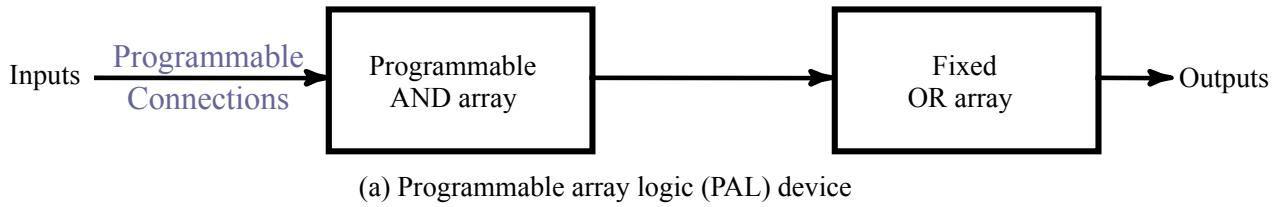
$$F_2 = \overline{A}B\overline{C} + AC + AB$$

$$F_3 =$$

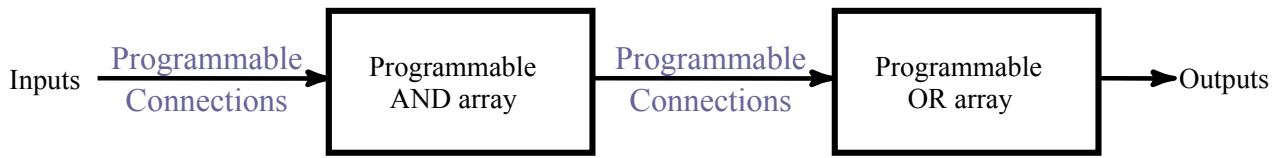
$$F_4 =$$



# PAL and PLA Comparison



(a) Programmable array logic (PAL) device



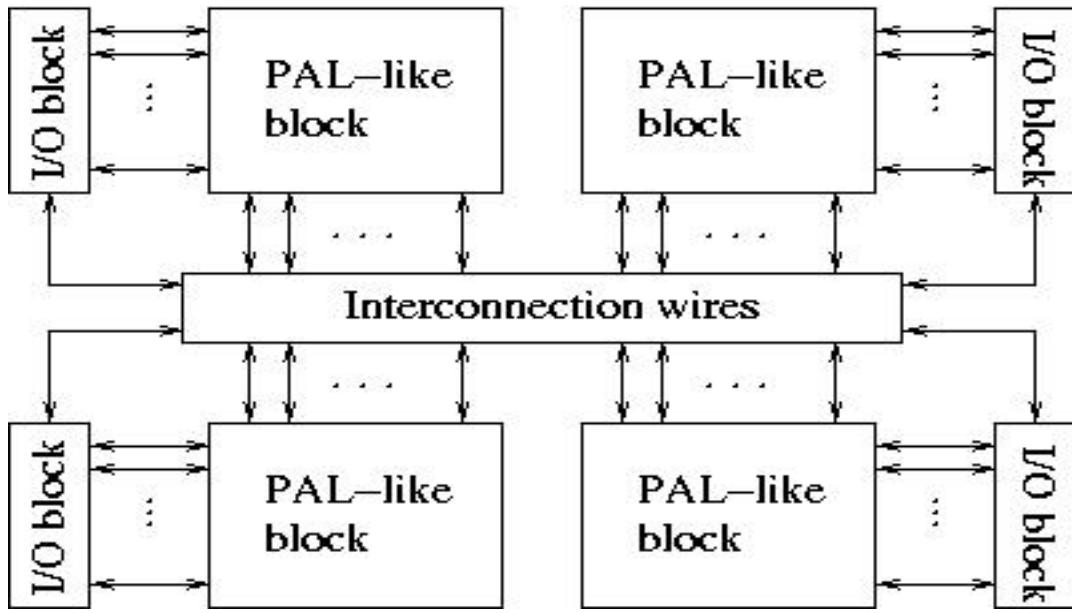
(b) Programmable logic array (PLA) device

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*How to get larger capacity?*

# Complex Programmable Logic Device (CPLD)



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# Complex Programmable Logic Device

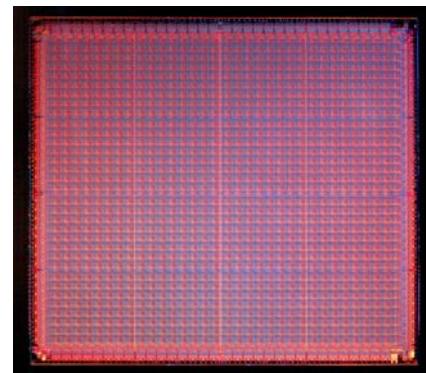
- Combines multiple PAL-like blocks with programmable interconnect network.
- Provides much larger capacity than SPLDs.

basic idea for SPLD/CPLD is sum of product  
but not for FPGA

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# Field-Programmable Gate Array (FPGA)

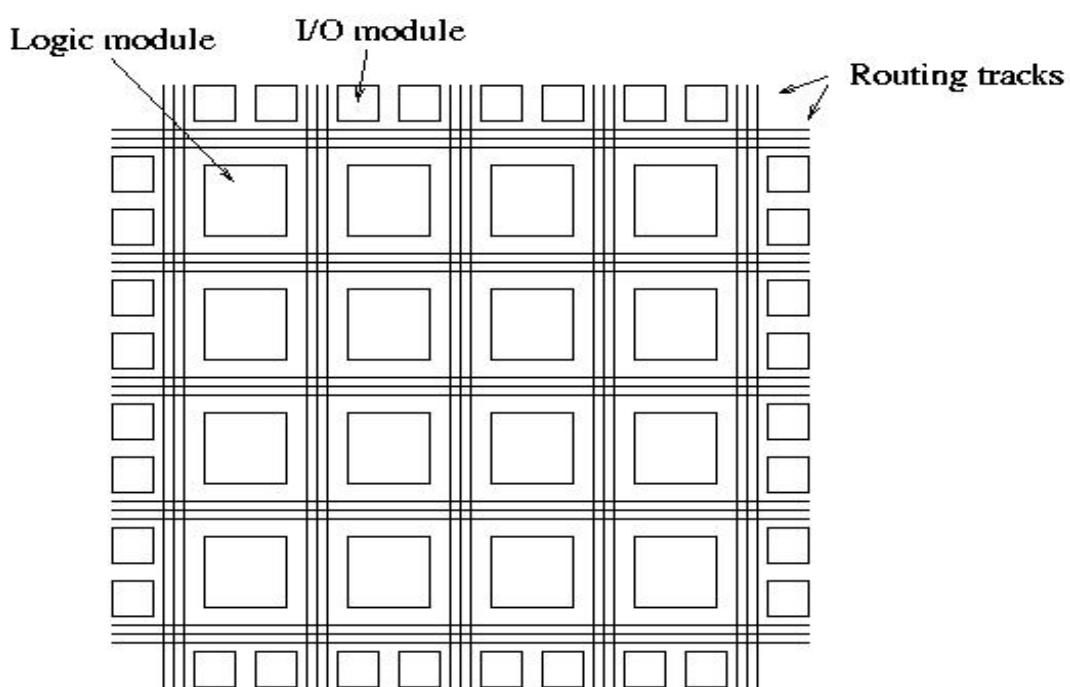
- A high-capacity programmable logic device providing multi-level logic.
- Introduced in 1985 by Xilinx.
- Classic FPGA consists of an array of programmable logic blocks surrounded by programmable interconnect.



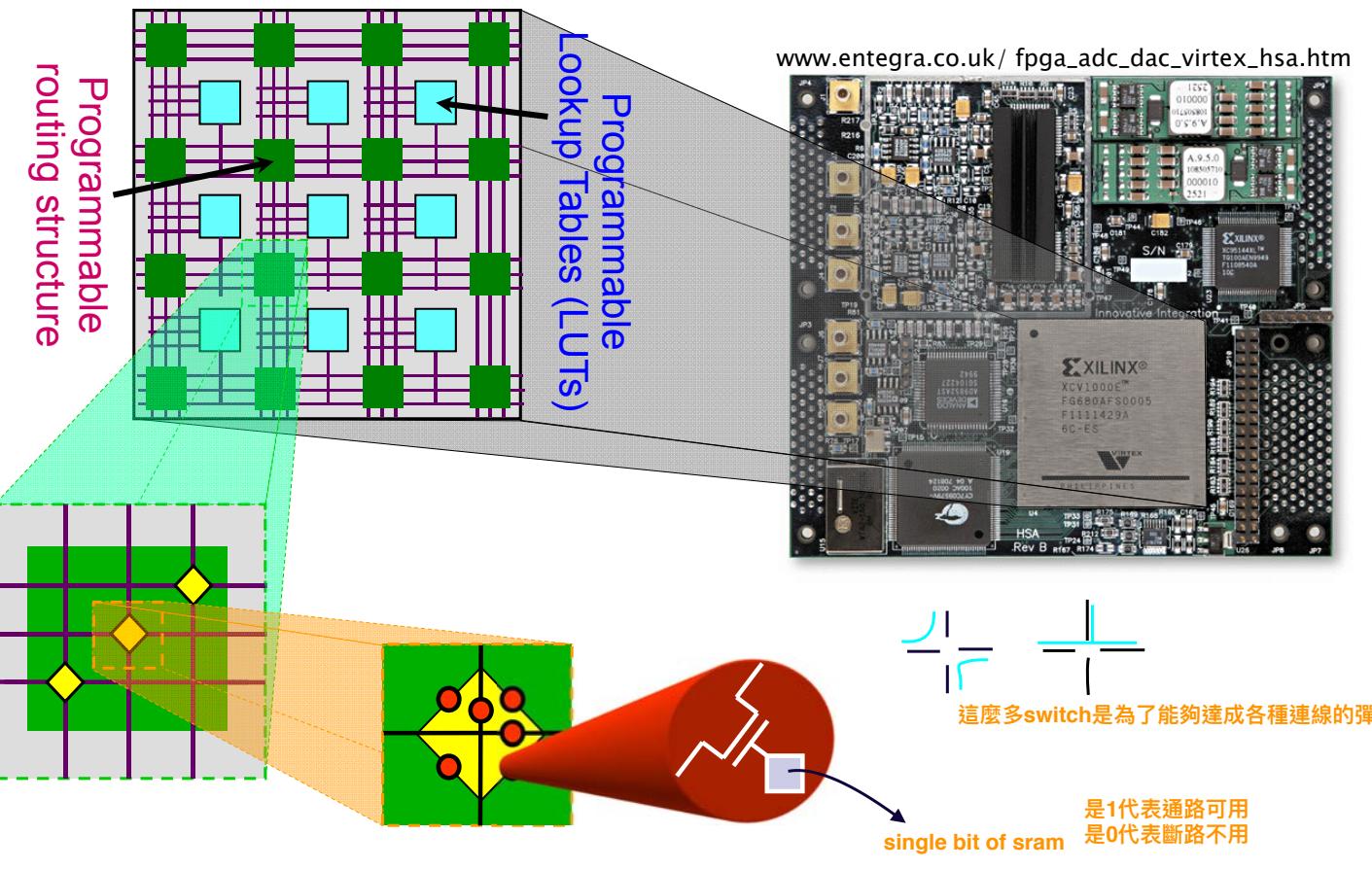
Xilinx XC4000ex

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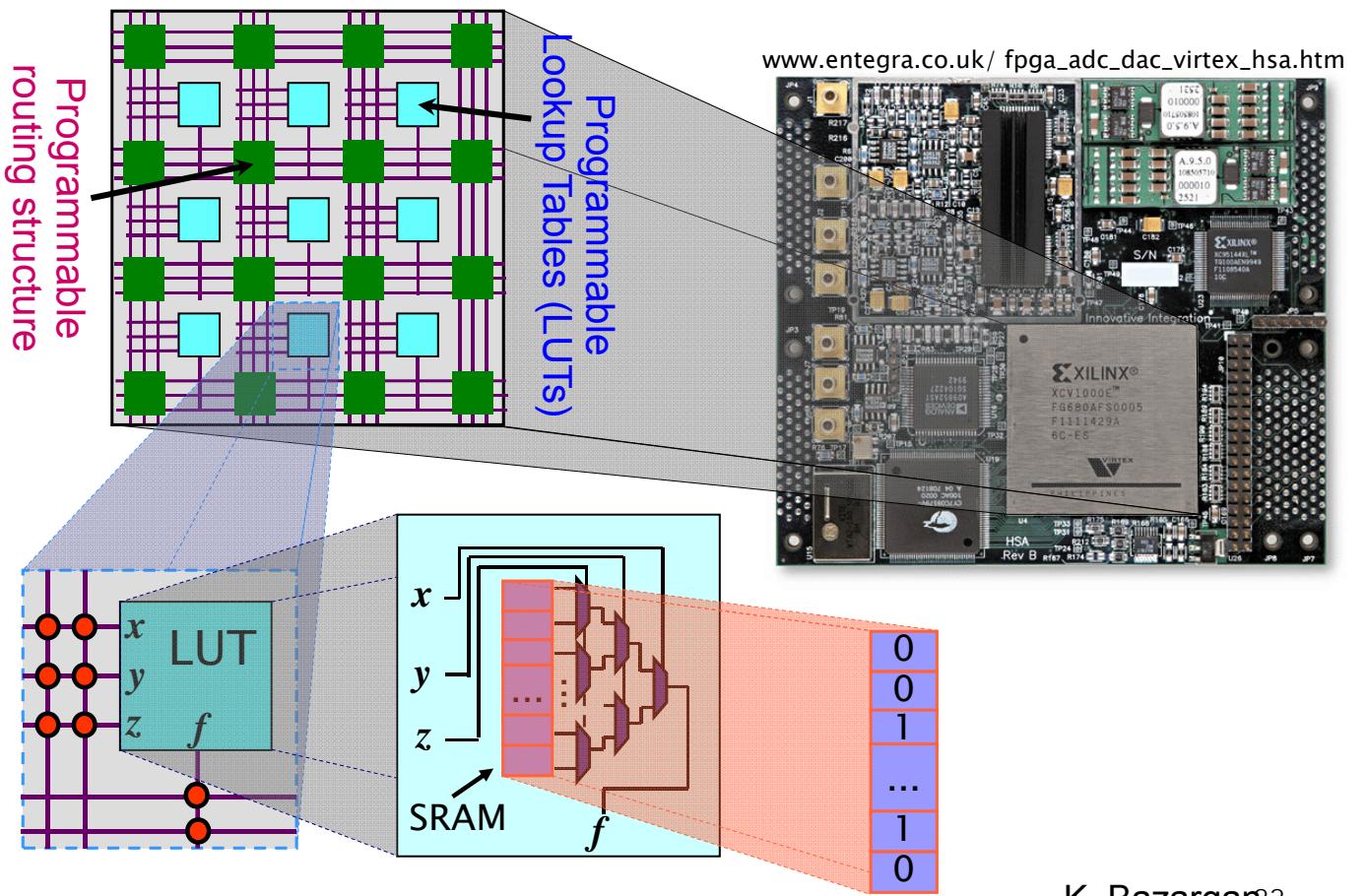
## Field-Programmable Gate Array



# SRAM-Based FPGA



# SRAM-Based FPGA



# Microprocessor vs Custom Chip vs FPGA

ie. ASIC

## ■ Microprocessor

- Rely on software to implement functions
- Slowest, most power-hungry
- Re-programmable (load different software)

## ■ Custom Chip

- Designed for a particular purpose
- Fastest, most power-efficient
- Not re-programmable

## ■ FPGA

- Not designed for any particular function
- In between microprocessor and custom chip in speed and power
- Re-programmable (most)

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## Rapidly Increasing Logic Capacity

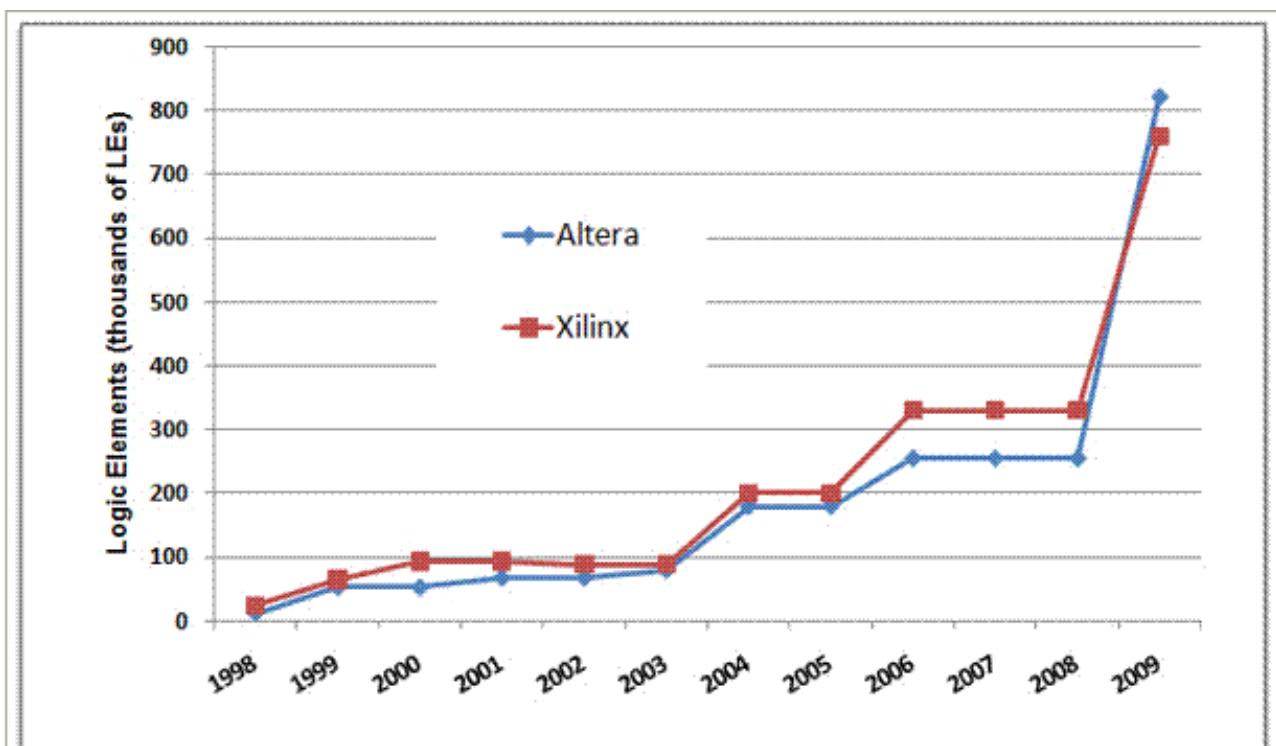


Figure 1. Largest FPGA announced (by equivalent 4-input Logic Elements - LEs).

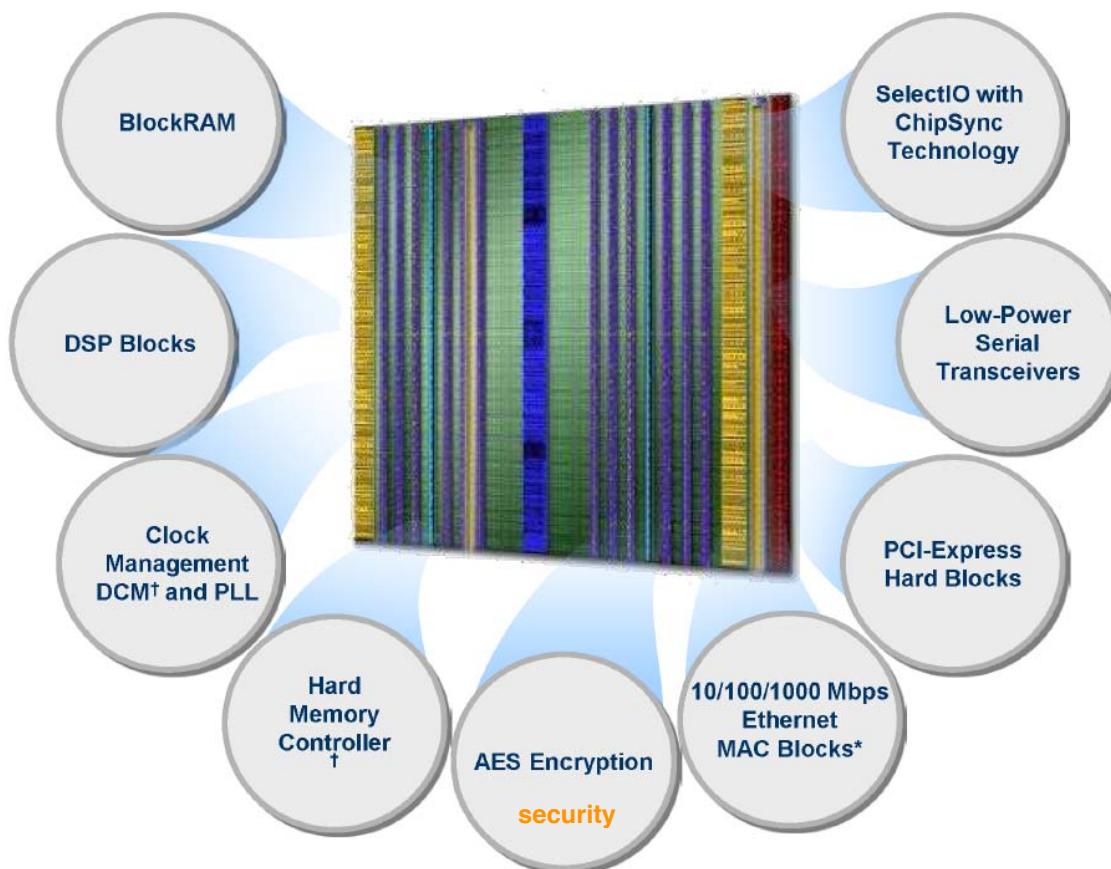
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# Today's FPGAs

- Additional resources: embedded memory blocks, fast carry logic chains, DSP blocks
- Versatile programmable I/Os
- Some even contain: 1 or more processors
- Applications: audio, video, wireless, industrial equipments, network components, medical, automotive, etc.
- Vendors offer a variety of FPGAs catering for different markets

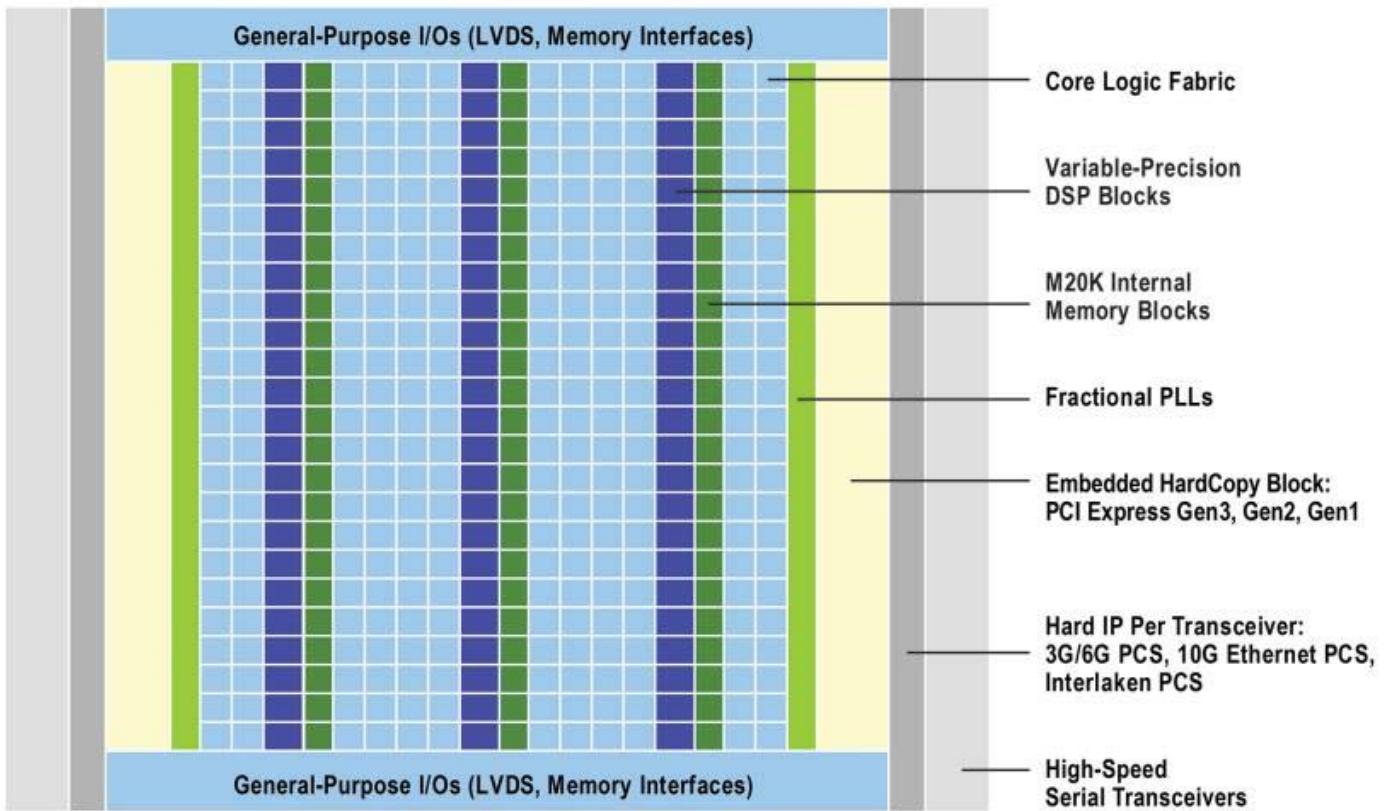
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## Advanced Features of Today's FPGAs



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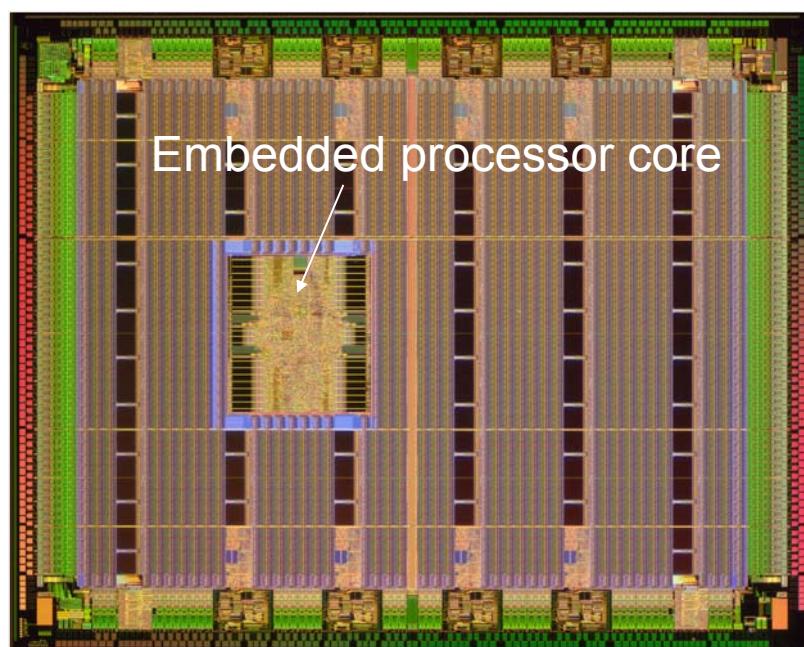
# Advanced Features of Today's FPGAs



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## SoC FPGA

- Xilinx's Zynq families and Intel's SoC FPGAs
  - with 1 or more ARM cores



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