



# *Comparison of IC Implementation Technologies*



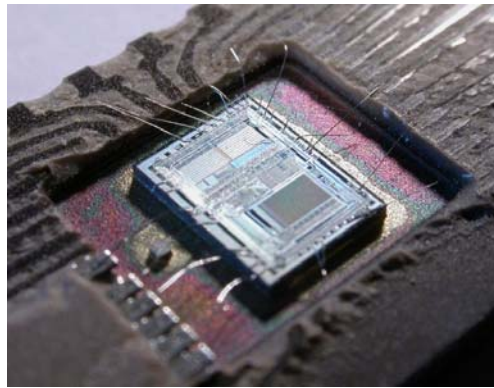
## **Outline**

- Full-Custom Design
- Cell-based Design
- Gate Array
- Structured ASIC
- FPLD

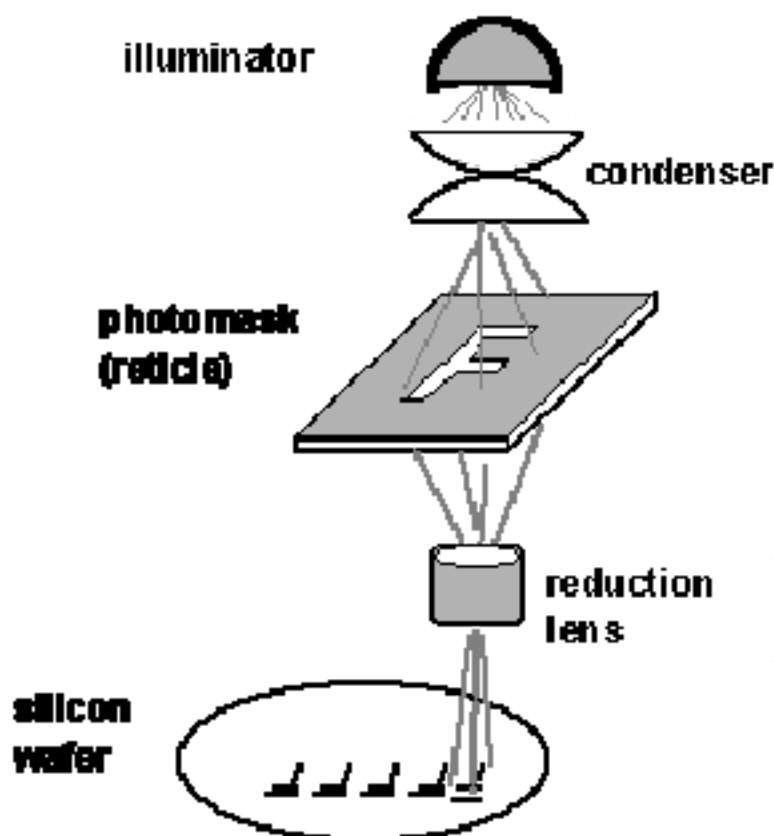
# Introduction to Integrated Circuits

small size ic

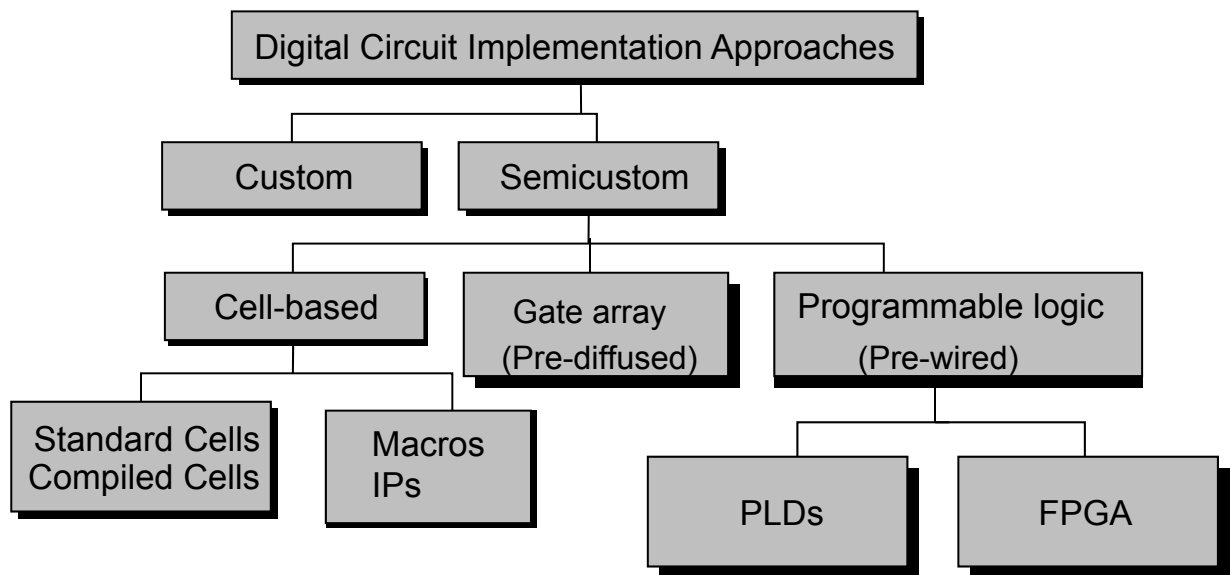
- *Integrated circuits* combine dozens (SSI) to millions (VLSI) of transistors into a single chip.
- The locations and connections of the transistors are defined by several *masks* in the *fabrication* process.



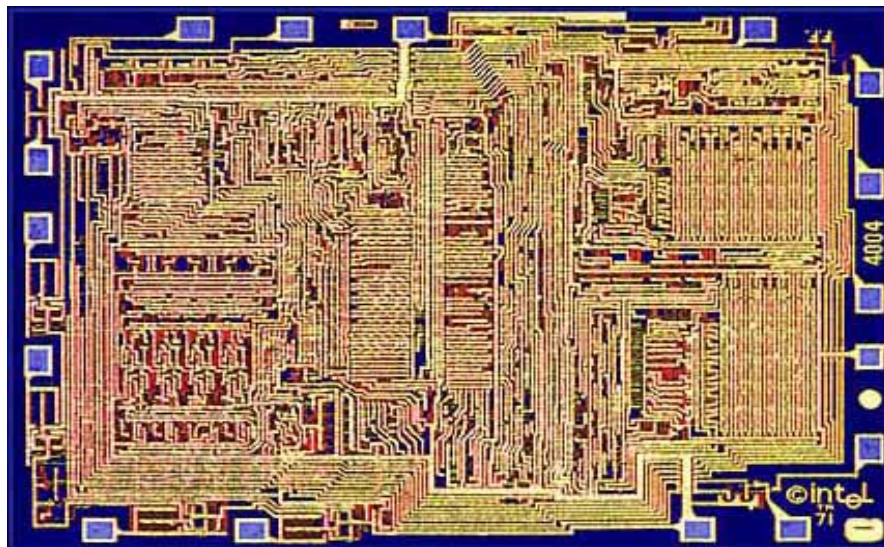
## Simplified View of IC Fabrication



# IC Implementation Options



## Full-Custom Layout Example



Intel 4004 ('71)

# Full-Custom Design

- Designers determine and draw all device geometries.
- All mask layers are customized.
- E.g. microprocessor, memory
- **Pros:** complete design flexibility, high degree of optimization in performance and area.
- **Cons:** large amount of design effort and time, expensive to design and manufacture.
- For applications that require high volume, cost can be amortized over the high volume.

攤平

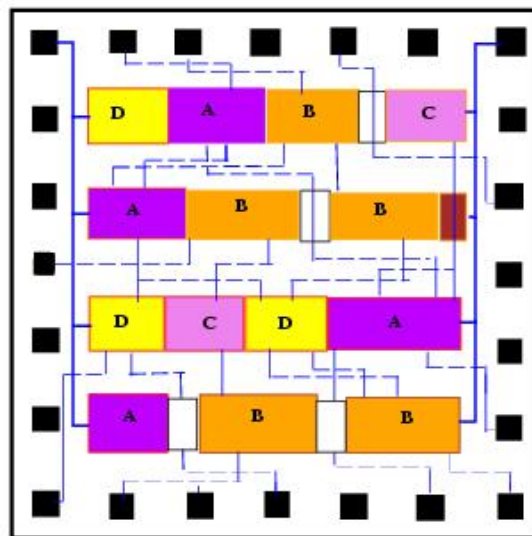
*How can we shorten the time from design to a physical IC?*

# Cell-Based Design

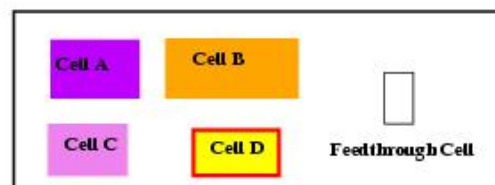
- Reuse!
- Large complex cells/blocks e.g. macros, IPs.
- Small cells e.g. standard cells.

ex : Intel CPU會放  
ARM的micro processor

## Standard Cell-Based Design Example



cell library

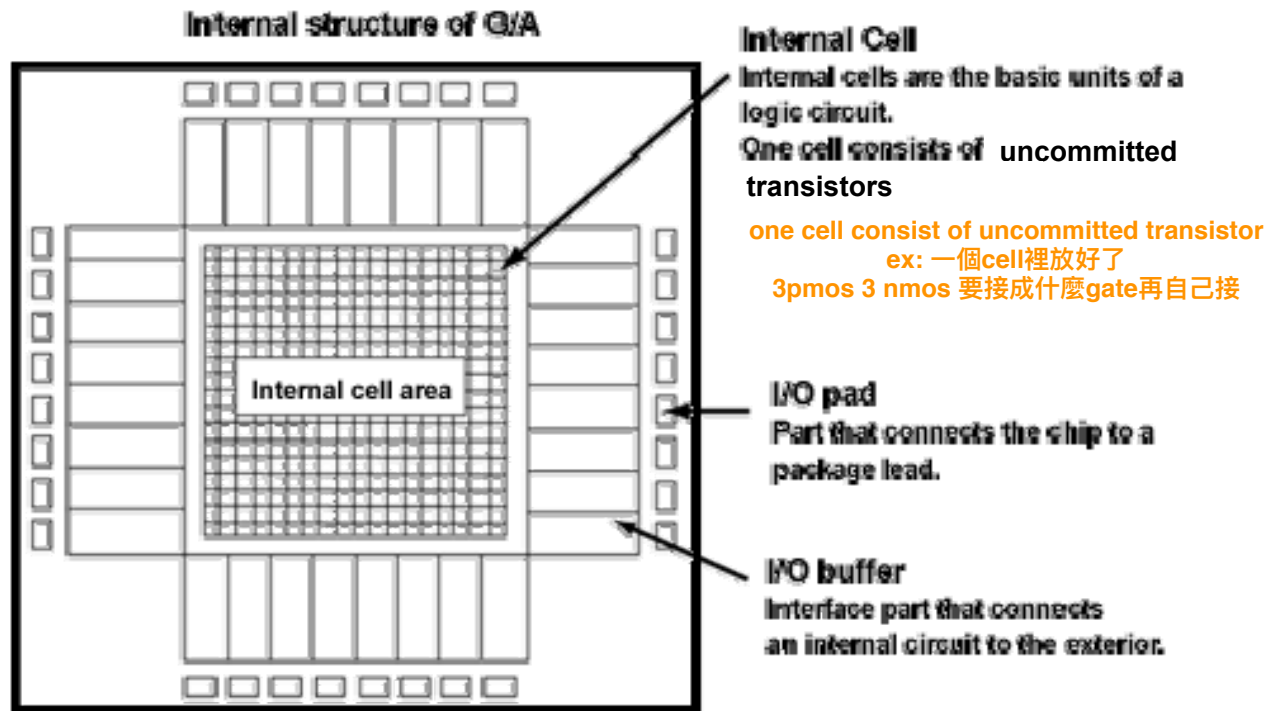


# Standard-Cell-Based Design

- Use predesigned, pretested and precharacterized logic cells from standard-cell library as building blocks.
- Standard cells are of the same height.
- Cells are laid out in rows.
- Chip layout (placement and routing) are much easier than in full-custom design.
- All masks need to be customized to fabricate a new chip.
- **Pros:** save design time and money, reduce risk compared to full-custom ICs.  
cell based是減少design的時間 而非製造的時間 那些mask還是要重新設計
- **Cons:** somewhat less efficient in size and performance than full-custom ICs.

*How about half-made chips?*

# Mask Programmable Gate-Array



Source: NEC Corp.

transistor都已經放好了 只要接metal那些的 減少製造的成本和時間

# Mask Programmable Gate-Array

- A gate-array is partly pre-fabricated.
- Identical base cells are pre-fabricated in the form of a 2-D array
- Wires between transistors inside the cells or across the cells are custom fabricated for each customer.
- So custom masks are made for wiring only.
- **Pros:** cost saving (fabrication cost of a large number of identical template wafers is amortized over different customers), shorter manufacture lead time.
- **Cons:** performance not as good as full-custom or standard-cell-based ICs.

# Structured ASIC

- Like gate-array, an array of tiles is pre-fabricated.
- Unlike gate-array, the majority of the metal layers are also pre-fabricated to form local and global interconnect.
- Power, clock and test structures are predefined in most structured ASICs.
- Structured ASICs may also have “built-in” macros common for certain applications.
- Customize only upper metal layers for customers.

只能設計高層的metal

## Structured ASIC Example

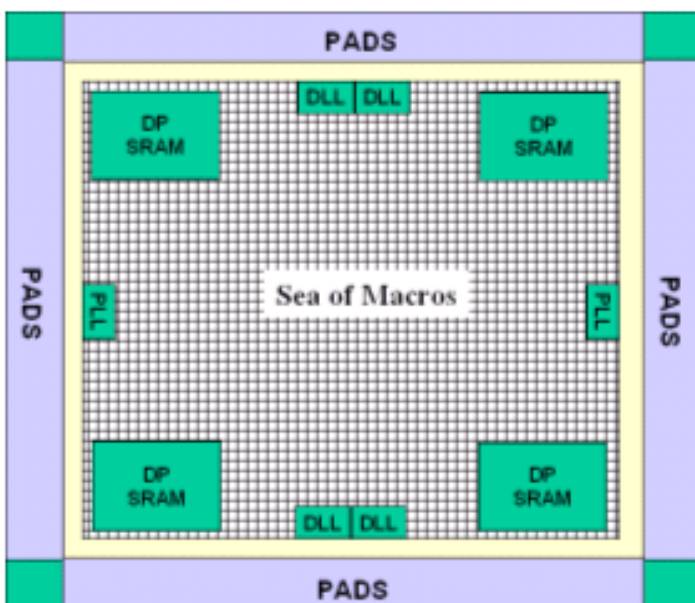


Figure 1: Structured ASIC Block Diagram

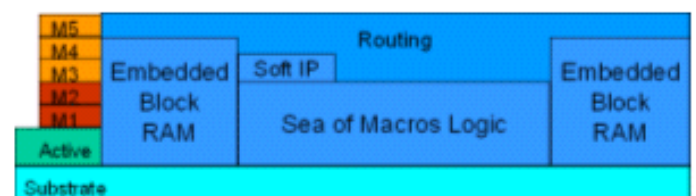
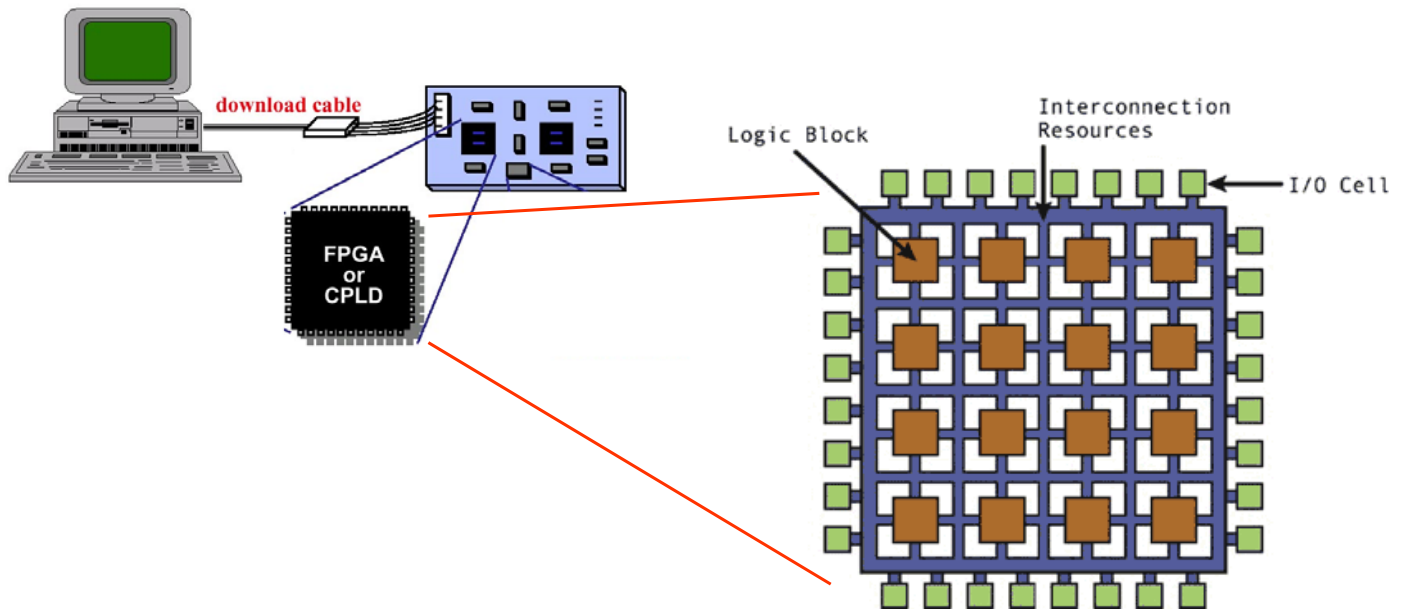


Figure 2: Structured ASIC Metal Utilization



# Field Programmable Logic Device (FPLD)

- Off-the-shelf
- Contains programmable logic blocks + programmable interconnect network



## Field Programmable Logic Device

- General-purpose chip for implementing logic circuitry.
- Logic cells and interconnect can be programmed by end-user to implement specific circuitry.
- Transistors and wires are already prefabricated on a PLD.
- Already packaged and fully tested.
- No need to create custom masks for each customer.
- **Pros:** low non-recurring-engineering cost (ideal for low-volume production), fast turnaround time.
- **Cons:** lower performance and larger chip size.

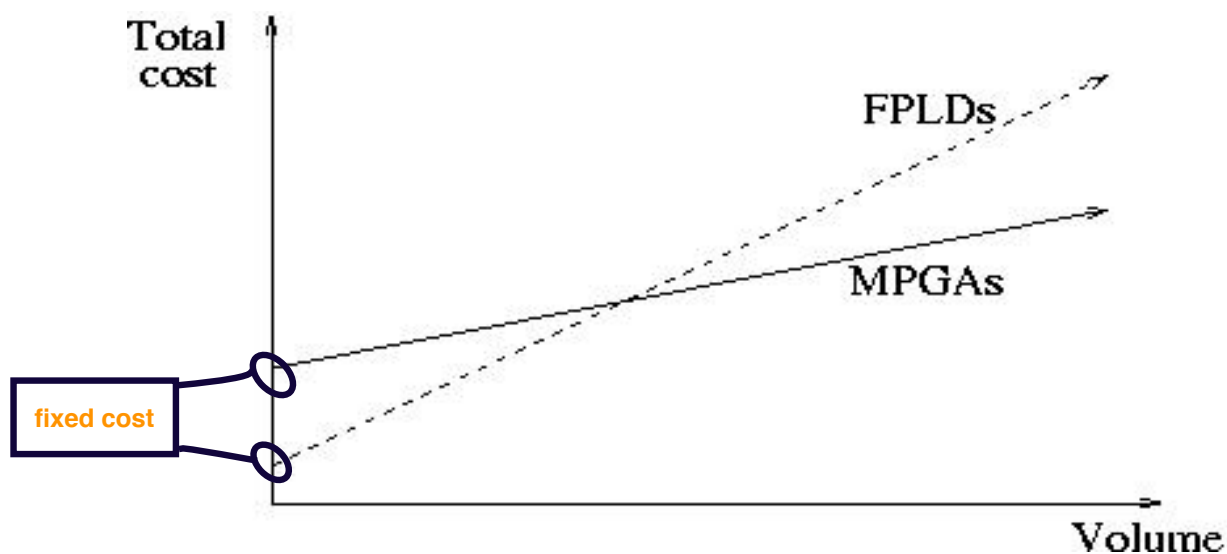
# IC Economics

- Total cost = Variable cost per unit \* Volume + Fixed cost
- **Fixed cost**: independent of volume produced e.g. costs of design and simulation, masks, equipments, etc.
- **Variable cost**: dependent on volume e.g. cost of the parts, assembly costs, other manufacturing costs, testing costs, etc.

(material cost per IC + testing cost per IC + packaging cost + ...) / Yield \* Volume

良率高就不用浪費cost做一堆

## Cost vs Design Volume Example



variable cost

每一個花多少

低的量多就能把價格壓下來

## Comparison of Technologies

	Full-custom	Standard cell-based	Gate array	FPLD
Cell size	variable	fixed height	fixed	fixed
Cell type	variable	variable	fixed	programmable
Cell placement	variable	in row	fixed	fixed
Interconnections	variable	variable	variable	programmable
Custom layers	all layers	all layers	routing layers only	none

## Comparison of Technologies

	Full-custom	Standard cell-based	Gate array	FPLD
Performance	+++	++	+	-
Area	+++ <small>smallest</small>	++	+	--
High-volume cost	++	++	+	+
Low-volume cost	---	--	+	+++
Fabrication time	---	--	-	+++
Time to market	---	--	++	+++
Risk reduction	---	--	-	+++
Design modification	---	--	-	+++



## Summary

- Different implementation options cater for different needs and concerns.
- IC design trend: going more regular to cope with increasing design complexity.
- Going more cell-based/array-based.