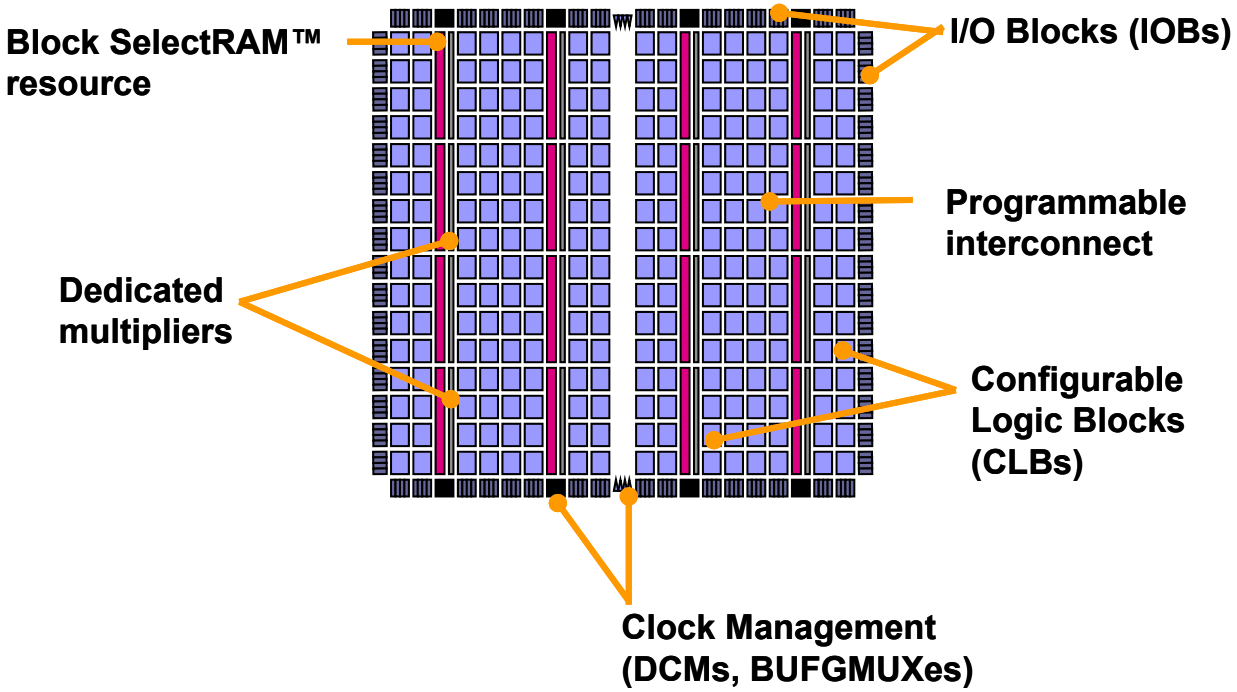
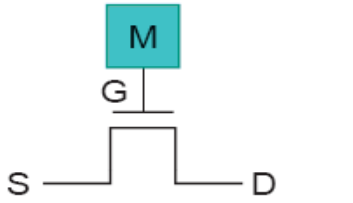
Commercial Examples (Part 1): Xilinx SRAM-based FPGAs

Xilinx FPGA

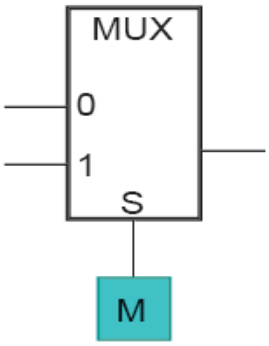
- A basic SRAM-based FPGA (Spartan-3)



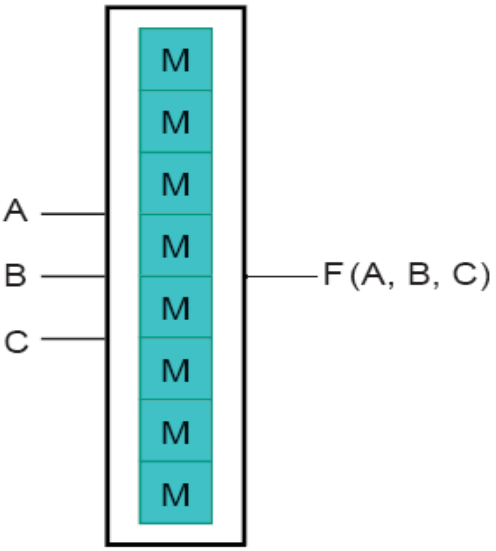
SRAM Usage



(a) Pass transistor control



(b) Multiplexer control

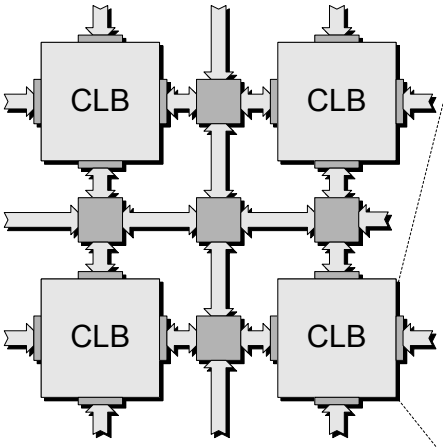


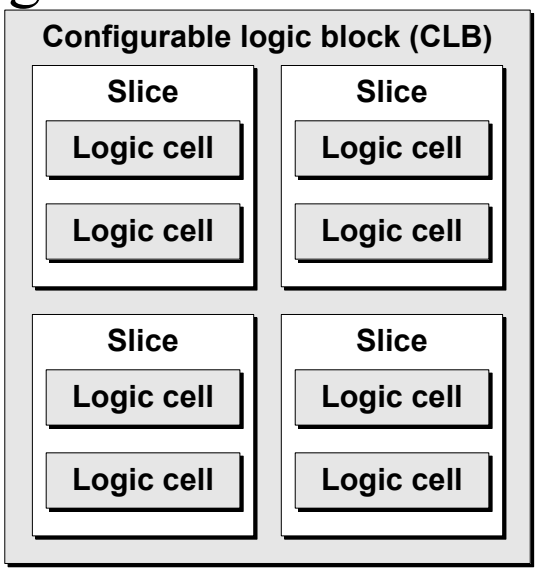
(c) Look up table implementation

Xilinx's CLBs

- A configurable logic block (CLB) contains a few (2/4) slices.
- Each slice has a few (2/4) logic cells.

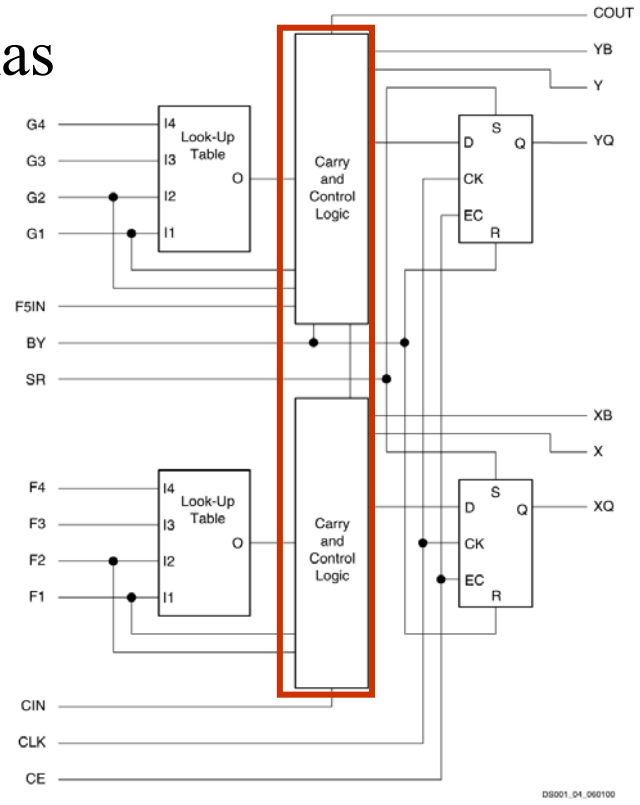
在同CLB內 溝通速度很快





Slice Structure

- E.g. A slice in Spartan-3 has
  - two 4-input LUTs
  - two carry and control logic blocks
  - two storage elements
- Carry logic runs up vertically

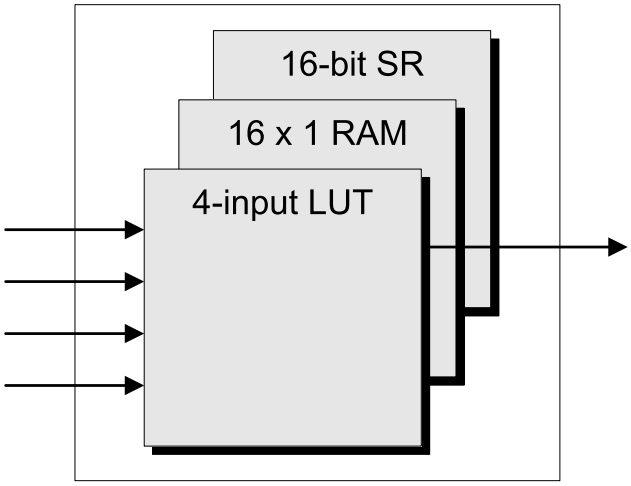


CLB Details

- Multiple roles of LUT
  - function generator/synchronous RAM/shift register
- Dedicated carry logic
  - perform fast arithmetic functions
- MUXes
  - can combine results of 2 function generators
- Storage elements
  - can be configured as DFF or latch
- CLB outputs
  - three-state drivers (BUFTs) are provided before routing

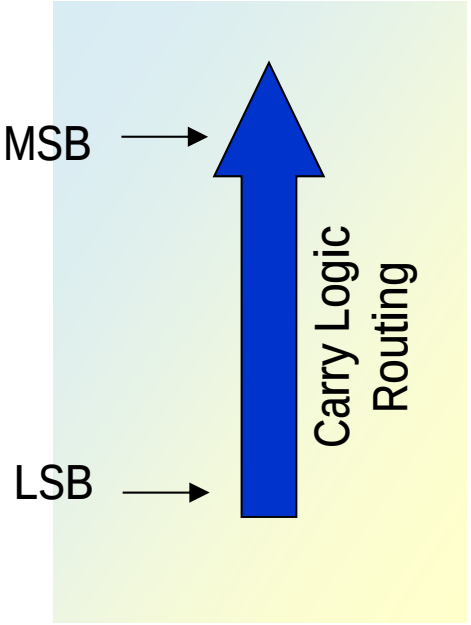
Multipurpose LUT

- E.g. A 4-LUT can be used as
  - a function generator
  - 16-bit synchronous RAM
  - 16-bit shift register



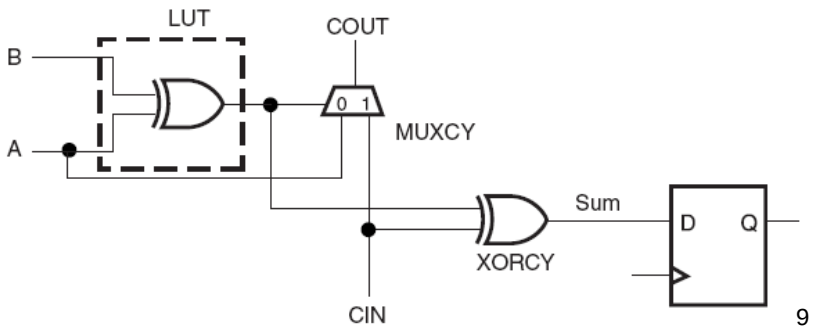
Fast Carry Logic

- Each CLB contains separate logic and routing for the fast generation of sum & carry signals
  - Increases efficiency and performance of adders, subtractors, accumulators, comparators, and counters



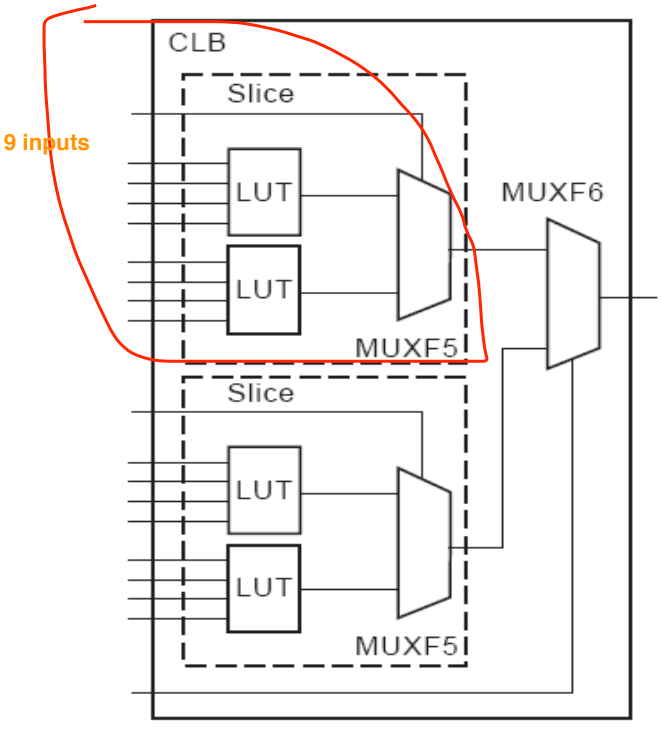
Carry and Arithmetic Logic

- Automatically used for most arithmetic functions in a design
- Include dedicated XOR gates and AND gates to implement efficient arithmetic functions together with the LUTs
- E.g. Addition



MUXes in CLB

E.g.

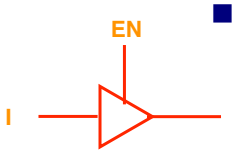


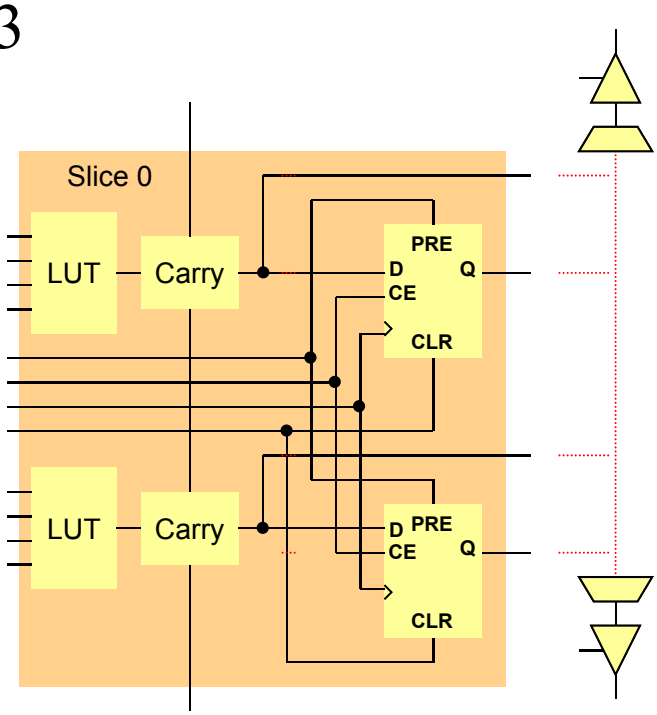
- The MUXes increase the flexibility of a CLB
  - Output of MUX F5 can be any function of ≤5 variables or a restricted class of functions of up to 9 variables. 5 input mux 能做的兩個4 input mux 都能做 但後者能多表現某幾個的 9 variable function
  - Output of MUX F6 can be any function of ≤6 variables or a restricted class of functions of up to 19 variables.

CLB Outputs

- E.g. A slice in Spartan-3
  - 4 outputs per slice
    - 2 registered, 2 non-registered
  - 2 BUFTs associated with each CLB
    - accessible by all 16 CLB outputs

tri state buffer

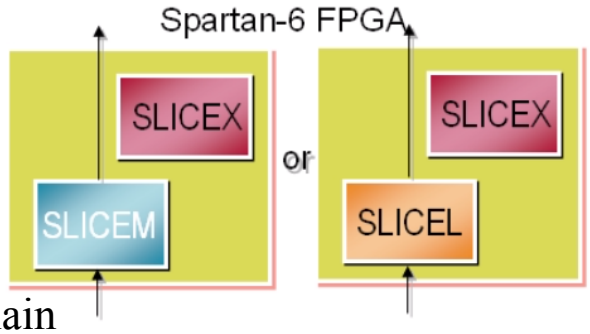




RC delay 與 length^2成正比
所以適當的插入buffer可以降低delay

Some Changes in Spartan-6

- 3 Types of slices
  - SLICEM: full slice (25%)
    - LUT can be used for logic and memory/SRL
    - Has wide multiplexers and carry chain
  - SLICEL: Logic and arithmetic only (25%)
    - LUT can only be used for logic
    - Has wide multiplexers and carry chain
  - SLICEX: Logic only (50%)
    - LUT can only be used for logic
    - No wide multiplexers and carry chain
- New LUT structure



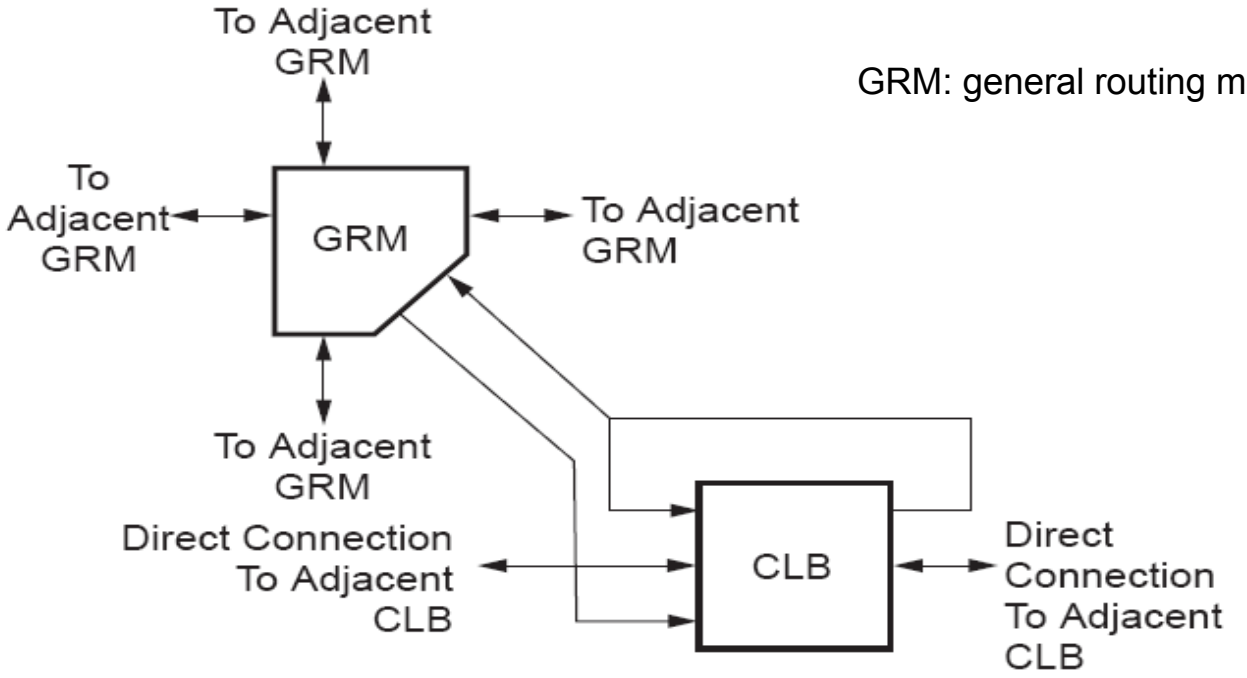
Interconnect

- Types of interconnect:
  - local;
  - general-purpose;
  - dedicated;
  - global routing network (for clock and other very high fanout signals)

General-Purpose Interconnect

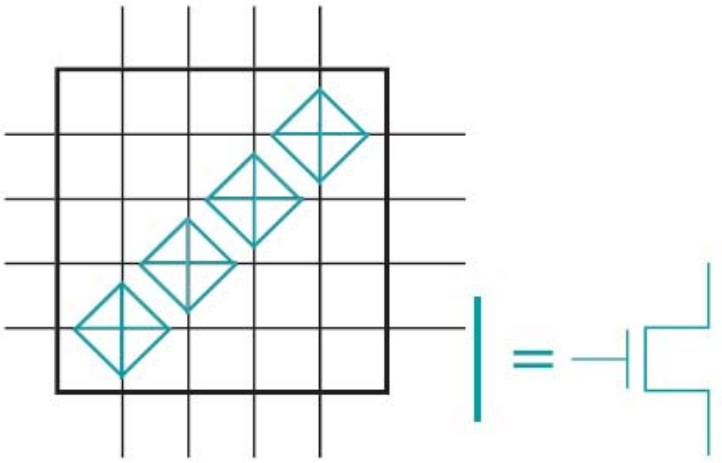
- General routing matrix (GRM) connects horizontal/vertical channels and CLBs.
- Single-length lines connect adjacent GRMs.
- Hex lines connect GRM to GRMs six blocks away.
- Buffered longlines span the chip.

General-Purpose Interconnect

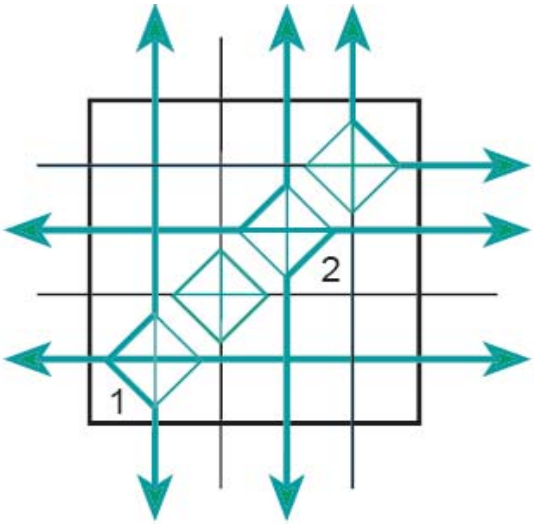


GRM: general routing matrix

General Routing Matrix



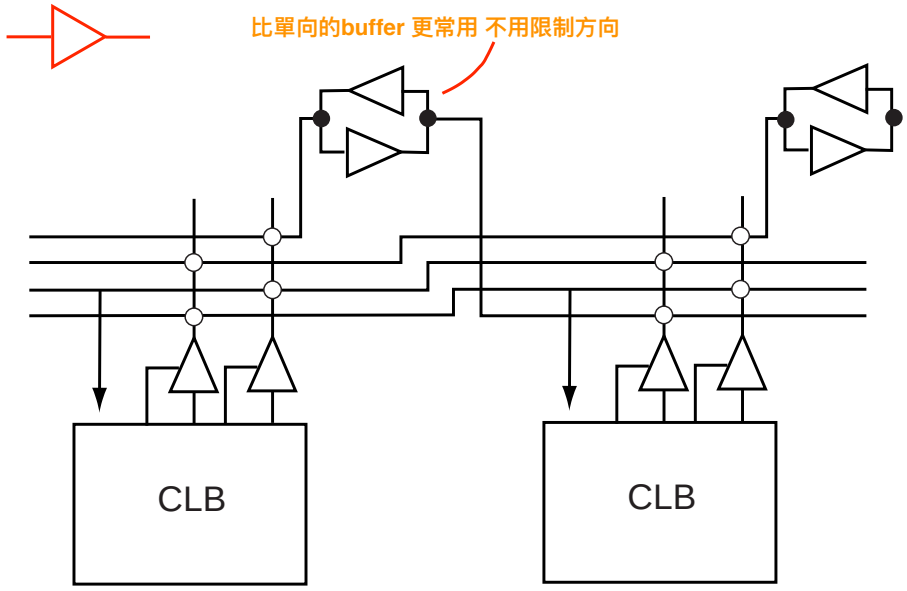
Switch box transistors



Connection example

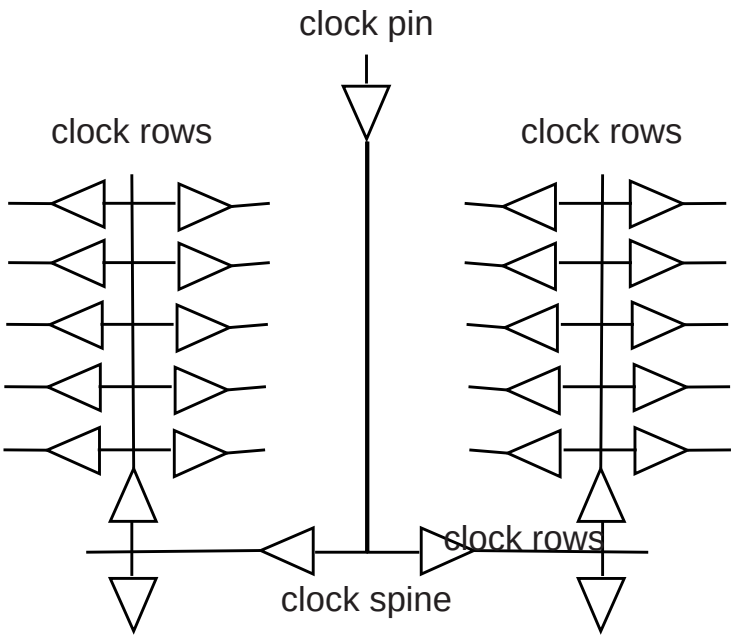
Three-State Bus

- Dedicated resources for horizontal on-chip busses:



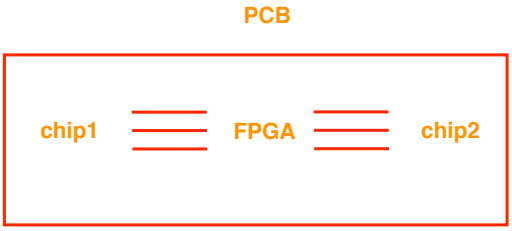
Clock distribution

- Use global routing resources

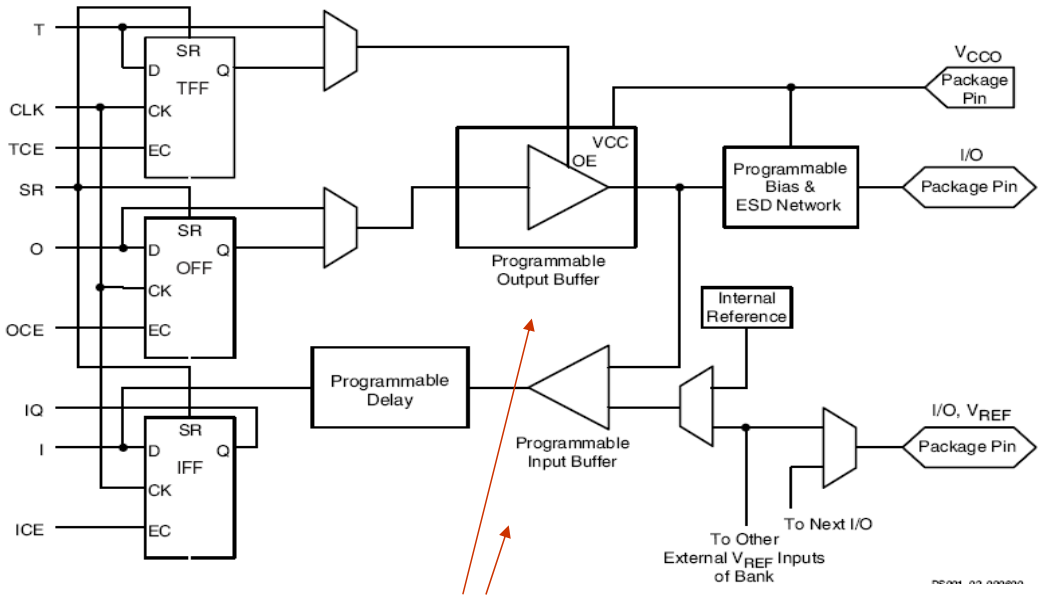


I/O Block

- IOB provides interface between the package pins and CLBs
- Support a variety of IO standards
- Each IOB can work as uni- or bi-directional I/O
- Outputs can be forced into High Impedance
- Inputs and outputs can be registered
  - advised for high-performance I/O
- Inputs can be delayed



I/O Block Diagram

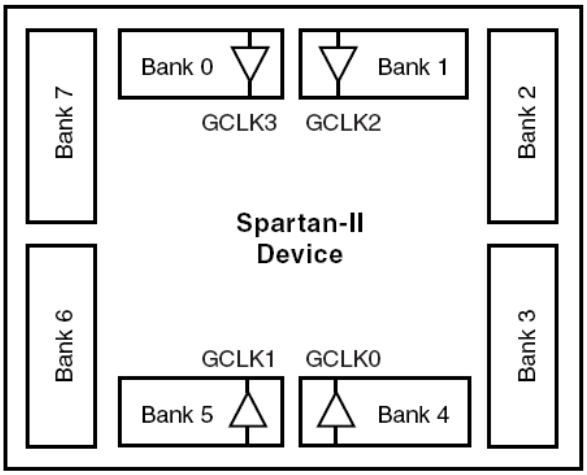


Can be configured to support different signaling standards

I/O Standards and I/O Banks

I/O Standard	Input Reference Voltage (V_{REF})	Output Source Voltage (V_{CCO})	Board Termination Voltage (V_{TT})
LVTTL (2-24 mA)	N/A	3.3	N/A
LVCMOS2	N/A	2.5	N/A
PCI (3V/5V, 33 MHz/66 MHz)	N/A	3.3	N/A
GTL	0.8	N/A	1.2
GTL+	1.0	N/A	1.5
HSTL Class I	0.75	1.5	0.75
HSTL Class III	0.9	1.5	1.5
HSTL Class IV	0.9	1.5	1.5
SSTL3 Class I and II	1.5	3.3	1.5
SSTL2 Class I and II	1.25	2.5	1.25
CTT	1.5	3.3	1.5
AGP-2X	1.32	3.3	N/A

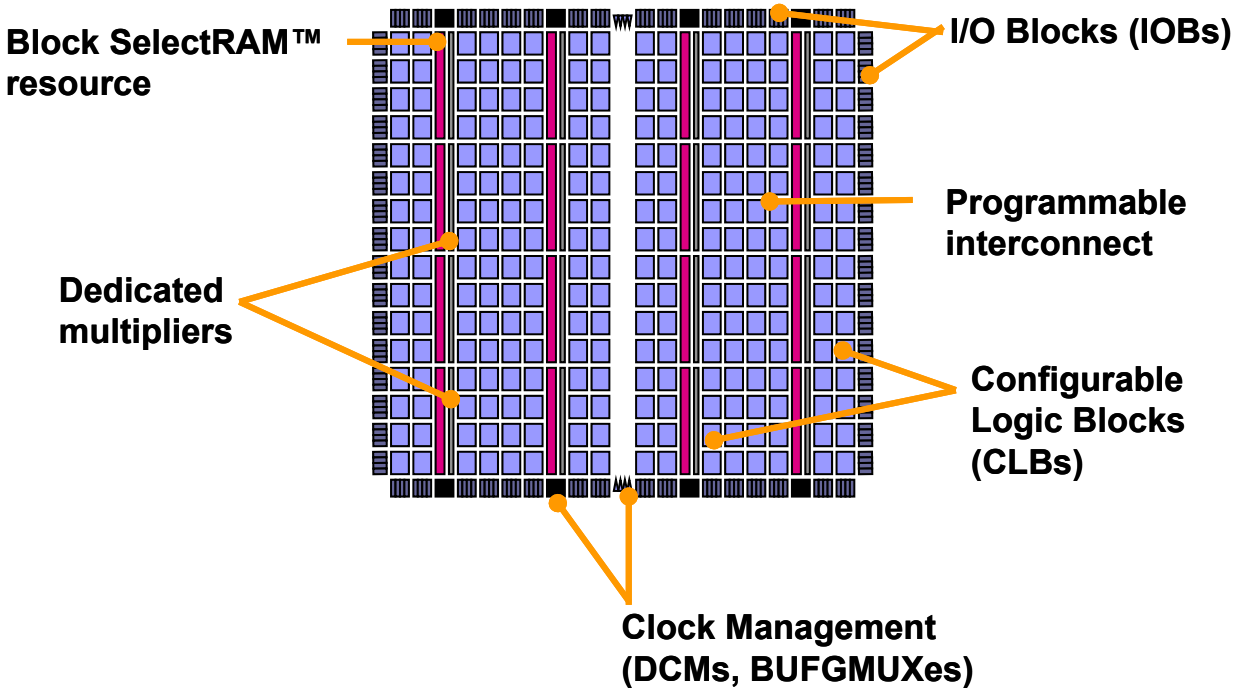
I/O standards supported by Spartan-II



I/O bank organization.

FPGA allows programmable io-standard

Spartan-3 Architecture



Other Features

- Block RAMs
  - Dedicated blocks of memory (18-kb blocks)
  - Use multiple blocks for larger memories
- Dedicated 18 x 18 multipliers next to block RAMs
- Clock management resources
  - Dedicated global clock multiplexers
  - Digital Clock Managers (DCMs)
    - multiple clock domains