CS 5160-00 Fall 2019

FPGA Architecture & CAD

Instructor: Prof. Wai-Kei Mak (麥偉基 教授) wkmak@cs.nthu.edu.tw
Office: 台達館 Delta 637 Consultation hours: M78
Teaching Assistant: 黃照軒 fp4397251@gmail.com
Office: 資電館 EECS 226 Consultation hour: R3-4p.m.

Prerequisites Interest in the area of electronic design automation;
Basic knowledge of logic design; C/C++ programming skill

Course Content

Field programmable gate arrays (FPGAs) are computer logic chips whose function and wiring can be re-programmed. FPGAs enable the creation of custom computing engines with higher efficiency than conventional software-programmed processors. FPGA-based electronic designs are found everywhere such as consumer gadgets, wired and wireless communication, automotive, industrial, medical, scientific, aerospace, military, etc. FPGAs are one of the first commercially available 3D/2.5D ICs. FPGAs are highly power-efficient for implementing neural networks for accelerating AI applications. Cloud service providers are offering customers the ability to use FPGAs as accelerators. Increasingly, FPGAs are displacing ASICs and ASSPs as IC design complexity and manufacturing costs continue to rise.

This course first introduces the characteristics, evolution and usage of field-programmable technologies, and then continues to look into some advanced researches related to FPGA architecture and CAD. On the hardware side, we will investigate the tradeoff involved in finding a balanced FPGA architecture and study some recent commercial FPGA architectures as examples. On the software side, we will look at the FPGA design flow and study the design of efficient FPGA CAD tools for technology mapping, placement, and routing, etc. to optimize power and performance. New directions of architecture & CAD research will be explored together at the end.

Class webpage NTHU e-learning system http://lms.nthu.edu.tw/

Textbook No required textbook.
Lecture notes written by the instructor will be provided.
Supplemented with selected articles and research papers.

References 1. *Field-Programmable Gate Arrays*, by S.D. Brown, R.J. Francis, J. Rose, and Z.G.. Vranesic, Kluwer Academic Publishers.

2. *FPGA-Based System Design*, by W. Wolf, Prentice Hall.
3. *Application-Specific Integrated Circuits*, M.J.S. Smith, Addison Wesley.

Schedule

Part I. FPGA Technology & Architecture

1. Why FPLDs?
2. Classification and Evolution of FPLDs
3. Programming Technologies and Logic Element Design
4. Routing Architecture Design
5. Commercial Examples
6. Circuit Design and Architecture Issues

Part II. FPGA CAD

1. Technology Mapping for FPGA
2. Placement for FPGA
3. Floorplanning for FPGA
4. Routing for FPGA
5. Timing Optimization Techniques for FPGA
6. Power Optimization Techniques for FPGA
7. Pin Assignment for FPGA
8. CAD for 2.5D FPGAs

Grading Assignments: 50%
Survey & presentation of research papers: 20%
Final project: 30%

General Policies

1. Discussions of homework problems with other students are encouraged. However, every student MUST do his/her own work and write up the solutions independently.
2. A 10% late penalty per day will be applied to all late assignments. Assignments should be turned in at the beginning of class on the due date.
3. Students who violate University rules on scholastic dishonesty are subject to disciplinary penalties, including the possibility of failure in the course and/or dismissal from the University. Since such dishonesty harms the individual, all students, and the integrity of The University, policies on scholastic dishonesty will be strictly enforced.