Routing Architecture Design Basics

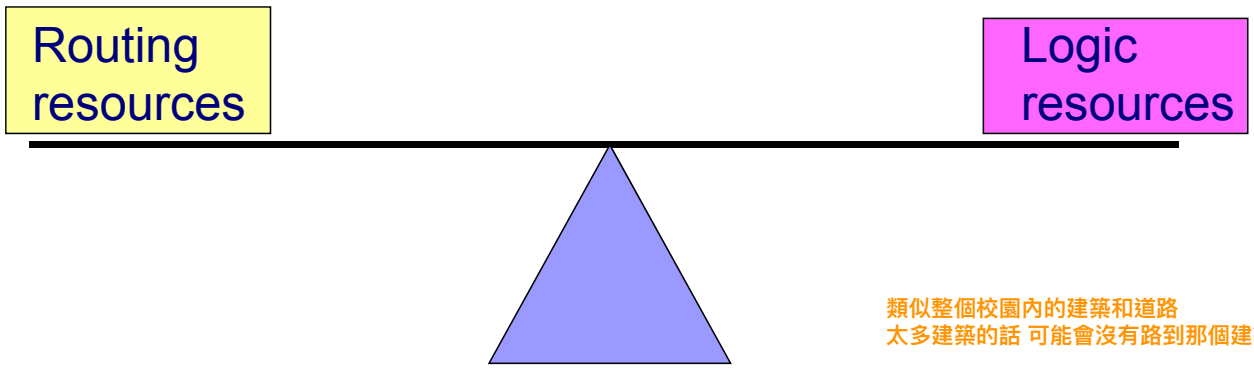
Topics

- Tradeoffs: area, routability, performance
- Architecture
  - Segmented wiring
  - Switch boxes
  - Connection boxes

Routing Architecture

- Determines the way in which wiring segments and programmable switches are positioned.
- Three concerns:
  - Area
  - Routability
  - Performance
- *Routability* – capability to accommodate all signal nets of a design.
- *Performance* – keep propagation delay low.

Importance of Routing Architecture

- Engineers found that 60% logic utilization was good, 70% great, and 80% a practical impossibility. *Why?* 用太多logic resources可能造成route不出來的情況
- 

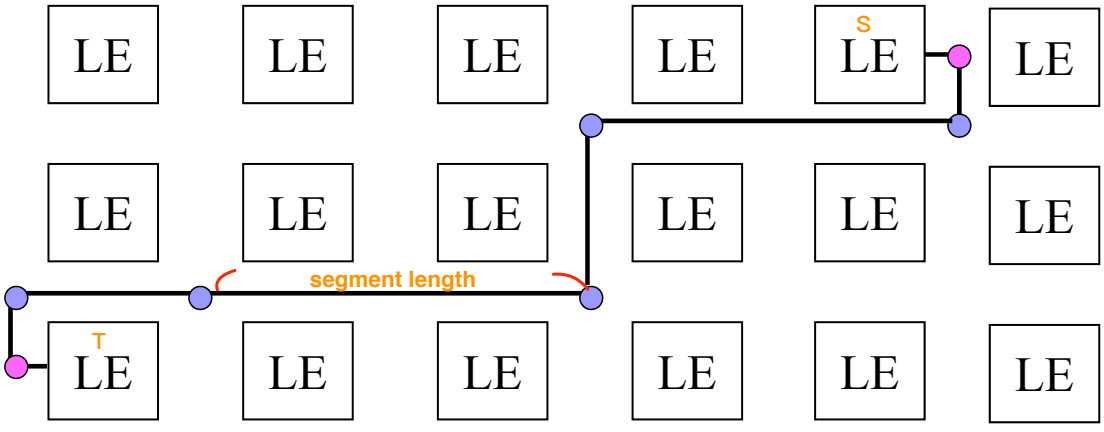
Competing for die area

Interconnect strategies for FPGA

- Observation:
  - Some nets are short, some are long
- Solution:
  - Provide different types of wires:
    - Short wires: local LE connections.
    - Global wires: long-distance, buffered communication.
    - Special wires: clocks, etc.

Paths in Programmable Interconnect

- How to make connection from LE to channel?
- How to make connection between channels?

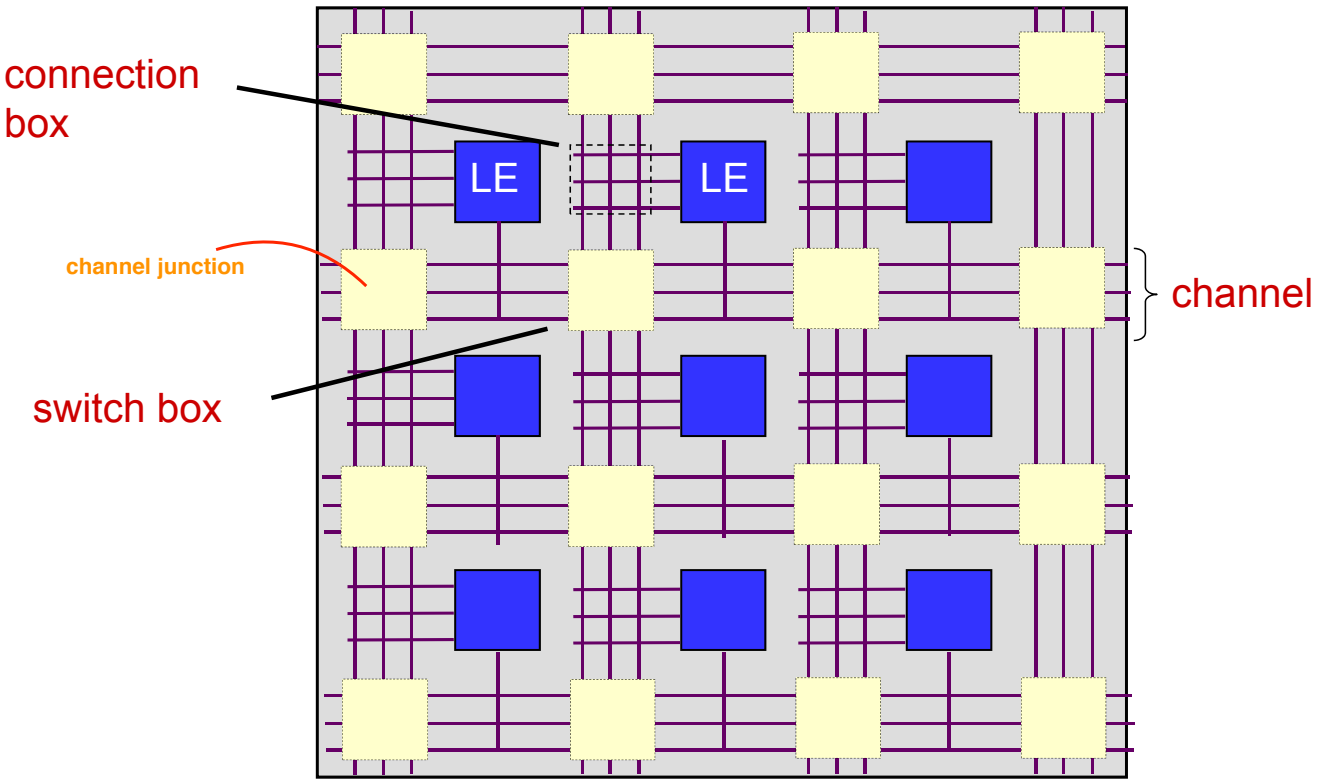


Interconnect Richness

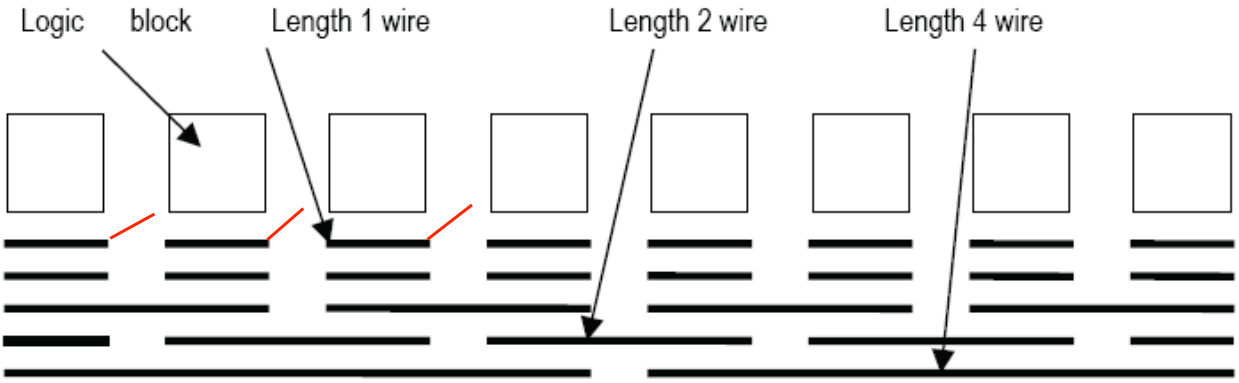
- Within a channel:
  - How many wires?
  - Length of segments?
  - Number of connections from LE to channel?
- Between channels:
  - Number of connections between channels?
  - Channel structure?

直的和橫的在junction內怎麼連接

Interconnect Network



Channel Segmentation



都有switch 決定要不要連

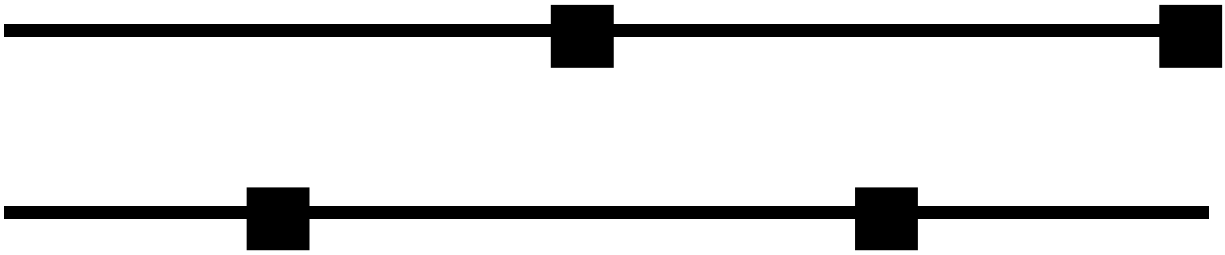
Segmented Wiring

Length 1 較靈活 但要經過較多的switches, worse performance

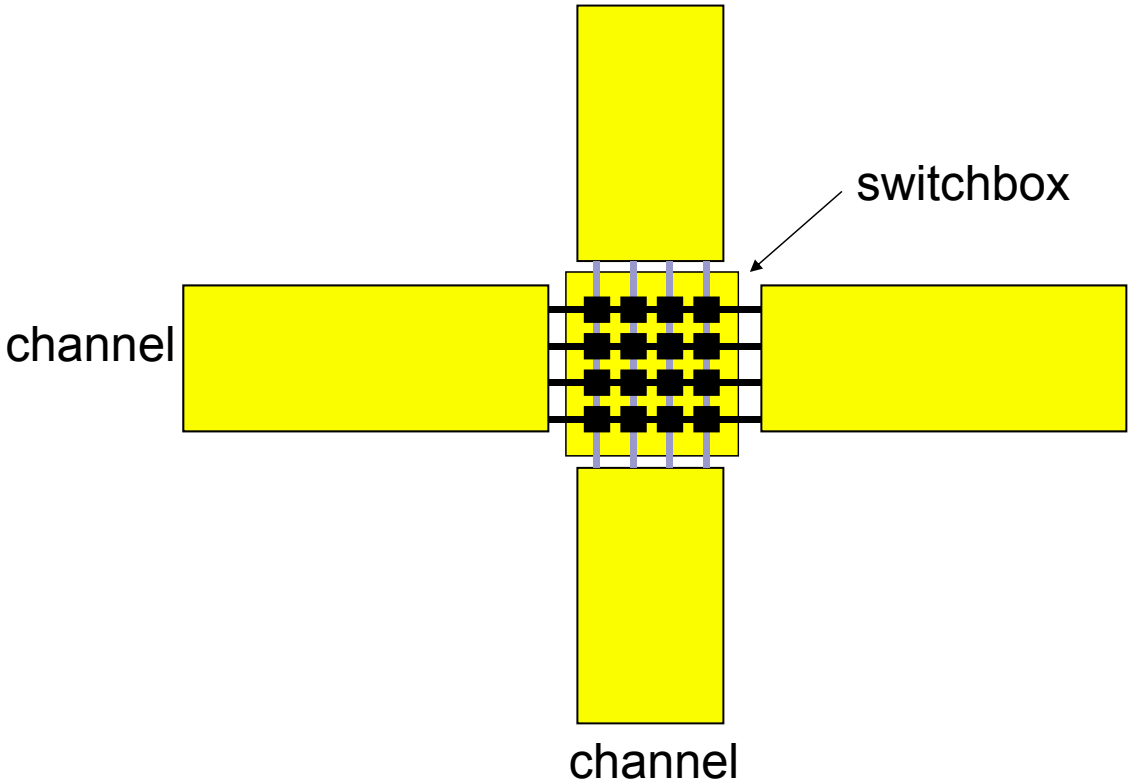
Length 2

Offset Segments

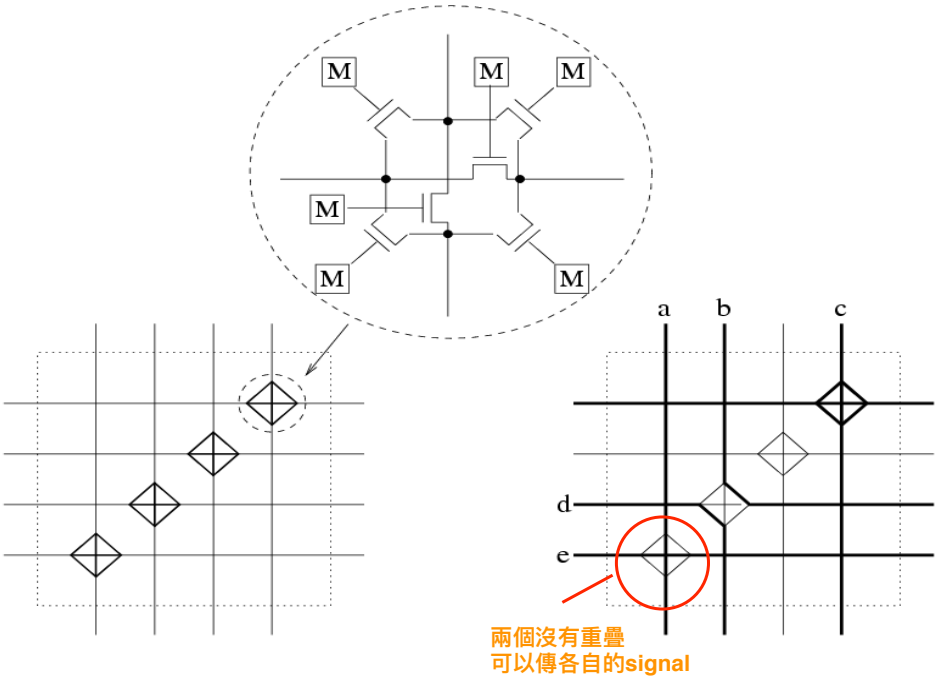
錯置



Connections between Channels: Switchbox Design



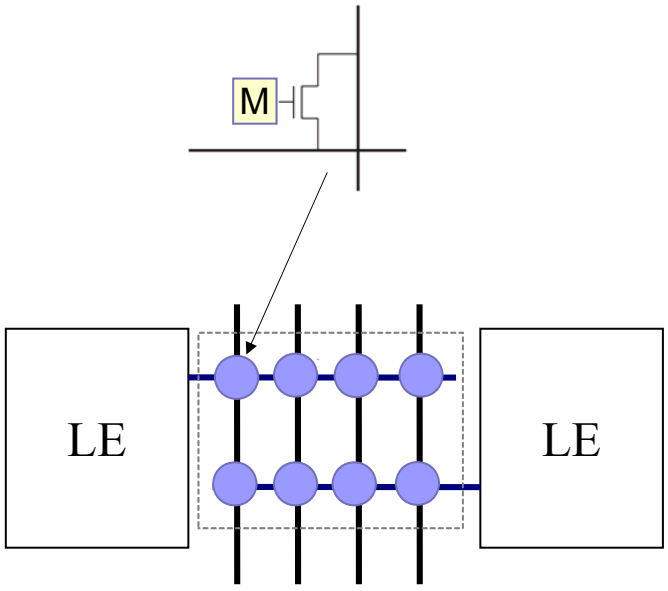
Switch Box Implementation



A Switch Box

Example routing of 5 nets

Connections from LE to Channel: Connection Box Design



Connection box

Drawbacks of Programmable Interconnect

- Switches add delay.
- Transistor off-state is worse in advanced technologies.
- FPGA interconnect has extra length ⇒ added capacitance.
- Some wires will not be utilized.

leakage power

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