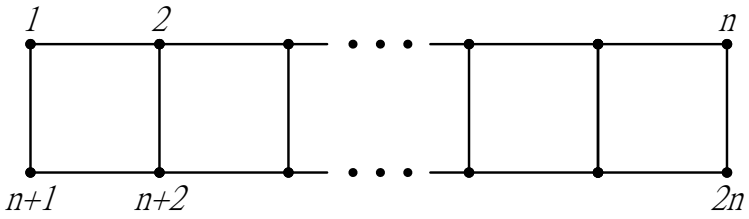
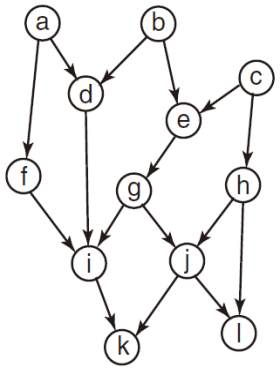
CS 6135 VLSI Physical Design Automation
Final Exam: 3:30 p.m. - 6:30 p.m., June 7, 2016

1. (10 points) Consider the following ladder graph with 2*n* vertices, and an initial bipartition *A*={1, 2,…, *n*} and *B*={*n*+1, *n*+2,…, 2*n*}. Prove that the given initial bipartition is a local minimum if only one step (i.e., exchanging one pair of vertices) of the Kernighan-Lin (KL) algorithm is applied.



2. (15 points) Assume the area of each gate is 1 unit, the area constraint of each cluster is 3 units, each gate delay is 1 unit, and the interconnection delay between two clusters is 2 units. Show your work by applying the clustering algorithm discussed in class to find *l*(e), *l*(g), *l*(h), *l*(j), *cluster*(e), *cluster*(g), *cluster*(h), and *cluster*(j).



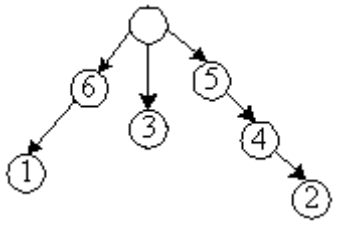
3. Consider the Polish expression *E*=123*H*4*V*56*HHV*.
   (a) (3 points) Does *E* have the balloting property? Justify your answer.
   (b) (3 points) Draw the slicing tree for *E* and determine whether it is skewed.
   (c) (9 oints) Assume modules 1, 2, ..., 6 are all hard modules with shapes given in the following table. Besides, each module can be rotated by 90-degree. Use the Stockmeyer algorithm to find a minimum-area floorplan for *E* as well as the shape of each module that achieves the minimum-area floorplan.

Module	Width	Height
1	2	1
2	2	2
3	3	1
4	2	3
5	1	2
6	2	2

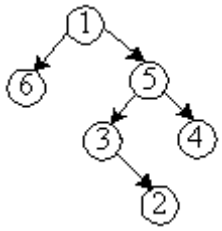
4. Consider the set of modules given in Problem 3, but assume that module rotation is not allowed.

(a) (7 points) Show your work for finding a minimum-area placement for the sequence-pair (135624, 562134).

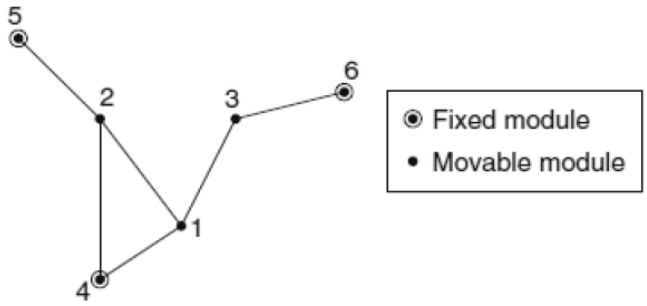
(b) (4 points) Show the placement for the following horizontal O-tree.



(c) (4 points) Show the placement for the following B*-tree.



5. (10 points) Consider a circuit with three movable modules and three fixed modules as represented by the following graph.

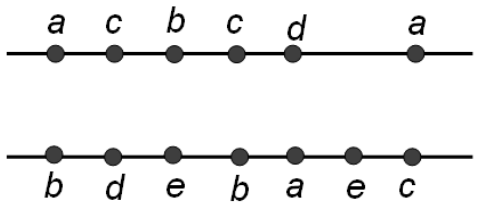


For the three fixed modules, module 4 is at (5, 5), module 5 is at (0, 20), and module 6 is at (25, 15). Assume all nets have a weight of 1. Determine Q, d_x, and d_y such that the cost function of quadratic placement for this circuit can be written as follows:

$$\frac{1}{2}x^T Qx + d_x^T x + \frac{1}{2}y^T Qy + d_y^T y + \text{const}$$

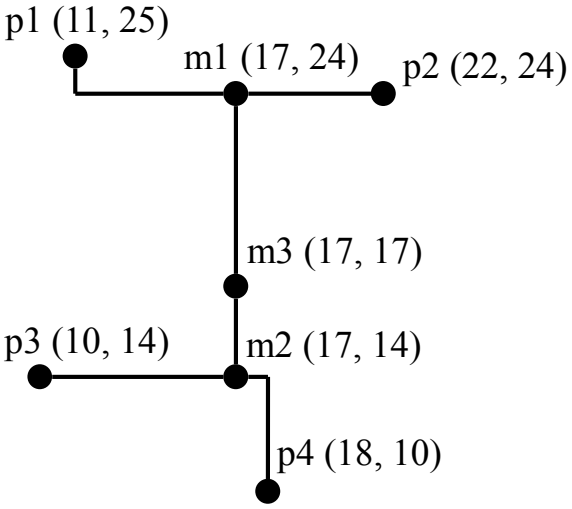
6. (10 points) In class we claimed that the BoundingBox net model (or called the Bound2Bound model) can accurately model HPWL in a quadratic placement framework. Prove this claim for the *x* direction.

7. Consider the following two-layer channel routing instance under the reserved HV routing layer model.



(a) (2 points) What is the channel density?
(b) (4 points) Draw the horizontal constraint graph (HCG) and vertical constraint graph (VCG).
(c) (3 points) Is the constrained left-edge algorithm applicable to this channel routing instance? If your answer is yes, you need to show the routing result produced by the constrained left-edge algorithm; otherwise, you need to explain why the constrained left-edge algorithm fails to do so.
(d) (6 points) Is the dogleg channel router applicable to this channel routing instance? If your answer is yes, you need to show the routing result produced by the dogleg channel router which alternates the routing directions: top, bottom, top, bottom,…; otherwise, you need to explain why the dogleg channel router fails to do so.

8. A routing tree for four clock pins p1, p2, p3, and p4 is given below. Suppose m1 is the tapping point for (p1, p2), m2 is the tapping point for (p3, p4), and m3 is the tapping point for (m1, m2). (Note that it is possible that a tapping point may not achieve zero skew in this problem.) The coordinates of p1, p2, p3, p4, m1, m2, and m3 are also shown below. The loading capacitances of p1, p2, p3, and p4 are $2F$, $1F$, $4F$ and $2F$, respectively. The per unit values of resistance and capacitance of a wire segment are $\alpha = 0.1\Omega$ and $\beta = 0.2F$, respectively. The point m3 is the final clock entry point. Assume the π-model is used for wires, and the Elmore delay model (i.e., the RC delay model discussed in class) is used for calculating delays.



(a) (6 points) What are the delay and skew of the routing tree?
(b) (4 points) If two identical buffers with resistance $r_b = 0.2\Omega$ and capacitance $c_b = 0.5F$ are inserted at m1 and m2, respectively, what are the resultant delay and skew? (Assume the switch-resistor model discussed in class is used for buffers, and the intrinsic delay of each buffer is negligible.)