CS5120 00
GCD Engine

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HW 01

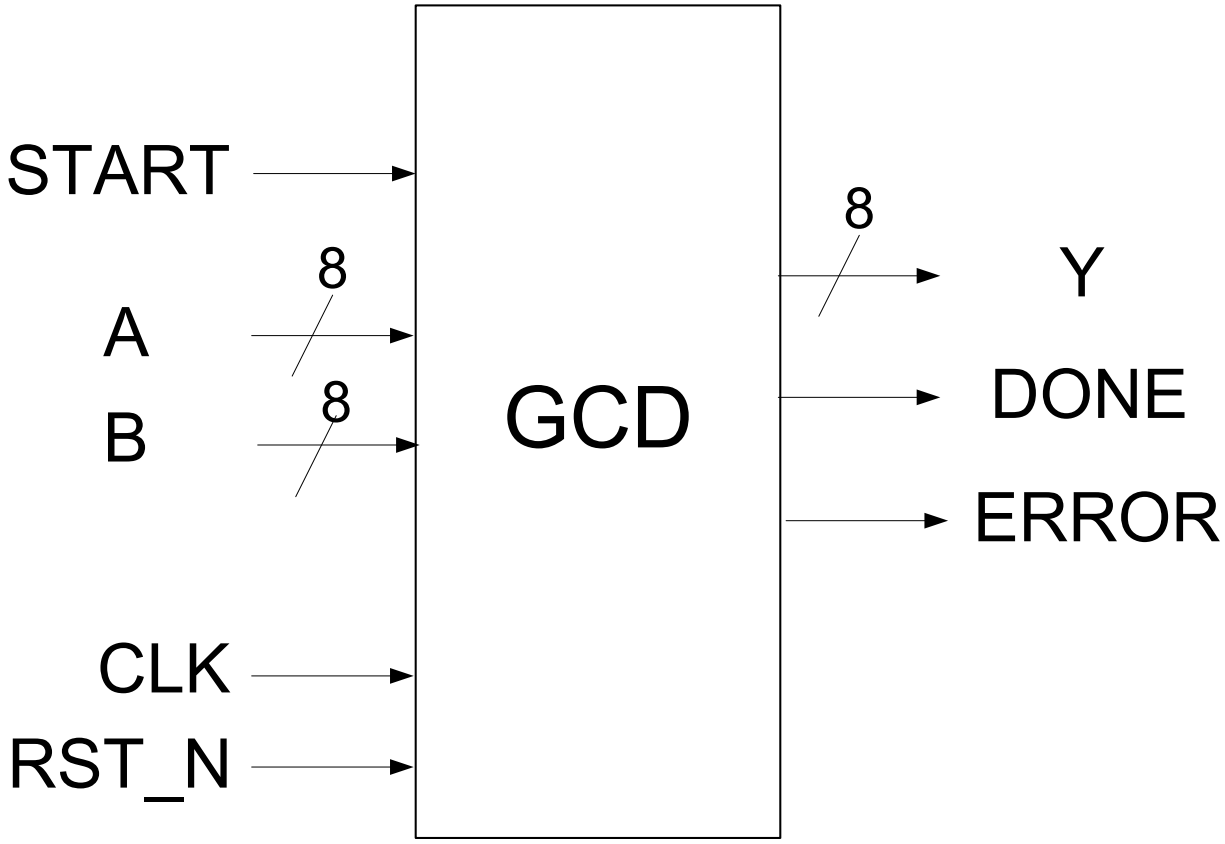
Description

- Calculate the greatest common divisor (GCD) of two 8-bit positive integers
- Using a START signal to load inputs
- Generate a DONE signal to indicate the result
- Assert an ERROR signal when one or more inputs are zero

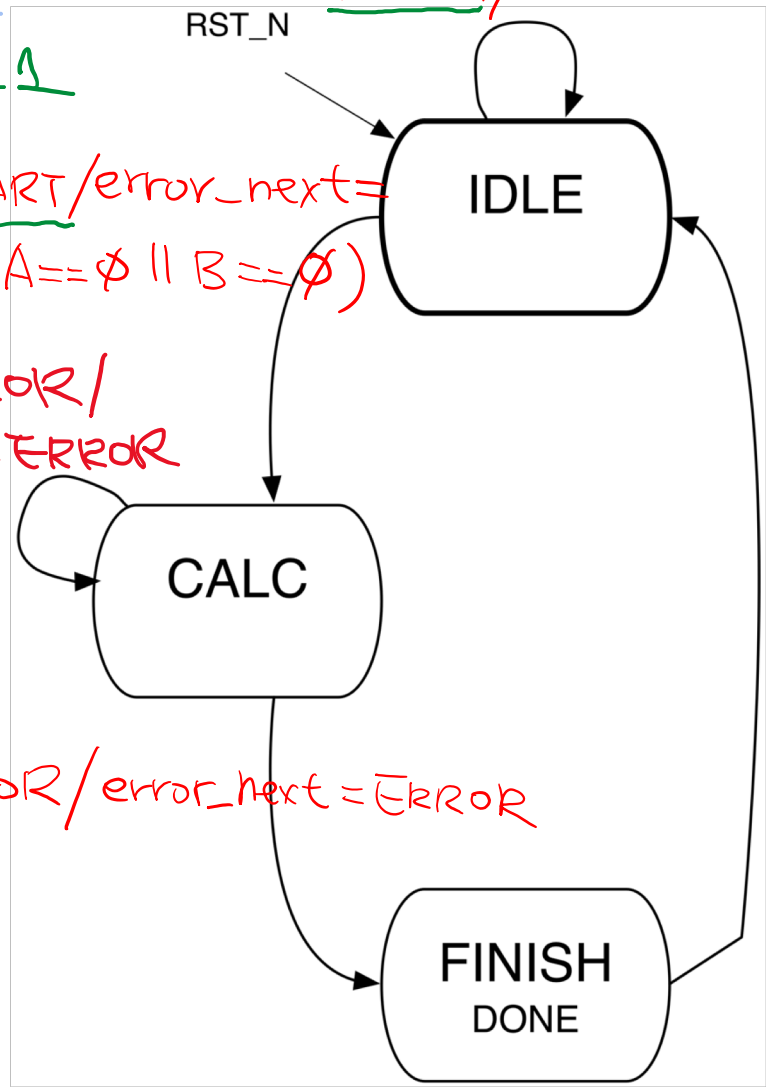
IO Specification

- Inputs:
  - *CLK*: clock source
  - *RST_N*: reset (low active)
  - *START*: to trigger the calculation
    - A one-cycle pulse to indicate the valid input numbers
  - *A, B*: two 8-bit input numbers
- Outputs:
  - *Y*: the result
  - *DONE*: to indicate the valid output with one-cycle pulse
  - *ERROR*: to indicate an error
    - 0: normal result
    - 1: invalid when A = 0 or B = 0

Primary IOs and Block Diagram



Finite State Machine (for Control)



START==0

!START/error_next=0

START==1

START/error_next=

(A==0 || B==0)

error_next → D → ERROR

clk

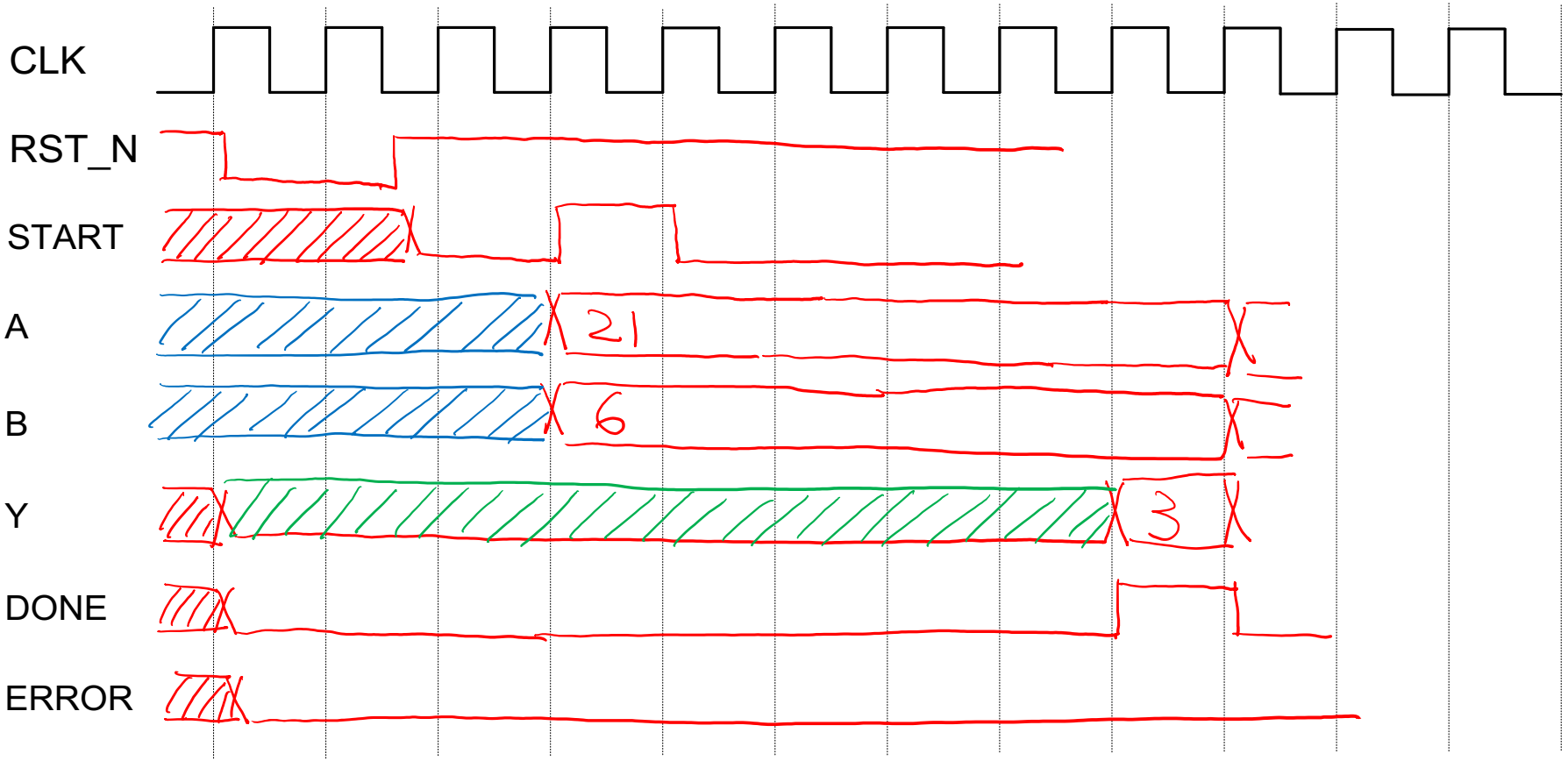
!found && !ERROR/

error_next=ERROR

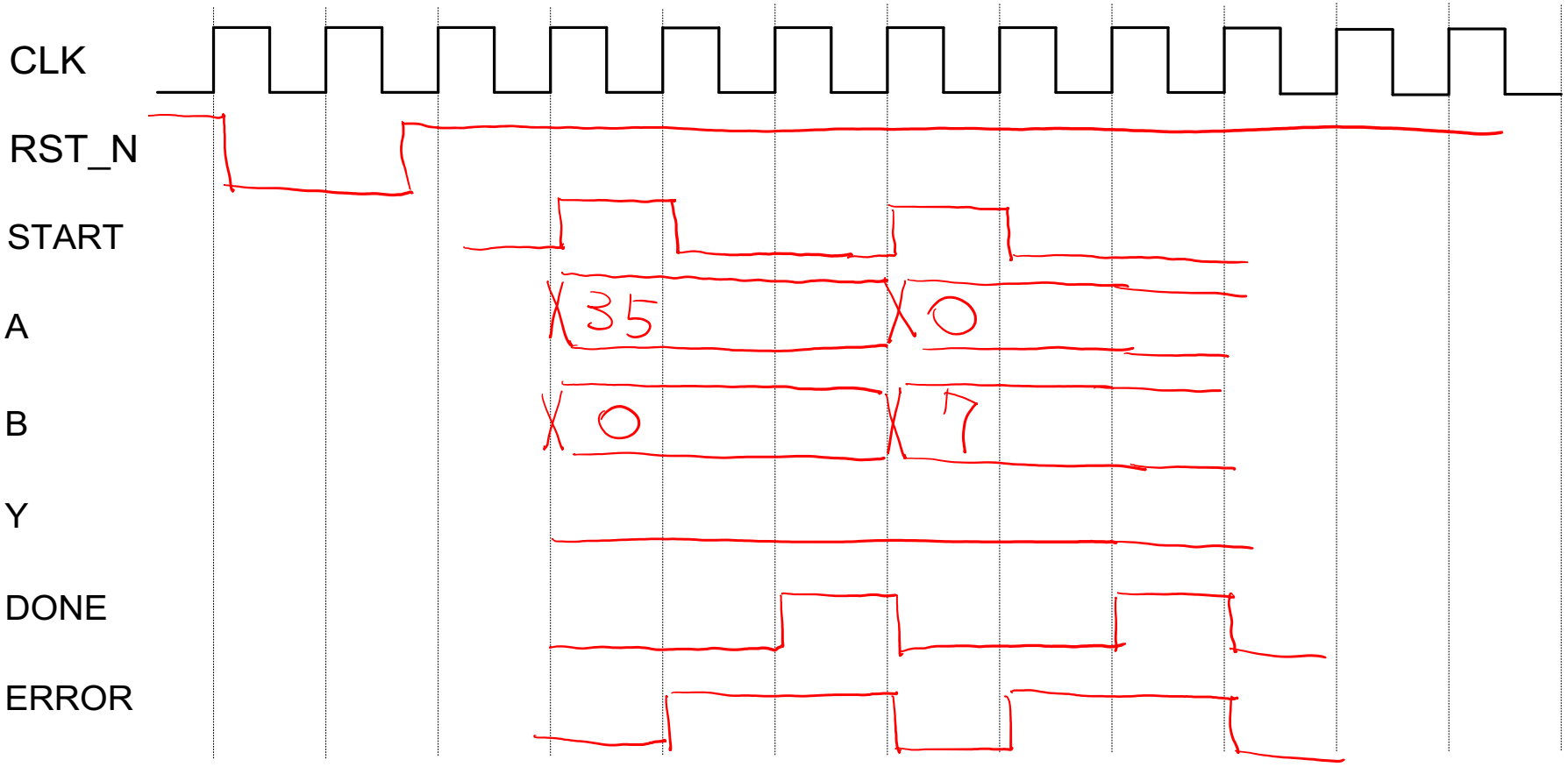
found || ERROR/error_next=ERROR

-/error_next=0

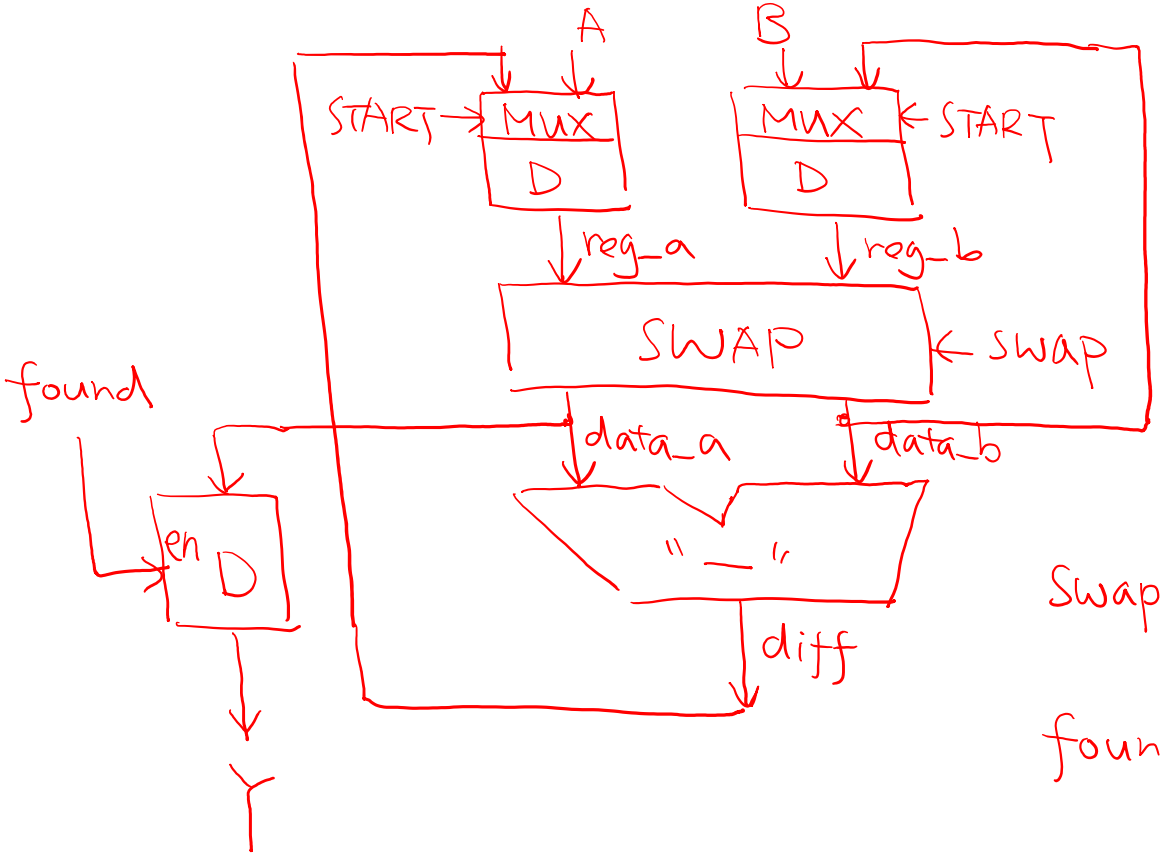
Timing Diagram – Normal Operation



Timing Diagram – Error



Overall Architecture (Block Diagram)

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Swap = (reg_b > reg_a) ? 1'b1 : 0;

found = (reg_a == reg_b || A == B) ?
        1'b1 : 0;
```

Design Procedure

- Start with spec, primary IOs, and block diagram
- Design the overall architecture
- Specify finite state machine(s), data path, and internal signals
- List the timing diagrams of major operations
- Verilog coding
- Prepare comprehensive test environment for efficient debugging

Guideline of Design Procedure

- Prepare the block diagram and FSM carefully
- Try to symbolize every condition for
  - State transitions
  - Mode selection for datapath
- FSM: the simpler the better
  - One single state can take multiple cycles
  - States can be nested
- Design should be done before Verilog coding
- There is no one BEST style for every design
  - State arrangement
  - Naming convention