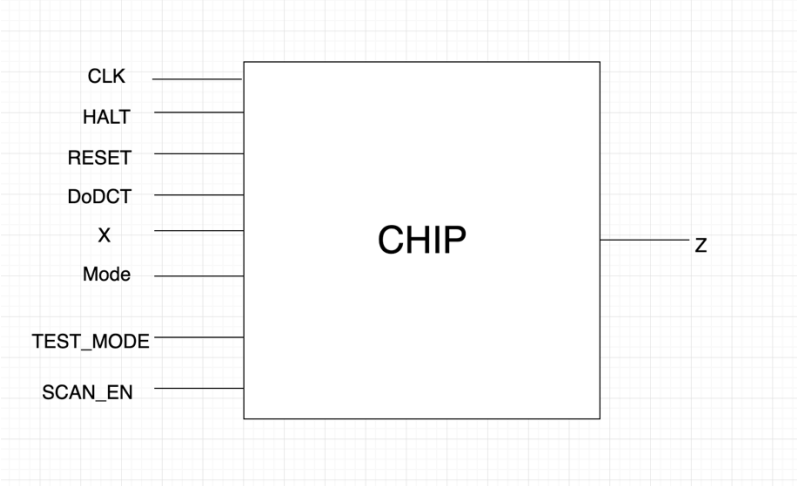
CS5120 LAB

Student ID: 104062135 Name: 魏聖修

1. 從 CHIP.v 裡的 module 來看，我想這個 design 要做的是 Discrete Cosine Transform & Inverse Discrete Cosine Transform.



2. 我主要遇到的問題就是對於操作這個軟體不是很熟悉，所以花費了大量的時間，估計分了 3 次做，每次 3～4 小時。不過都慢慢點順利地完成了。其中花比較多的時間的是，為了解決 DRC violation，要去手動操作 stretch 和刪 via 的部分。另外，最後 LAB11 可能是因為分很多次做，沒有做成功。

3.

Performance 因為其實還是不太清楚這個 design，所以我覺得不太好評斷。

Area 我目前是依照那個 tool 裡面的 ruler 量去算出來的，920.210 * 792.182。

Power consumption

```
Total Power
-----------------------------------------------------------
Total Internal Power:        6.66019548        58.0296%
Total Switching Power:       1.55686835        13.5648%
Total Leakage Power:         3.26016847        28.4055%
Total Power:                11.47723234
-----------------------------------------------------------
```

4.

這次的 lab 有附上很完整的教學，而且讓我們從頭試著做到尾其實蠻有趣的，之前的課程也有用過另一套 APR 軟體，操作好像有簡單一點，但是選項沒有這麼多。不過共同點是很多部分其實都不了解到底為何要這樣選，希望有時間能了解透徹一點。

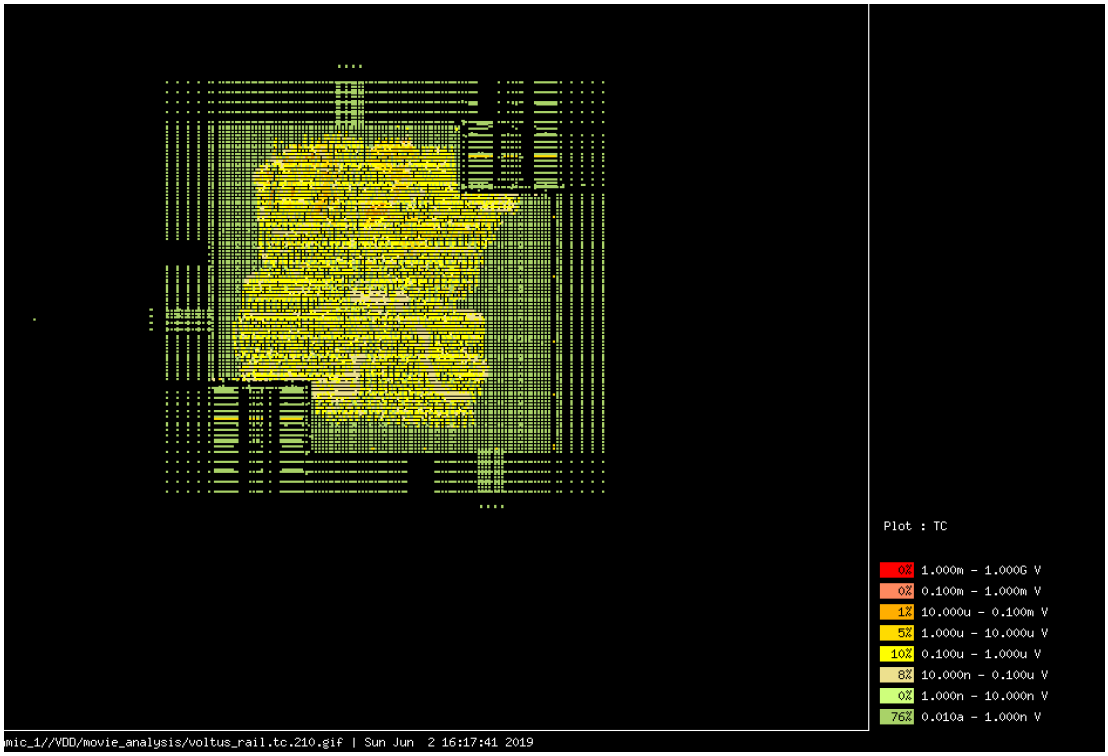
另外，final project 的部分好像有點蠻難做的，我也會盡我全力去盡量做到最好，希望助教和老師可以給好一點的成績。謝謝老師和助教。

LAB7

1.

```
IO                              2.099      0.1556        1.07       3.324       28.97
Combinational                  0.9411      0.5927      0.7985       2.332       20.32
Clock (Combinational)          0.2687      0.5858     0.02593      0.8804       7.671
Clock (Sequential)            0.04886    0.008588    0.006697     0.06415      0.5589
-------------------------------------------------------------------------------------
Total                            6.66       1.557        3.26       11.48         100
-------------------------------------------------------------------------------------


Rail                  Voltage   Internal   Switching     Leakage       Total  Percentage
                                Power      Power         Power         Power  (%)
-------------------------------------------------------------------------------------
VDD                      1.25      4.561       1.401        2.19       8.153       71.03
Default                  0.95      2.099      0.1556        1.07       3.324       28.97


Clock                           Internal   Switching     Leakage       Total  Percentage
                                Power      Power         Power         Power  (%)
-------------------------------------------------------------------------------------
CLK1                             0.8176       0.606     0.07349       1.497       13.04
-------------------------------------------------------------------------------------
Total (excluding duplicates)     0.8176       0.606     0.07349       1.497       13.04
-------------------------------------------------------------------------------------

Clock: CLK1
Clock Period:               0.008 usec
Clock Toggle Rate:   250.0000 MHz
Clock Static Probability:  0.5000



-------------------------------------------------------------------------------------
*   Power Distribution Summary:
*               Highest Average Power:                ipad_CLK (PADIN):          0.5525
*               Highest Leakage Power: u_DCT/tposemem_Bisted_RF_2P_ADV64x16_RF_2P_ADV64x16_u0_SRAM_i0 (rf_2p_hse):          0.1227
*          Total Cap:      3.13224e-10 F
*          Total instances in design: 10612
*          Total instances in design with no power:    29
*          Total instances in design with no activity:    14
*          Total Fillers and Decap:    10
-------------------------------------------------------------------------------------
```

2.

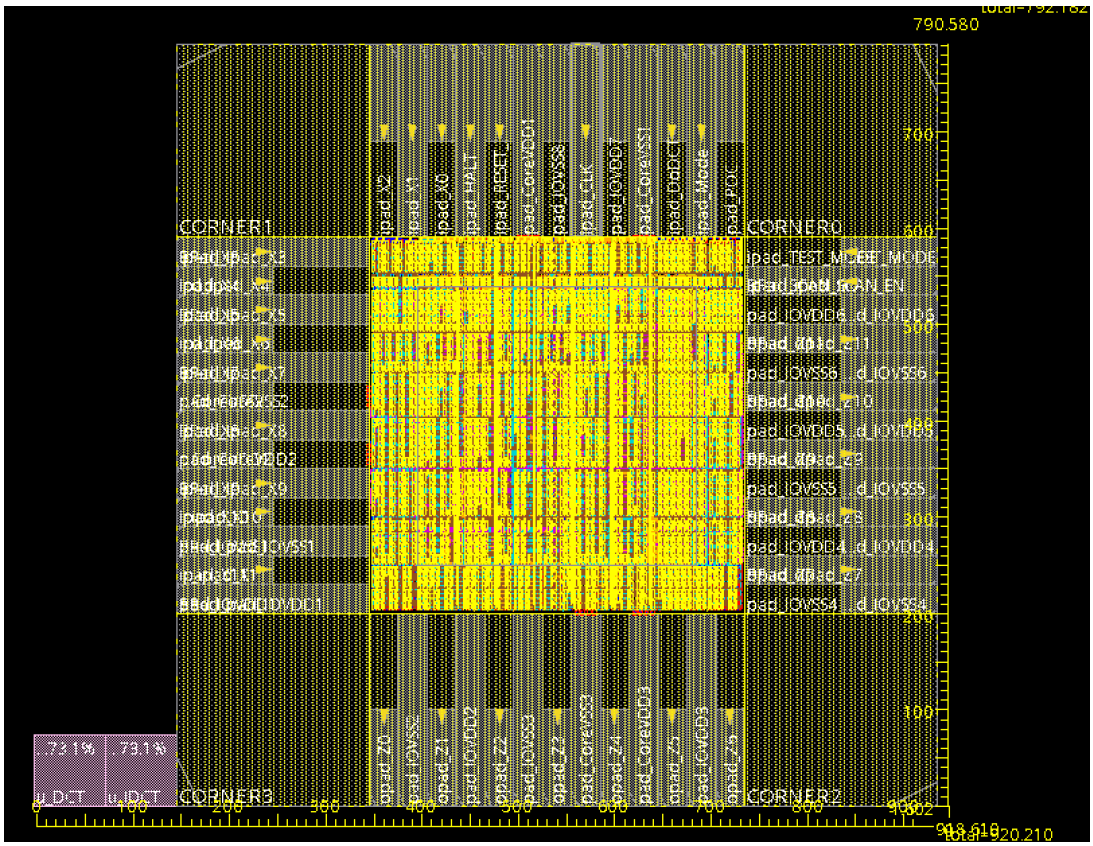


3.

```
                    streams:   0, words:     0
               worklib.retiming_state_point_4159_8:v <0x7e084822>
                    streams:   0, words:     0
               worklib.retiming_state_point_4159_9:v <0x695b66ad>
                    streams:   0, words:     0
               worklib.retiming_state_point_4:v <0x7cbcb6d6>
                    streams:   0, words:     0
               worklib.retiming_state_point_5:v <0x680fd561>
                    streams:   0, words:     0
               worklib.retiming_state_point_6:v <0x5362f3ec>
                    streams:   0, words:     0
               worklib.retiming_state_point_7:v <0x3eb61277>
                    streams:   0, words:     0
               worklib.retiming_state_point_8:v <0x2a093102>
                    streams:   0, words:     0
               worklib.retiming_state_point_9:v <0x155c4f8d>
                    streams:   0, words:     0
               worklib.test:v <0x3b4c2dd1>
                    streams:  13, words:  9485
       Building instance specific data structures.
       Loading native compiled code:     ..................... Done
       Design hierarchy summary:
                                  Instances  Unique
               Modules:               11046     531
               UDPs:                  13243       9
               Primitives:            58319       5
               Timing outputs:        15951     268
               Registers:              3671     203
               Scalar wires:          19916       -
               Expanded wires:          100       9
               Always blocks:           186      95
               Initial blocks:           24      16
               Cont. assignments:        30     534
               Pseudo assignments:        1       1
               Timing checks:         47201   10538
               Interconnect:          31295     316
               Delayed tcheck signals:  13238    6398
               Simulation timescale:     1ps
       Writing initial simulation snapshot: worklib.test:v
Loading snapshot worklib.test:v ..................... Done
*Verdi3* Loading libsscore_ius141.so
*Verdi3* : Enable Parallel Dumping.
ncsim> source /usr/cad/cadence/INCISIV/cur/tools/inca/files/ncsimrc
ncsim> run
block          0
block          1
block          2
block          3

RESULT CORRECT

Simulation complete via $finish(1) at time 1906 NS + 0
./CHIP_sim.v:79     $finish;
ncsim> exit
[zscaxd5651@ic57 post_sim]$
```

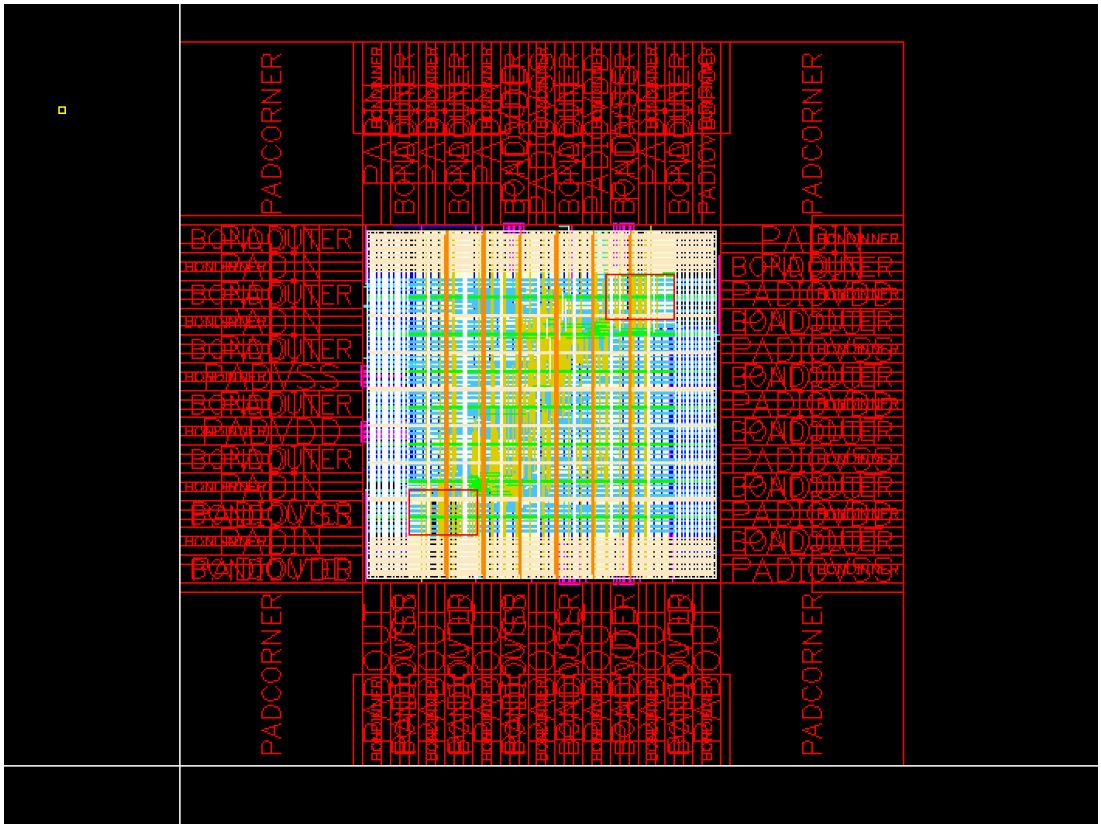
LAB8

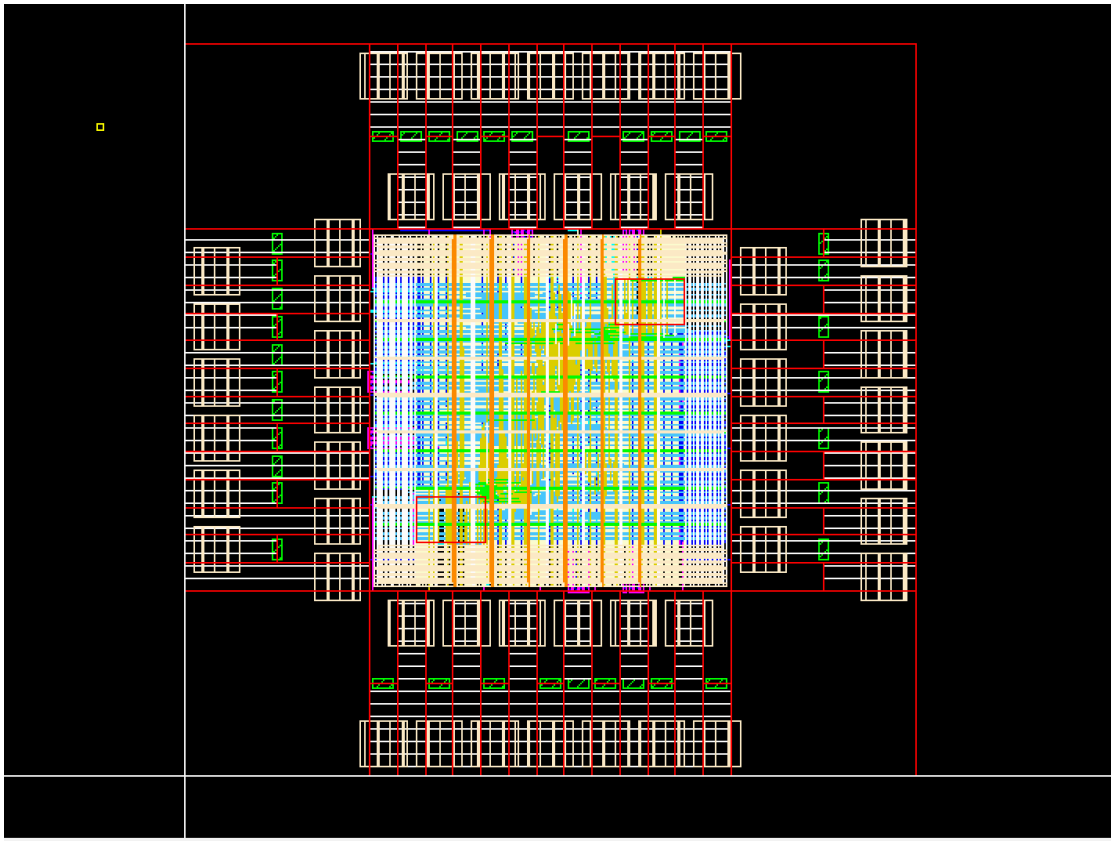
1.



CORE AREA: 920.210 * 792.182 = 728973.8(units^2)

LAB9





LAB10

DRC

```
Cumulative ONE-LAYER BOOLEAN Time: CPU = 0  REAL = 0
Cumulative TWO-LAYER BOOLEAN Time: CPU = 1  REAL = 1
Cumulative SIZE Time: CPU = 1  REAL = 1
Cumulative EDGE TOPOLOGICAL Time: CPU = 1  REAL = 1
Cumulative EDGE MEASUREMENT Time: CPU = 0  REAL = 0
Cumulative ONE-LAYER DRC Time: CPU = 2  REAL = 2
Cumulative TWO-LAYER DRC Time: CPU = 0  REAL = 0
Cumulative NET AREA (RATIO) Time: CPU = 0  REAL = 0
Cumulative MISCELLANEOUS Time: CPU = 1  REAL = 1
Cumulative CONNECT Time: CPU = 3  REAL = 3
Cumulative RDB Time: CPU = 0  REAL = 0

--- CALIBRE::DRC-F EXECUTIVE MODULE COMPLETED.  CPU TIME = 14  REAL TIME = 14
--- TOTAL RULECHECKS EXECUTED = 167
--- TOTAL RESULTS GENERATED = 0
--- DRC RESULTS DATABASE FILE = DRC_RES.db (ASCII)

--- CALIBRE::DRC-F COMPLETED - Mon Jun  3 22:28:27 2019
--- TOTAL CPU TIME = 14  REAL TIME = 14
--- SUMMARY REPORT FILE = DRC.rep
```

LVS

```
REPORT FILE NAME:         lvs.rep
LAYOUT NAME:              layout.spi ('CHIP')
SOURCE NAME:              source.spi ('CHIP')
RULE FILE:                calibreLVS.rul
RULE FILE TITLE:          LVS Rule File for FreePDK45
HCELL FILE:               (-automatch)
CREATION TIME:            Mon Jun  3 22:31:00 2019
CURRENT DIRECTORY:        /users/student/topic/zscaxd5651/VLSI_System_Design/LAB/Lab_nangate/innovus/Lab10/lvs
USER NAME:                zscaxd5651
CALIBRE VERSION:          v2012.2_26.20    Thu Jun 14 11:44:29 PDT 2012


                            OVERALL COMPARISON RESULTS


                       #      ##################       _   _
                      #       #                #       *   *
                  #   #       #    CORRECT     #         |
                   # #        #                #       \___/
                    #         ##################


********************************************************************************************************************
                                    CELL  SUMMARY
********************************************************************************************************************

  Result         Layout                       Source
  -----------    -----------                  -------------
  CORRECT        CHIP                         CHIP
```