Homework Assignment 02

Extended GCD Engine with Synthesis

Based on the GCD engine in the previous homework assignment, extend your design to support GCD calculation of two 16-bit positive integers with the same IOs.

➔ The IO names and widths remain the same.
- A, B, and Y are still 8-bit signals.
- You need two cycles to complete the data transfer.
  - E.g., the 1st cycle for A[15:8]; the 2nd cycle for A[7:0]
- In addition, the START and DONE are also extended to two-cycle signals.
  - Assume they are asserted for two consecutive cycles.
  - (Discussion) Can you support the control either with two consecutive cycles and two separate active cycles?

Requirements

1. Define the specification of the extended GCD engine. Discuss any modifications you need (e.g., FSM, datapath, timing, etc.), if necessary.
2. Complete the RTL design and its test stimulus in Verilog.
3. Synthesize the RTL design to the gate-level implementation.
4. Verify the design by covering as many input conditions as you can. Discuss your selection of test patterns. Compare your RTL and gate-level simulation.
5. Discuss the area/timing/power reports.
6. (Discussion) Is there any room of improvement regarding to the timing.
7. Write a summary report.

Note:

➔ This is a graduate-school-level homework assignment. Make reasonable assumptions or raise a discussion if there is any detail needed to be more specific.

➔ For each assignment, you are requested to write a report with your name and student ID. The topics should include, but are not limited to, the following items:
   a. The design concept with figure and description;
   b. Simulation result with explanation, including the discussion about problems you encounter, and the way you solve them (or not);
   c. A brief summary, including suggestions for us (or this course).

   DO NOT put the entire source code into the report without proper explanation!

➔ The report file should be hw01_YourStudetID.pdf

➔ Submit the source files and the electrical report based on TA's instructions.

➔ The source files may include the followings (I assume that you can know what these files are for from their naming):

- RTL designs: hw02.v
- Testbenches: hw02_t.v
- Gate-level implementation: hw02_syn.v
- SDF file from the Design Compiler: hw02_syn.sdf
- FSDB waveforms: hw02.fsdb, hw02_syn.fsdb
- Document: README.txt to briefly describe how to perform all the simulations
- (Optional) Makefile (if you use your own Makefile)
- (Optional) hw02.f (if you have your own one)
- (Optional) Other files or documents for your designs and simulations to fulfill the requirement of this assignment. Put the details in your report and README.txt
- The PDF report: hw02_YOUR-STUDENT-ID.pdf

DO NOT hand in compressed files.

Assignment due on 3/16/2019, 23:30

1. Submit your source designs and the report.
   - No overdue is allowed.
   - Submission rules will be strictly enforced.