Homework Assignment 01

GCD Engine

Please refer to the slides for the details of the GCD Engine.

Requirements

1. Complete the design in Verilog.
2. Verify the design by covering as many input conditions as you can. Discuss your selection of test patterns.
3. Debug the timing by using waveform viewer nWave.
4. (Discussion) Is there any room of improvement regarding to the timing.
5. Write a summary report.

Note:

➔ This is a graduate-school-level homework assignment. Make reasonable assumptions or raise a discussion if there is any detail needed to be more specific.

➔ For each assignment, you are requested to write a report with your name and student ID. The topics should include, but are not limited to, the following items:

a. The design concept with figure and description;
b. Simulation result with explanation, including the discussion about problems you encounter, and the way you solve them (or not);
c. A brief summary, including suggestions for us (or this course).

DO NOT put the entire source code into the report without proper explanation!

➔ The report file should be hw01_YourStudetID.pdf

➔ Submit the source files and the electrical report based on TA's instructions.

➔ The source files may include the followings (I assume that you can know what these files are for from their naming):

- RTL designs: hw01.v
- Testbenches: hw01_t.v
- Document: README.txt to briefly describe how to perform all the simulations
- FSDB waveforms: hw01.fsdb
- (Optional) Makefile (if you use your own Makefile)
- (Optional) hw01.f (if you have your own one)
- (Optional) Other files or documents for your designs and simulations to fulfill the requirement of this assignment. Put the details in your report and README.txt

Assignment due on 3/2/2019, 23:30

1. Submit your source designs and the report.
   - No overdue is allowed.
   - Submission rules will be strictly enforced.