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IPC-2252

Design Guide for RF/ Microwave Circuit Boards

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Developed by the High Speed/High Frequency Design Task Group (D-21b) of the High Speed/High Frequency Committee (D-20) of IPC

Supersedes:
IPC-D-316 - June 1995

Users of this standard are encouraged to participate in the development of future revisions.

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Acknowledgment

Any Standard involving a complex technology draws material from a vast number of sources. While the principal members of the High Speed/High Frequency Design Task Group (D-21b) of the High Speed/High Frequency Committee (D-20) are shown below, it is not possible to include all of those who assisted in the evolution of this standard. To each of them, the members of the IPC extend their gratitude.

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Design Guide for RF/Microwave Circuit Boards

1 GENERAL

1.1 Purpose The purpose of this document is to aid in the design of manufacturable microwave circuit boards. This document is not intended to include information relating to the detailed electrical design of microwave circuits. Rather, it is intended to include information from which practical, functional, and cost-effective circuit boards may be designed once the design engineer has determined the circuit requirements. The document also provides information on the manufacturing options available to the designer for the achievement of realistic and cost-effective circuit designs. This design aid is to be used by RF and microwave circuit design engineers, printed wiring board designers, packaging engineers, and drafters.

1.2 Scope This document addresses microwave circuitry. For the purpose of this document microwaves apply to radio waves in the frequency range of 100 MHz to 30 GHz. The document also applies to operations in the region where distributed circuits are used instead of conventional lumped circuit elements.

1.3 Terms and Definitions

Anisotropy The condition for a substance having differing values for properties, such as permittivity, depending on the direction within the material. Isotropy describes the case where a property is the same in all directions. Isotropy may exist in non-crystalline homogeneous (single phase) substances. In a microwave laminate based on a polymer composite, anisotropy of the dielectric layer exists.

***Characteristic Impedance* (Z_O)** A transmission line parameter dependent on the distributed series impedance per unit length and the distributed shunt admittance per unit length of the transmission line. The series impedance is given by $R + j\omega L$ and the shunt admittance by $G + j\omega C$, where R,L,G, and C are the resistance, inductance, conductance, and capacitance per unit length of the transmission line, j is $\sqrt{-1}$ and ω is the angular frequency. The characteristic impedance, Z_0, is the square root of the ratio of the impedance to the admittance.

***Coaxial Cable* (Coax)** A transmission line (see Transmission Line) structure where a round signal conductor centered coaxially inside a round tubular return (ground) conductor. The inside diameter of the return conductor is greater than the outside diameter of the signal conductor.

***Coefficient of Thermal Expansion* (CTE)** The linear dimensional change of a material per unit change in temperature.

Copper Weight The mass of copper per unit area for a foil. The copper foil industry typically expresses weight in ounces per square foot (oz/ft^2). A copper foil weight of 1 oz/ft^2 corresponds to a nominal 34 µm [1350 µin] thickness. This designation is being replaced by thickness in micrometers (µm). (See IPC-4562.)

Copper Thickness The thickness dimension of the copper cladding on a laminate.

Dielectric A material that has a zero or nearly zero electrical conductivity.

Dielectric Constant See definitions of Relative Permittivity, Static Relative Permittivity, and Effective Permittivity.

Dielectric Thickness Thickness dimension of the dielectric of the laminate averaged over an area.

Directional Coupler A device or structure which causes some of the energy propagating along one transmission line to be transferred to a second transmission line so that most of the transferred energy propagates in a specific direction along the second line. The other direction is considered isolated. At lower frequencies this function can be accomplished in a design with lumped capacitive and inductive elements while at microwave frequencies two stripline or microstrip traces that run parallel to each other for a certain distance can serve the purpose. One use for such devices is to sample amplitude or phase of a signal traveling in a specific direction.

Directivity The difference between the isolation and the coupling values of a directional coupler.

Dissipation Factor The ratio of loss current to charging current. The dissipation factor or loss tangent, $\tan\delta$, is given by $\varepsilon''/\varepsilon'$, where ε' and ε'' are the real and imaginary parts of the permittivity (see Permittivity). The loss tangent is a parameter used to express the tendency of insulators or dielectrics to absorb some of the energy in an ac signal.

Distributed Component An electrical component with dimensions greater than or on the order of the wavelength of the propagating signal. The reactive and resistive electrical characteristics of such a component are said to be distributed.

***Effective Permittivity* (effective dielectric constant or $\varepsilon_{r,eff}$)** The permittivity of a mixed media configuration, such as air and the solid dielectrics used in microstrip, that has the equivalent electromagnetic wave propagation characteristics of a single dielectric medium.

Ground Plane An electrically conductive metal layer within a printed wiring board that provides a low inductance ground reference (return path) for signal conductors

on adjacent or buried lines. The ground plane also provides a ground connection for active and passive devices.

Ground-to-Ground-Spacing Distance between ground planes in a stripline circuit.

Ground-to-Signal-Spacing Distance between ground and signal planes or conductors in a transmission line.

Impedance A measure of the opposition to the flow of alternating current in a circuit, equal to the ratio of the rms electromotive force in the circuit to the rms current produced by it. Impedance is usually represented in complex notation as $Z = R + jX$, where R is the ohmic resistance, X is the reactive, either inductive or capacitive, and j is $\sqrt{-1}$.

Insertion Loss The ratio of transmitted electromagnetic power to incident power, usually expressed logarithmically in decibel (dB) units. This loss of power includes losses by conversion to heat in the dielectric and in the conductors.

Loss Tangent See Dissipation Factor.

Lumped Circuit elements that are not distributed.

Metallization A deposited or plated thin metallic film that is used for its protective and/or electrical properties.

Microstrip A transmission line (see Transmission Line) structure that consists of a signal conductor that runs parallel to and is separated from a much wider ground plane.

Microwave Laminate A laminate of metal cladding on dielectric substrate of composition selected to be suitable for circuit boards intended for operation at microwave frequencies.

Microwaves A term generally applied to radio waves in the frequency range of 1 GHz to 100 GHz. It generally refers to the frequency range where circuits and device interconnects are described as distributed elements instead of lumped elements.

Open Circuit A high impedance condition that ideally exhibits 0 dB return loss and a reflection coefficient of 1.0.

Peel Strength The force per unit width that is required to peel a conductor foil from a laminate perpendicular to the surface of the substrate.

Permittivity The square root of the ratio of the electromagnetic wave propagation characteristics of free space to that of the dielectric medium. The permittivity, ε, of a material is, in general, a complex-valued (has real and imaginary parts) parameter. The real and imaginary parts of ε are given by ε' and ε''. See definitions of Relative Permittivity, Static Relative Permittivity, Effective Permittivity.

Plated-Through Holes A hole with plating on its walls that makes an electrical connection between conductive patterns on internal layers, external layers, or both, of a printed circuit board.

PTFE Polytetrafluoroethylene.

Reflection Coefficient The percentage of power (or voltage) reflected from a load that is attached to a circuit or transmission line.

Relative Permittivity (ε_r) The relative permittivity, ε_r, is the ratio of the permittivity of a material to that of free space. The relative permittivity is a complex-valued parameter and is given by: $\varepsilon_r = \varepsilon/\varepsilon_0$, where ε_0 is the permittivity of free space (which is a real value). The real and imaginary parts of ε_r are ε'_r and ε''_r. Herein ε_r denotes the real part of the complex relative permittivity of the dielectric.

Return Loss Level of the reflected signal which is a result of a mismatch between a load and a source. It is usually expressed as the ratio of reflected power to incident power in dB units.

Static Relative Permittivity The ratio of the capacitance (C_x) of a given configuration of electrodes with a specified dielectric, filling all the region of electropotential field, to the capacitance (C_v) of the same electrode configuration with a vacuum (or air) as the dielectric.

S-Parameters Parameters used to describe the operations of a microwave circuit: S11 is the input reflection coefficient, S22 is the output reflection coefficient, S21 is the forward transmission, and S12 is the reverse transmission.

Semi-Rigid Cable A coaxial cable that has a solid outer conductor.

Short Circuit A low impedance that ideally exhibits 0 dB return loss and a reflection coefficient of -1.0.

Skin Depth The depth into a conductor for which e^{-1} of the current associated with a propagating electromagnetic signal is flowing. The depth becomes less as frequency increases and so resistive loss also increases. e is the base for natural logarithms and is approximately 2.7183.

Skin Effect The increase in resistance of a conductor at microwave frequencies that is caused by the tendency of electrical current to concentrate at the conductor's surface (see Skin Depth).

Smith Chart A transmission line calculator used to evaluate and analyze microwave circuitry.

Stripline A transmission line (see Transmission Line) structure that consists of a signal line that runs parallel to and is sandwiched between and separated from two wider ground planes.

Soft Substrate For the purpose of this document the term soft substrate refers to the materials specified in IPC-4103.

***TEM Mode* (Transverse Electromagnetic Mode)** A mode of electromagnetic wave propagation in which, at any point along the line, the electrical and the magnetic

fields both lie in a plane perpendicular to the direction of propagation. This efficient mode is characteristic of free space and is favored by coaxial and stripline transmission lines up to a frequency where other modes, with propagation characteristics different from that of the TEM mode, can exist. The frequency at which these other modes can exist is dependent on frequency and the dimensions of the line perpendicular to the direction of wave propagation.

Transmission Line A device for guiding or conducting electromagnetic energy from one point to another. A transmission line consists of two or more parallel conductors each separated by a dielectric.

VSWR Voltage Standing Wave Ratio, a measure of the degree of mismatch between a load and a transmission line.

Wavelength The distance an electromagnetic wave propagates during one full cycle. It is the ratio of the propagation velocity in length units per unit time to the frequency in cycles per unit time.

2 APPLICABLE DOCUMENTS

The following specifications of the revision in effect at the time of order form a part of this document to the extent specified herein.

2.1 IPC[1]

IPC-T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits

IPC-D-325 Documentation Requirements for Printed Boards

IPC-2221 Generic Standard on Printed Board Design

IPC-2615 Printed Board Dimensions and Tolerances

IPC-4103 Specification for Base Materials for High Speed/High Frequency Applications

IPC-4562 Metal Foil for Printed Wiring Application

IPC-6018 Microwave End Product Board Inspection and Test

IPC-9191 General Guidelines for Implementation of Statistical Process Control (SPC)

J-STD-003 Solderability Test Methods for Printed Circuit Boards

2.2 American Society for Testing and Materials[2]

ASTM B-488-95 Standard Specification for Electrodeposited Coatings of Gold for Engineering Use

2.3 Society of Automotive Engineers[3]

SAE AMS-C-5541 Chemical Conversion Coatings on Aluminum and Aluminum Alloys

SAE AMS-P-81728 Plating, Tin/Lead (Electrodeposited)

2.4 American Society of Mechanical Engineers[4]

ASME-Y-14.100 Engineering Drawing Practices

2.5 International Organization for Standardization[5]

ISO 9001 Quality Management

2.6 Reference Information Software, which is commercially available, can be used when designing microwave boards.

3 DESIGN CONSIDERATIONS

Figure 3-1 shows the major steps in the microwave circuit design process. These steps are explained in the following subsections.

3.1 Initial Input The complete performance characteristics of the product are defined together with the environmental requirements, cost goals, size and weight constraints, and other pertinent information affecting the design. Administrative input comprises completion date, available financial and personnel resources, and expected delivery times for potential materials and components to be used in the design.

3.2 Design Options A literature search is made for similar product designs. These design options are listed with their expected performance specifications, and the most appropriate design is selected as the starting point.

3.3 Transmission Line Type, Materials, and Components The transmission line type (such as microstrip, stripline, suspended substrate, etc.), substrate type, and components are selected. An estimate of the electrical performance is made and compared to the design specification. If the design specification is not met, the design process loops back to select another design option.

1. www.ipc.org
2. www.astm.org
3. www.sae.org
4. www.asme.org
5. www.iso.ch

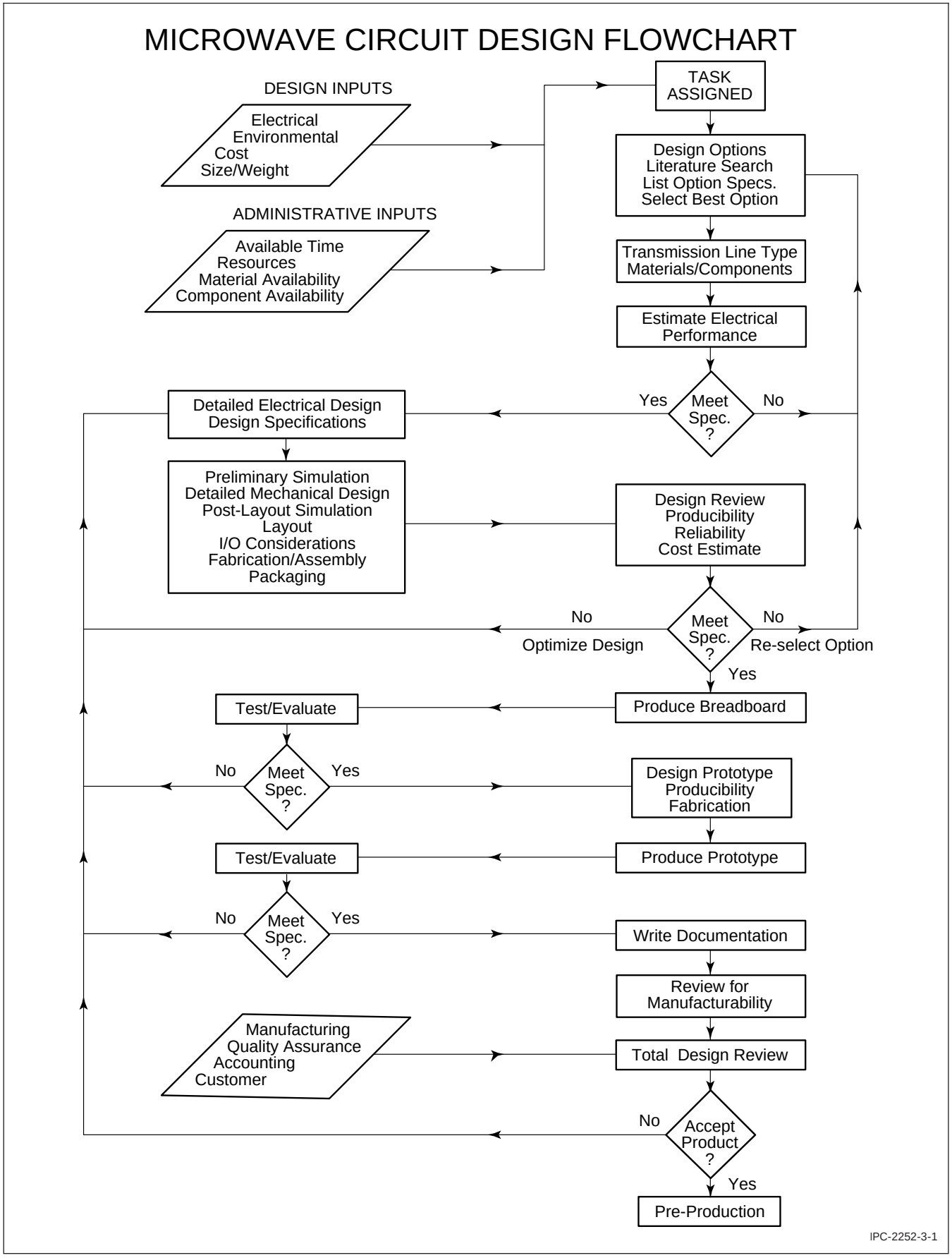

Figure 3-1 Microwave Circuit Design Flowchart

3.4 Electrical Design Detailed electrical design calculations are done to find values for all circuit features and components, and a complete circuit diagram is completed.

3.5 Mechanical Design Electrical values are realized (converted to line dimensions), and a circuit layout constructed. Input/output connection considerations, fabrication, assembly and packaging needs must be considered in designing the layout. A tolerance analysis should be made at this point.

3.6 Preliminary Design Review The preliminary design is reviewed for produceability and reliability, and a preliminary cost estimate made. Electrical performance is re-calculated and these data are compared to the product specification. If the specification is not met, a decision must be made to either select another design option, or to optimize the existing design.

3.7 Breadboard A breadboard simulation of the design is constructed and electrically tested. Output performance is compared to the design specification. If the design specification is not met, the design process loops back to the detailed electrical design.

3.8 Prototype A prototype of the design is made using the exact materials, components, and fabrication processes used for the circuit design. The prototype is fully electrically and mechanically tested under the product environmental specification conditions. Test results are compared to the product specification. If the specification is not met, the design process loops back to the detailed electrical design.

3.9 Documentation The product and manufacturing processes are fully documented, including drawings, purchasing specifications, and Quality Assurance Provisions. The documentation and product control are turned over to manufacturing.

3.10 Final Design Review The design is given a final review with input from internal departments and the customer. If the product is not accepted, control is returned to the design group and the design process loops back to the detailed electrical design. Otherwise, manufacturing retains control and the product goes into pre-production.

4 DOCUMENTATION REQUIREMENTS

4.1 Design Features Listing Circuit boards designed using this Guide should meet or exceed the requirements of IPC-6018, internal company documents, or the contract. Coupon configuration should be per IPC-6018 unless otherwise defined on the master drawing. Test coupons should represent all the printed circuit board manufacturing processes such as drilling, plating, etching, fusing, ground/voltage/thermal/mechanical planes, etc.

Test circuitry, when provided, should be included on the production master and on each panel to be manufactured.

4.2 Master Drawing The master drawing should be prepared in accordance with IPC-D-325, or, in the case of a military contract, ASME-Y-14.100. The master drawing should include all appropriate detail board requirements including, but not restricted to, the following:

a. The type, size and shape of the printed circuit board.

b. The size, location, and tolerance of all holes, slots, and internal routed areas.

c. Thickness of the dielectric separation between layers. In multilayer boards, consider thickness of bonding films.

d. Shape and arrangement of both conductive and nonconductive patterns defined on each layer of the printed circuit board.

e. Separate views of each conductor layer.

f. A modular grid system to identify all holes, test points, lands and overall board dimensions with modular units of length of 2.5 mm [0.100 in], 1.25 mm [0.050 in], 0.625 mm [0.025 in], or other multiples of 0.125 mm [0.005 in] in that order of preference. The grid system should be applied in the X and Y axes of the Cartesian coordinates. The grid system should not be reproduced on the master drawing, but may be indicated using grid scales or X-Y control dimensions.

g. Any and all patterned, drilled, or routed features not controlled by hole sizes and locations should be dimensioned either specifically or by reference to the grid system.

h. Include all notes starting on the first sheet of the master drawing.

i. Conductor layers numbered consecutively starting with the component side or ground side routed through to accommodate component mounting as layer 1.

j. The identification marking and location of traceability marking.

k. The dimensions for critical pattern features that may affect circuit performance because of distributed inductive or capacitive effects within the tolerance required for circuit performance.

l. All terms used on the master drawing should be in conformance with the definitions of IPC-T-50 or IPC-2615.

m. The minimum line width and spacing of the finished printed circuit board.

n. The plating and coating materials and thickness. Particular attention must be paid to defining plated-through holes and plated edges.

o. Applicable fabrication specifications.

p. The relative permittivity (ε_r), tanδ, etc of substrate. (Reference IPC-4103).

q. The type and thickness of copper. (Reference IPC-4103).

r. The type and thickness of bonding films.

4.3 Master Pattern The printed circuit board documentation package usually consists of the master drawing, master pattern drawing, or copies of the artwork masters (film or electronic data). This documentation should meet the requirements of IPC-D-325. Documentation for Military boards should meet the requirements of ASME-Y-14.100. Other documentation, in addition to electronic data for artwork, may include NC tape or electronic data for drilling, routing, testing, and panelization.

When a production master is not supplied, the supplier will be responsible for the preparation of the production master with sufficient accuracy to meet the requirements of the printed circuit detailed on the master drawing. It is recommended that the accuracy of the production master (single image, multiple image and/or any associated test coupons) should be such that the lands, conductors and other features be located within 0.050 mm [0.002 in] diameter of the true grid position established for the layer. In the event that smaller tolerances are required in order to produce critical printed circuits, the production master precision requirements, as considered in the design process, should be defined on the master drawing.

5 MATERIALS

5.1 Microwave Printed Circuit Board Materials Table 5-1 lists typical microwave materials, including the resin system, reinforcement type, typical values of relative permittivity and maximum loss tangent at X-band frequencies (5.20 GHz to 10.90 GHz). A complete listing of the materials and their specifications that are suited for high-speed and high-frequency applications can be found in IPC-4103.

5.1.1 Substrate Selection Since selection of the substrate is made early in the design process it is important to choose the correct substrate to avoid subsequent costly and time-consuming re-design using a different substrate. The major considerations for substrate selection are described in the following subsections.

5.1.1.1 Relative Permittivity The relative permittivity of the substrate must be high enough to permit the manufacture of devices that meet both space and weight limitations. That is, resonant elements must be small enough and any delay lines must be short enough and line widths narrow enough (with the appropriate line-to-line spacing to achieve the required electrical isolation) to fit within the maximum allowable dimensions.

For other applications, such as high-speed interconnects, the relative permittivity must be low enough to allow manufacture of high impedance circuit lines having acceptable line width and characteristic impedance tolerances.

Line widths for a range of board thicknesses, wavelengths for the operating frequencies of the circuit, and estimations of circuit element dimensions should be determined, and a rough layout of the circuit board should be made to determine the maximum and minimum acceptable values of relative permittivity.

The substrate manufacturer's stated tolerance in relative permittivity must be small enough to allow the electrical performance of the circuit to remain within its specified tolerance limits.

5.1.1.2 Loss Tangent Dielectric loss in dB/m for microwave circuit boards is given by:

for stripline designs [1]:

$$\alpha_{d,strip} = 27.3\sqrt{\varepsilon_r}\,\frac{\tan\delta}{\lambda};$$

for microstrip designs [1]:

$$\alpha_{d,micro} = 27.3\,\frac{\varepsilon_r}{\varepsilon_r - 1}\,\frac{\varepsilon_{r,eff} - 1}{\sqrt{\varepsilon_{r,eff}}}\,\frac{\tan\delta}{\lambda};$$

Table 5-1 Typical Microwave Materials

Material Type	Relative Permittivity, ε_r	Loss Tangent, tanδ	IPC-4103 Specification Sheet
Woven Glass Reinforced PTFE	2.40 to 2.60	0.0025	/02
Random Glass Reinforced PTFE	2.15 to 2.35	0.0015	/04
Woven Glass Reinforced PTFE	2.15 to 2.35	0.0015	/05
Ceramic Filled PTFE	3.0, maximum	0.0017 to 0.003 (depending on ε_r)	/06
Ceramic Filled PTFE	5.0 to 7.0	0.003	/07
Ceramic Filled PTFE	8.5 to 11.0	0.0035	/08

where:
ε_r = real part of the relative permittivity of the substrate,
$\varepsilon_{r,eff}$ = real part of the effective relative permittivity (microstrip),
$\tan\delta$ = loss tangent of the substrate, and
λ = free space wavelength.

Thus dielectric losses are a function of both the loss tangent and the relative permittivity. The increased dielectric loss per unit line length for some substrates may be accommodated to some extent by using shorter line lengths in the circuit design. Shorter line lengths also reduce conductor losses, and this may be important at high frequencies where conductor loss becomes significant. A useful circuit parameter for estimating some circuit element losses is loss per wavelength (or frequency) for a given line length rather than the conventional expression of loss per line length for a given frequency.

The loss tangent of the substrate in the design frequency range must be low enough to meet input/output power requirements without thermal management problems. Furthermore, the power response for some circuit elements (such as filters) must have frequency roll-off characteristics sharp enough for the associated circuit to meet the design performance specifications and these roll-off characteristics can be impacted by dielectric losses.

5.1.1.3 Thickness The thickness of the substrate affects the following design considerations:

a. *Line Width* To maintain a given characteristic impedance, decreasing the line width requires decreasing the substrate thickness. High impedance lines on thin substrates may need line widths too narrow for practical fabrication.

b. *Mechanical Strength* Unsupported circuits built on thin soft substrates may bow, warp or distort, and these may not occur when using thermoset materials that are hard and rigid.

c. *Dimensional Stability* Dimensional stability is generally worse for thin substrates than for thick substrates. Fabrication tolerances may also be more difficult or costly to maintain for thin substrates than for thick substrates.

d. *Cost* In general, thicker substrates have a higher cost per unit area than thinner substrates.

e. *Conformability* For circuit boards which will be formed into simple curved shapes (such as cylinders, cones, etc.) thin boards may be bent to smaller radii of curvature than thicker boards without damage to the substrate or copper cladding.

f. *Dielectric Breakdown* Thinner materials generally have higher dielectric breakdown values in proportion to thickness, measured parallel to lamination.

g. *Power Handling Capability* The ability of a high frequency circuit board to handle high power is limited in two ways; these limits are relaxed by increasing the substrate thickness.

1. High power can be partially dissipated as heat generated by resistive loss in the conductors and by absorption loss in the substrate dielectric. The thermal limit for power dissipation in a circuit is affected by the associated temperature rise in the substrate and the acceptable operating temperature limit. Higher powers can be accommodated by using wider signal lines. However, the wider signal line will require a thicker substrate to maintain a given Z_0 for a given material type. The wider lines will also reduce signal attenuation.
2. High peak power levels can result in corona discharge that degrades the substrate with operating time. This is especially true with microstrip or unbonded stripline (stripline made where the top dielectric is held in place on top of the signal line mechanically, such as by clamping) where the voltage gradient may exceed the corona inception voltage of voids within the substrate. Thicker substrates will permit higher peak power before corona inception.

5.1.1.4 Environment Both board fabrication and operational environments place constraints upon the substrate choice. Critical material properties for consideration are:

a. *Temperature Resistance* Operational and processing maximum and minimum temperatures must be established. Furthermore, temperature extremes should be characterized as ''peak'' or ''continuous.'' Changes in electrical properties with temperature for the temperature extremes should be calculated and performance compared to the design specification. The board may not be required to function during ''intermittent'' temperature extreme periods so that only the ''continuous'' temperatures should be used to estimate performance. However the mechanical properties of the board should be examined for permanent damage at ''intermittent'' extreme temperatures.

b. *Moisture and Chemical Resistance* Moisture absorption of the substrate must be low enough so that electrical performance is not significantly degraded in high humidity environments. Added fabrication costs and design compromises may be incurred if additional environmental protection is needed. Proposed processing environments must be compatible with the chemical and solvent resistance of the substrate. Significant processing costs may be incurred if extraordinary measures must be taken to accommodate poor solvent and chemical resistance.

c. *Radiation Resistance* For space or nuclear environments, the board substrate may experience high doses of ionizing radiation. The effects of ionizing radiation on the mechanical and electrical properties should be determined and the performance estimated. Also the effects of cumulative radiation doses should be estimated and the effective service life of the board compared to the design specification.

d. *Other Substrate Properties* Although detailed analysis of all relevant material properties is not recommended during the initial substrate selection, the designer should be aware of other properties that may have electrical and mechanical performance, and fabrication considerations.

1. The copper bond strength must be high enough to withstand both the service and board processing environments without permanent damage.
2. The temperature dependence of the relative permittivity may affect electrical performance over the operational temperature range.
3. The coefficient of thermal expansion should be considered when designing for extreme environmental temperature ranges and high power devices, and when solder reflow processes or other high temperature processes are used during fabrication.
4. Surface mounted device and plated-through hole reliability questions are affected by thermal expansion.
5. The thermal conductivity of the substrate will affect design of the board where thermal management problems need consideration.
6. Deformation under load should be evaluated when considering board mounting and housing options.
7. The electrical resistivity may be a factor in electrical performance, particularly if high impedance lines carry high voltages in power amplifier circuits, for example.
8. Mechanical properties (tensile, compressive, and flexural strengths and moduli) considerations may affect mounting and housing decisions.
9. The specific gravity of the substrate will determine the weight of the circuit board.

5.1.1.5 Cost Direct cost goals set by the design specification should include not only the substrate costs but also the estimated fabrication costs. Estimates should be made for prototype, pre-production and production phases for appropriate quantities of circuits, and of the total program direct costs.

5.1.1.6 Supplier If possible, the substrate type selected should be available from more than one supplier. However, although different suppliers' substrates may be made from the same resins and reinforcements or fillers and may meet the same product specifications, subtle differences in substrate manufacturing methods will yield circuits with different performance and processing characteristics. Consequently, if development time and budgets permit, comparative material studies should be made. Selection of the primary and secondary suppliers should be based upon material cost, estimated reliability of supply over the program period, and degree of technical support for quality problems and design assistance.

5.2 Bonding Films Bonded assemblies may be made with either thermoplastic or thermoset bonding films, or by direct bonding. The properties of the bonding layer will affect the electrical performance of the assembly. This should be taken into consideration when planning a bonded assembly. The use of bonding films with low dielectric constant substrates is common because the dielectric constant of the bonding film and the substrate material are closely matched. When ceramic filled or high dielectric constant substrates are used, however, the mismatch of dielectric constants of the film and the substrate makes the circuit much harder to design and model. For high dielectric constant substrates, direct bonding should be considered.

5.2.1 Thermoplastic Bonding Films Thermoplastics are made up of a polymer that will change from the solid to liquid phase at elevated temperatures and return to a solid when cooled. If the polymer is again taken to elevated temperatures, it will again change to its liquid phase. Table 5-2 lists the typical characteristics of the common thermoplastic bonding films:

LDPE is low density polyethylene
IPO is Irradiated Polyolefin co-polymer
CFP is chlorofluoro-copolymers
FEP is poly(tetrafluoroethylene-co-hexafluoropropylene)
PFA is poly(tetrafluoroethylene-co-perfluoroalkoxy)

5.2.2 Thermoset Bonding Films Thermosets are cured by a chemical change induced by elevated temperatures. This chemical change is not reversible; that is, once the bonding film is cured, further high temperature exposure will not remelt the film. Table 5-3 lists the characteristics of the common thermoset bonding films:

5.2.3 PTFE Bonding Considerations Most bonding films will require that the surface of the PTFE laminate be treated for wettability. This is done with either a plasma etch or a sodium etch, however, a bondable PTFE surface may be achieved after etching off the copper cladding and taking care that the surface is undisturbed prior to bonding. When selecting a bonding system, the following should be considered:

a. The heat sensitivity of solder joints or mounted components.

Table 5-2 Typical Characteristics of Thermoplastic Bonding Films

Film Type	LDPE	IPO	CFP	FEP	PFA
Melting point (°C)	90	121	181	260	305
Permittivity @10 GHz	2.30	2.30	2.35	2.10	2.10
Loss Tangent	0.0005	0.0020	0.0025	0.0003	0.0010
Bond temperature (°C)	120	121 to 149	220	280	320

Table 5-3 Characteristics of Thermoset Bonding Films

Resin Type	Epoxy System	Acrylic System
Cure temp (°C)	165 to 180	177 to 191
Permittivity	3.76 (1 MHz)	4.00 (1 MHz)
Loss tangent	0.064 (1 MHz)	0.027 (1 MHz)

b. The availability of plasma etching equipment, or willingness and facilities to use a sodium etching system.

c. The temperature available in the press or autoclave of suitable design.

d. The temperature to be encountered by the device in service.

e. The tolerance for dielectric losses and for dielectric constant match of the bond layer to the laminate.

When designing a multilayer board to use metal-clad PTFE laminates, it is recommended that the board be designed so that interlayer bonding is accomplished primarily by contacting the large metal areas left on the clad PTFE laminate after etching, which are typically used for power and ground planes. If this is not possible, then surface treatment may be necessary, as described above.

5.3 Metals

5.3.1 Cladding Microwave printed circuit board materials are available with a variety of metal claddings.

5.3.1.1 Thin Cladding Considerations The most common thin copper foils, less than 100 µm [<0.004 in] thick (<3 oz) are listed in Table 5-4. Typical microwave applications use Type 1 and Type 5. On thin copper, a treatment is added to roughen the surface of the copper to enhance adhesion to the substrate. The surface roughness of claddings contributes to microwave circuit losses and this effect is greater at higher frequencies.

5.3.1.2 Heavy Cladding Considerations Thick metal claddings, 100 µm [0.004 in] thick (3 oz) or greater, can be laminated to microwave substrates. For thick metal claddings, the metal surface is mechanically roughened to obtain sufficient bond strength. Table 5-5 lists the more common types of metals used. Other metals may be available.

5.3.2 Metal Plating The requirements for printed circuit boards often includes some type of plating, whether it be for improved conductivity, oxidation protection, improved solderability, or providing a path to ground. Many types of metals and chemistries have been tried, and the platings listed in this section continue to find use within the industry. Different types of plated metals will have different conductivities and the conductivity of a given type of plating may also vary. This variation in conductivity may be caused by morphology, impurity concentrations, and/or alloy composition. Furthermore, the resistance of a plated conductor may be affected by metal thickness, surface topology, interfacial effects, and/or conductor cross section. The effect of conductor resistance on losses in transmission lines is discussed in 6.1.2 for striplines and 6.3.2 for microstrip.

Table 5-4 Most Common Thin Copper Foils, less than 100 µm (<0.004 in, <3 oz)

1.	Standard electrodeposited (STD-Type E)
2.	High ductility electrodeposited (HD-Type E)
3.	High temperature elongation electrodeposited (HTE-Type E)
4.	Annealed electrodeposited (ANN-Type E)
5.	As rolled-wrought (AR Type W)
6.	Light cold rolled-wrought (LCR-Type W)
7.	Annealed Wrought (ANN-Type W)
8.	As rolled-wrought low-temperature annealable (LTA-Type W)

Table 5-5 Thick Metal Claddings

Aluminum (Alloy 6061, 5083)
Brass (70/30 Cartridge)
Copper (Alloy 110)
Stainless Steel
Copper Invar Copper
Copper Molybdenum Copper

5.3.2.1 Preparing Holes and Edges for Plating Either an electroless copper or a conductive coating is used when plating is required in the holes of vias or on the edges of a substrate. A very thin layer of copper or conductive coating is deposited on the dielectric and this coating provides an electrical path for the subsequent electrodeposition of additional copper. This coating is one of the electrodes necessary in the electrodeposition process and is the one on which copper is plated.

5.3.2.2 Electrodeposited Copper Copper is normally electrodeposited after an electroless metal deposition or application of one of the alternatives to electroless copper

in the plated through holes (see 5.3.2.1). Normal plating thickness is 0.025 mm [0.001 in.] minimum but for substrate materials with high z-axis thermal expansion, a thickness of 0.038 mm [0.0015 in] provides a more durable coating.

Acid copper is a copper sulfate and sulfuric acid bath that contains additives which produce a bright finish. This type of bath is cost effective, easy to work with, and can withstand higher current densities than other copper baths.

Pyrophosphate copper is a copper bath that provides the high plating rates required for plating through holes. However, it is not a process that is widely available.

5.3.2.3 Nickel Nickel may be applied by electrodeposition or electroless deposition. Electrodeposited nickel is used primarily as a base plate for gold. Nickel acts as a barrier to prevent gold migration into the copper at high temperatures. It also acts as a hard base for applications where pressure is applied to the gold plate, such as wire bonding or connector contacts. Nickel has higher electrical resistance than copper and is ferromagnetic which can cause undesirable performance in microwave circuits. Electroless nickel is used primarily on aluminum as the base plate prior to subsequent plating operations such as gold, silver, tin, or tin lead.

Typical plating thicknesses are as follows: Electrodeposited nickel: 1.3 µm to 5.0 µm [0.00005 in to 0.0002 in], Electroless nickel: 5.0 µm to 7.5 µm [0.0002 in to 0.0003 in].

5.3.2.4 Gold Gold is used primarily because of its corrosion resistance and its low electrical resistance. It is easily soldered, is ductile, and has relatively good electrical characteristics. Gold also has the highest values of infrared emissivity and reflectivity which makes it excellent for use in space applications. Typically gold plating for microwave applications is type III gold (soft) per ASTM B-488-95. Plating thicknesses with a nickel barrier range from 0.25 µm to 0.8 µm [0.00001 in to 0.00003 in] for applications requiring soldering and 3.8 µm to 7.5 µm [0.00015 in to 0.0003 in] for applications requiring bonding.

When plated directly over copper, the thinner deposits (0.9 µm to 3.8 µm [0.000035 in to 0.00015 in]) may exhibit copper migration over a period of time resulting in a deterioration of solderability. In those cases an underplate of nickel will aid in maintaining solderability. Refer to ASTM B-488-95 for further characteristics and requirements.

5.3.2.5 Silver Silver has the highest conductivity and the lowest contact resistance, but tarnishes easily. Also, silver may migrate through or across the circuit board substrate when placed under a positive dc voltage. Typically, silver is plated over nickel and occasionally will be overplated with rhodium.

5.3.2.6 Tin-lead Tin-lead plating is commonly used for solderability and oxidation protection of the copper cladding. The optimum plating thickness is 7.5 µm to 17.5 µm [0.0003 in to 0.0007 in] with the optimum tin-lead composition being 63 % tin and 37 % lead. Tin-lead plating is often left in the as-plated condition. Reflow of the tin-lead may cause the plating to be thicker in the center than at the edges and designs with unbalanced circuitry (e.g., fine line circuitry one side; ground plane the opposite side) may bow or twist. Refer to SAE AMS-P-81728 for further characteristics and requirements for tin-lead.

5.3.2.7 Solder Coating Solder coating is used to increase the solderability and oxidation protection of the copper cladding. It is usually either a fused tin-lead electroplated or soldered surface.

5.3.2.8 Immersion Tin Immersion tin is deposited onto copper using an electroless process. The minimum thickness of an immersion tin plating is normally 0.64 µm to 1.3 µm [0.000025 in to 0.00005 in]. Immersion plating thickness is self-limiting and ceases when the copper is completely covered by the tin.

5.3.2.9 Electroplated Tin Electroplated tin is used as an oxidation protection layer for the copper. To improve solderability, matte tin plate is preferred. Bright acid tin electrodeposits may form dendrites that can bridge closely spaced conductors. This plating should use bismuth additives to minimize dendrite formation or equivalent.

5.3.3 Galvanic Corrosion It is important to remember that contact between dissimilar metals may cause galvanic action to occur. A general rule of thumb is to avoid a voltage difference of greater than 0.25 V between dissimilar metals in contact. (See table below.)

Metal	EMF Voltage
Gold	+0.15
Platinum	+0.15
Rhodium plated on silver	+0.05
Silver	0.00
Nickel	–0.15
Monel metal	–0.15
High Nickel Copper alloys	–0.15
Titanium	–0.15
Copper	–0.20
Bronze, low	–0.20
Nickel-Chromium alloys	–0.20
Brass, low	–0.20
Copper-Nickel alloys	–0.20
Brass, yellow commercial	–0.25
Bronze, commercial	–0.25
Brass, high	–0.30
Bronze, high	–0.30

Brass, naval	–0.30
Brass, Muntz	–0.30
Steels, 18 % chromium type corrosion resistant	–0.35
Chromium	–0.45
Steels, chromium type corrosion resistant	–0.45
Tin plate	–0.50
Tin-lead solder	–0.50
Lead	–0.55
High lead alloys	–0.55
Aluminum 2000 series	–0.60
Iron, wrought	–0.70
Steel, plain carbon	–0.70
Aluminum, other than 2000 series	–0.75
Aluminum, cast alloys silicon type	–0.75
Aluminum, cast alloys other than silicon type	–0.80
Aluminum, chromated	–0.80
Cadmium	–0.80
Steel, galvanized (hot dip zinc plate)	–1.05
Zinc	–1.10
Magnesium	–1.60

5.3.4 Chromate Conversion Coating Chromate conversion coatings are available to protect aluminum surfaces from oxidation. These coatings are most commonly used when the circuit has a thick aluminum ground plane or chassis that is used as a ground return. Electrically conductive chromate conversions are available which aid in maintaining electrical connection between the ground plane and chassis. Refer to SAE AMS-C-5541 for further characteristics and requirements.

5.4 Conformal Coating

5.4.1 General Caution Conformal coatings are not recommended for microwave designs because they degrade the electrical performance of the circuit by changing the effective permittivity of the dielectric (relative permittivity of the coating is greater than 1) and by increasing dielectric losses. Conformal coatings on circuits are intended for protection against adverse environmental conditions during operation.

For circuit substrates that are not PTFE based, a conformal coating is often needed to protect the substrate, particularly in high humidity environments. If the exposure to high humidity is continuous for long periods of time, then a conformal coating only slows the rate of moisture absorption but does not reduce the final amount of moisture absorbed. In low humidity environments, conformal coatings slow the loss of moisture from the substrate.

5.4.2 PTFE Considerations For PTFE based substrates, environmental protection for the dielectric is rarely used because of its low moisture absorption characteristics. Conductors should be plated rather than conformally coated for environmental protection. Only when mounted components need protection should conformal coating be considered. For PTFE based substrates that are to be conformally coated, and where the adhesion to the dielectric surface is inadequate, one of the following procedures may be adopted:

a. A perimeter of copper (which may be plated) is left on the circuit. The conformal coating will adhere well to the perimeter copper.

b. If the circuit board is to be mounted in a housing, it may be possible to coat the board after mounting to include the mounting perimeter.

[1] K.C. Gupta, R. Garg, and R. Chadha, ‘‘Computer-aided Design of Microwave Circuits,’’ Artech House, Dedhman, MA, USA, 1981.

6 ELECTRICAL CHARACTERISTICS

The important electrical characteristics for high frequency circuit designs are the characteristic impedance (Z_0), the attenuation factor (α), and the signal propagation speed (v). The Z_0 and v are affected by the effective relative permittivity ($\varepsilon_{r,eff}$) whereas signal losses are affected by α.

Among the possible types of transmission structures, stripline, microstrip, coplanar waveguide, slot line, etc., the stripline and microstrip structures are most commonly used in printed wiring board circuit design and are used typically with soft substrates. For either stripline or microstrip, Z_0 and α are strongly affected by the ratio of ground plane spacing to conductor width, the conductor thickness, and the space between coupled conductors. The α, $\varepsilon_{r,eff}$ and Z_0 may exhibit frequency dependent behavior depending on the frequency range and transmission line design.

When cross-sectional dimensions of microstrip or stripline are large relative to the wavelength in the media (which occurs at high frequencies), other (higher) modes of propagation become important and these modes usually adversely affect the electrical performance of the transmission line. To avoid higher order modes as the signal speed and frequencies increase, the transmission line geometries must be reduced in scale. Reduction of the transmission line geometries requires the use of thinner substrates to maintain a given Z_0.

Parameters that will be used in this section to calculate Z_0, α_c, $\varepsilon_{r,eff}$ of the transmission line and that are common to the different transmission line structures discussed in this section are given below.

c	speed of light, 2.99792×10^8 m/s
f	frequency (Hz)
t	copper thickness (m)
w	width of signal line (m)
R_s	surface resistivity of copper conductor (ohms/square)
Z_0	characteristic impedance (ohms)
e	2.71; natural constant of growth or decay

ln natural logarithm (base *e*)
tanδ dissipation factor (loss tangent) of substrate
α attenuation factor of transmission line (dB/m). $\alpha = \alpha_d + \alpha_c + \alpha_r$, which are the dielectric, conductor, and radiative losses.
α_d attenuation due to dielectric losses (dB/m)
α_c attenuation due to conductor losses (dB/m)
α_r attenuation due to radiative losses (dB/m)
ε_r relative permittivity
η_0 impedance of free space, 376.73 ohms
ϕ surface roughness of the conductor at interface with substrate (m)
8.68589 conversion from Neper to dB units = 20/ln (10)

6.1 Stripline Stripline is defined in 1.3. A sectional view of a typical stripline transmission line is shown in Figure 6-1 and a cutaway view is shown in Figure 6-2. For stripline transmission lines, the values for Z_0 and attenuation are usually computed using either one of two sets of equations, one set is for narrow lines and one is for wide lines. These equations will be presented later in this section.

Description of symbols used for stripline calculations (in addition to those mentioned above):

b ground plane spacing (m), see Figure 6-1.

Formulas are now presented for calculating Z_0 and α_c. The formulas should be chosen based on the ratio of the signal line width (w) to the difference between the dielectric and conductor thickness (b-t).

6.1.1 Characteristic Impedance of Stripline

6.1.1.1 Narrow Signal Lines Narrow signal lines occur when $\frac{w}{b-t} \leq 0.35$. For narrow signal lines, Z_0 is calculated using [1, equation 3; or 3, equation 3]:

$$Z_0 = \frac{60}{\sqrt{\varepsilon_r}} ln\left(\frac{4b}{\pi w Y}\right)$$

where

$$Y = \frac{1}{2}\left[1 + \left(\frac{X}{\pi}\right)\right]\left[1 + \ell n\left(\frac{4\pi}{X}\right) + 0.51\pi X^2\right]$$

and $X = \frac{t}{w}$. The function for Y is taken from J. F. White, Semiconductor Control, Artech House, 1977, pp. 521-522 rather than the chart provided by Cohn.

6.1.1.2 Wide Signal Lines Wide signal lines occur when $\frac{w}{b-t} > 0.35$.

For wide signal lines, the characteristic impedance of a stripline is [1, equation 4]:

$$Z_0 = \frac{94.15}{\sqrt{\varepsilon_r\left(C_f + \frac{w}{b-t}\right)}},$$

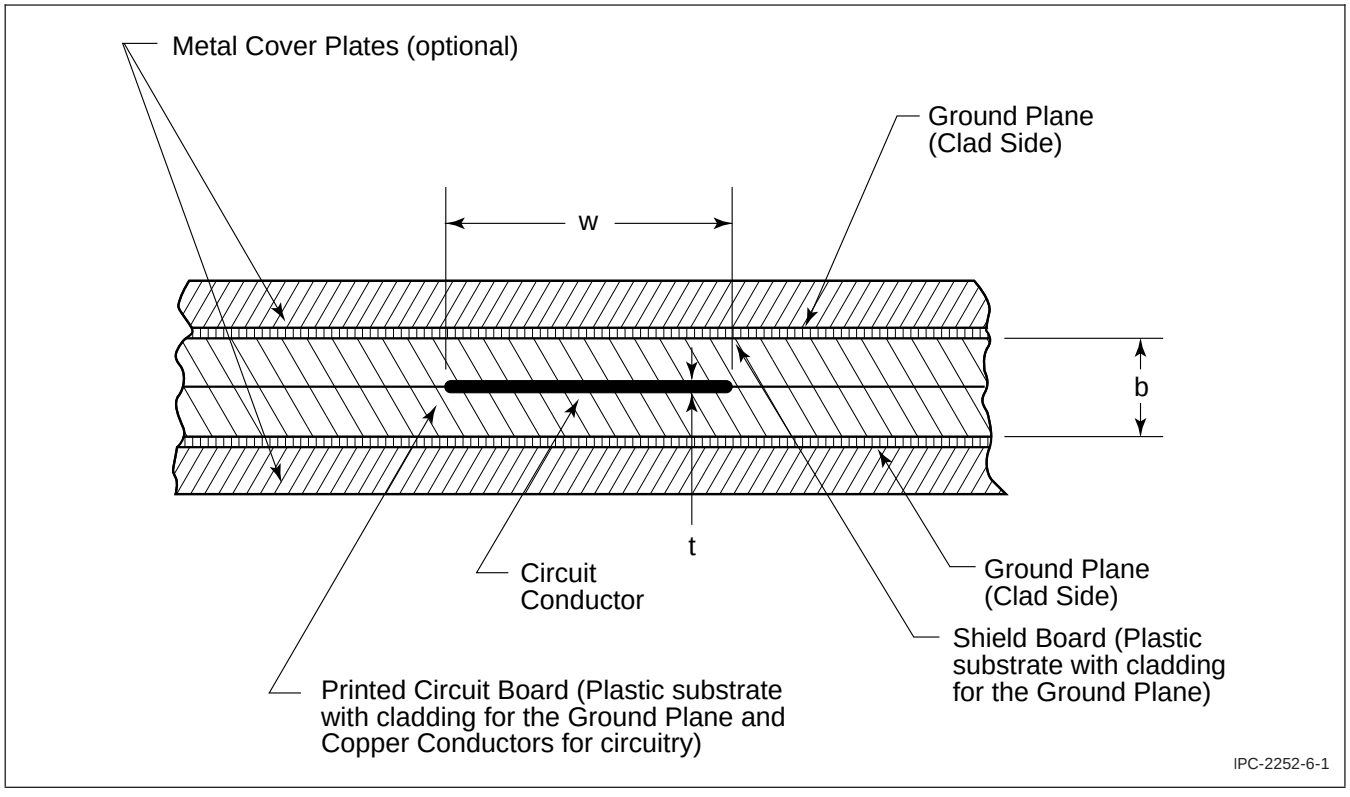

Figure 6-1 Stripline

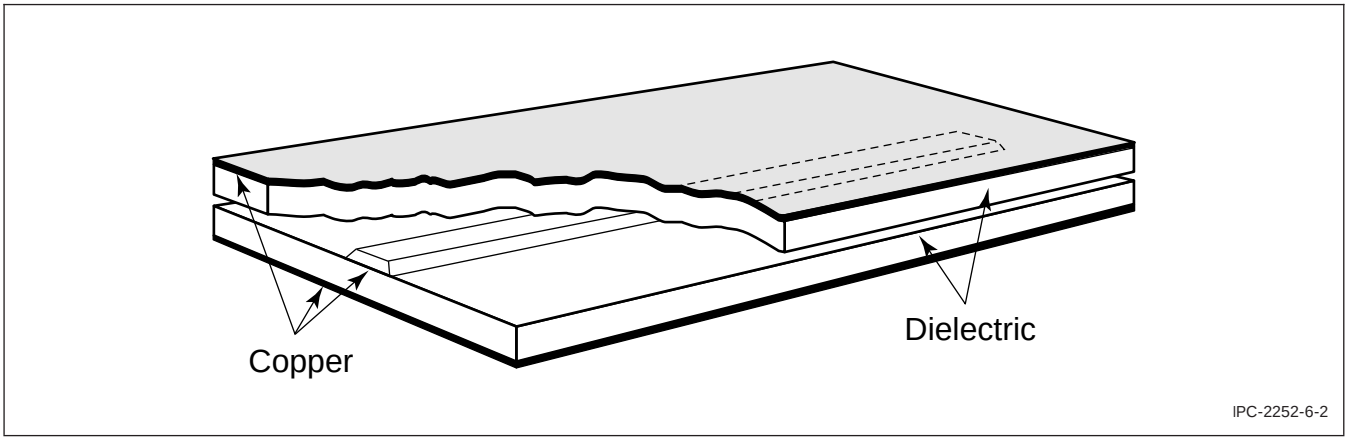

Figure 6-2 Cutaway View of Stripline

where C_f is a term reflecting the effect of fringing capacitance and is given by [1, equation 5]:

$$C_f = \frac{[2\chi \ell n(\chi+1)-(\chi-1)\ell n(\chi^2-1)]}{\pi},$$

$$\text{and } \chi = \frac{b}{(b-t)}.$$

6.1.2 Attenuation in Stripline Attenuation in the transmission line is given by:

$$\alpha = \alpha_c + \alpha_d.$$

The α_r is zero for a uniform continuous transmission line, which is the case considered here, and will not be considered further. The dielectric contribution, α_d, to the attenuation is not affected by signal line width. The attenuation, in dB/m, due to dielectric losses is given by [1, equation 7]:

$$\alpha_d = 8.68589\pi\frac{f}{c}\sqrt{\varepsilon_r}\tan\delta.$$

The conductor losses are dependent on the penetration of the electrical current into the conductors. For smooth conductors the surface resistivity in ohms/square is given by:

$$R_s = \sqrt{\frac{\pi f \mu}{\sigma}}.$$

The conductor surface resistivity in ohms/square, corrected for surface roughness is [2]:

$$R_s(\phi) = R_s\left(1 + \frac{2}{\pi}\tan^{-1}\left[1.4\,\frac{\phi^2}{\delta^2}\right]\right),$$

where δ is the skin depth (frequency dependent penetration of the current into the conductor), and is given by:

$$\delta = \frac{1}{\sqrt{\pi f \mu \sigma}},$$

where μ is the magnetic permeability of the conductor and σ is the electrical conductivity of the conductor. The permeability of metals commonly used as conductors, such as gold, silver, aluminum, and copper, is approximately the same as that of free space ($4\pi\ 10^{-7}$ H/m). Ferromagnetic metals, such as cobalt, nickel, iron, and their alloys, have permeabilities much greater than that of free space.

6.1.2.1 Narrow signal lines The attenuation, in dB/m, due to conductor losses is given by [1, using equations 19 and 22]:

$$\alpha_c = 8.68589\left[\frac{R_s(\phi)}{(2\pi\ Z_0\ b)}\right]$$

$$\left[1 + \left\{\frac{b}{Y\ w}\right\}\left\{0.5 + 0.669X - 0.255X^2 + \left(\frac{1}{(2\pi)}\right)\ell n\left(\frac{4\pi}{X}\right)\right\}\right].$$

The accuracy of this equation is questionable when t/w or w/t exceeds 0.11[1]

6.1.2.2 Wide signal lines The attenuation, in dB/m, due to conductor losses for wide signal lines is, after correcting apparent errors in [3, equation 17]:

$$\alpha_c = 8.68589\ \frac{4\ R_s\ (\phi)\varepsilon_r\ Z_0\ \Psi}{(\eta_0\ ^2 b)}$$

where Ψ is:

$$\Psi = X + \frac{2w\ X^2}{b} + \left(1 + \frac{t}{b}\right)\left(\frac{X^2}{\pi}\right)\ell n\left(\frac{X+1}{X-1}\right)$$

6.2 Asymmetric Stripline In the case where a signal line is placed between two ground (or power) planes, but is not centered between them, the stripline equations must be modified. The modification is necessary to account for the difference in coupling of the signal line between the nearer and farther ground planes. When the signal line is placed within the middle third of the interplane distance, the error caused by assuming it to be centered will be small.

Where a high degree of controlled coupling between signal lines is desired, an asymmetric stripline structure may be

used that consists of two signal lines, each on a separate plane and separated by a dielectric, located between the ground planes. Coupling between the signal lines is accomplished by running the signal lines parallel to each other or by having them overlap. It is poor practice in high frequency circuit design to use such a structure for orthogonal crossovers of signal lines where coupling is not desired.

6.3 Microstrip Microstrip transmission lines are defined in 1.3. Figures 6-3 and 6-4 illustrate microstrip transmission lines.

Description of symbols for microstrip calculations:

h	substrate thickness (m)
P(f)	filling factor
Q_c	inductive quality factor
Q_d	capacitive quality factor
Q_0	quality factor of transmission line
T	ratio of conductor thickness, t, to substrate thickness, h
u	ratio of signal line width to substrate thickness, u = w/h
$Z_0(f)$	characteristic impedance at frequency f
q	mixed dielectric filling factor
ε_r	real part of the relative permittivity
$\varepsilon_{r,eff}$	real part of the effective relative permittivity
$\varepsilon_{r,eff}(f)$	effective relative permittivity at frequency f

6.3.1 Characteristic Impedance and Effective Permittivity of Microstrip The equations for the characteristic impedance and effective relative permittivity for a microstrip transmission line, such as that shown in Figure 6-3, are presented here. The Z_0 of a microstrip line is based on a simple microstrip model, a model where the microstrip consists of only one dielectric and the conductors have zero thickness. This impedance, $Z_{0,0,1}$ is given by [2, equation 1]:

$$Z_{0,0,1}(u) = \frac{\eta_0}{2\pi} ln\left[\frac{6+(2\pi-6)exp\left[-\left(\frac{30.666}{u}\right)^{0.7528}\right]}{u} + \sqrt{1+\frac{4}{u^2}}\right],$$

where u = w/h and the second "0" and "1" subscript denote zero conductor thickness and one dielectric. According to [2], the accuracy of this model is better than 0.01 % for u ≤1 and better than 0.03 % for u ≤ 1000. However, this microstrip model assumed a zero thickness conductor, which is not correct, and one dielectric, which is not typically the case. To correct for the finite thickness of the conductors, the value of u is corrected and this corrected value of u is then used to calculate the characteristic impedance of the transmission line. For a homogenous dielectric, the corrected u, u_1, is [2, equation 6]:

$$u_1 = u + \frac{T}{\pi} ln\left[1 + \frac{4e}{T}\tanh^2\left(\sqrt{6.517u}\right)\right]$$

where u = w/h. For a mixed dielectric medium, the corrected u, u_r, is [2, equation 7]:

$$u_r = u + \frac{(u_1 - u)}{2}\left[1 + \frac{1}{\cosh\left(\sqrt{\varepsilon_r - 1}\right)}\right].$$

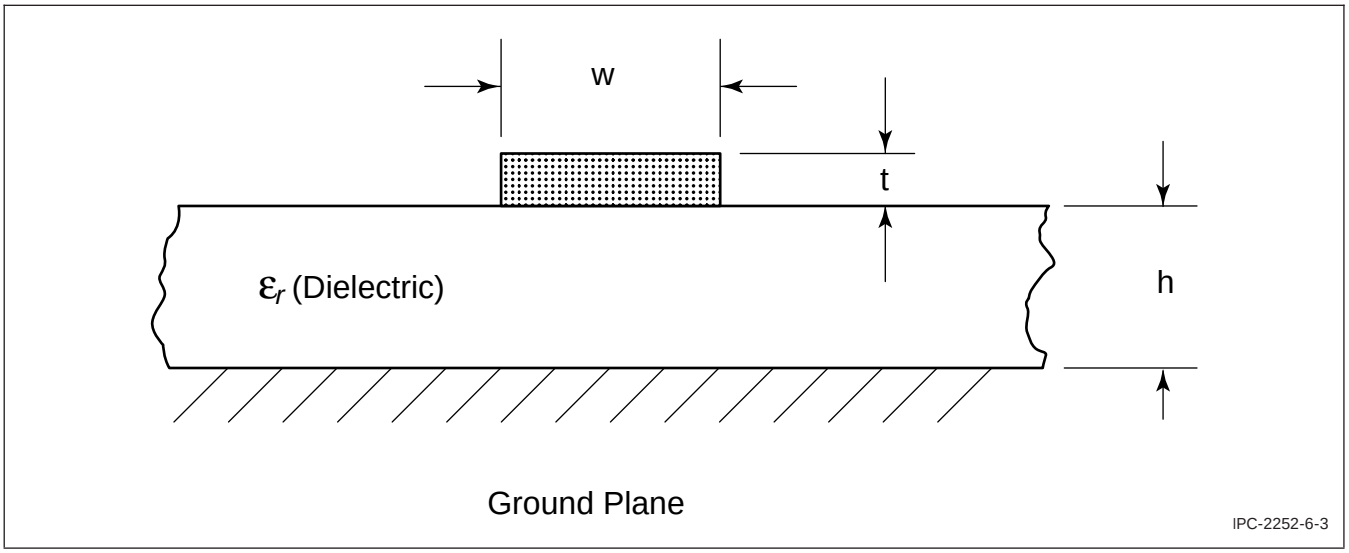

Figure 6-3 Cross Sectional View of Microstrip Line without Metal Cover

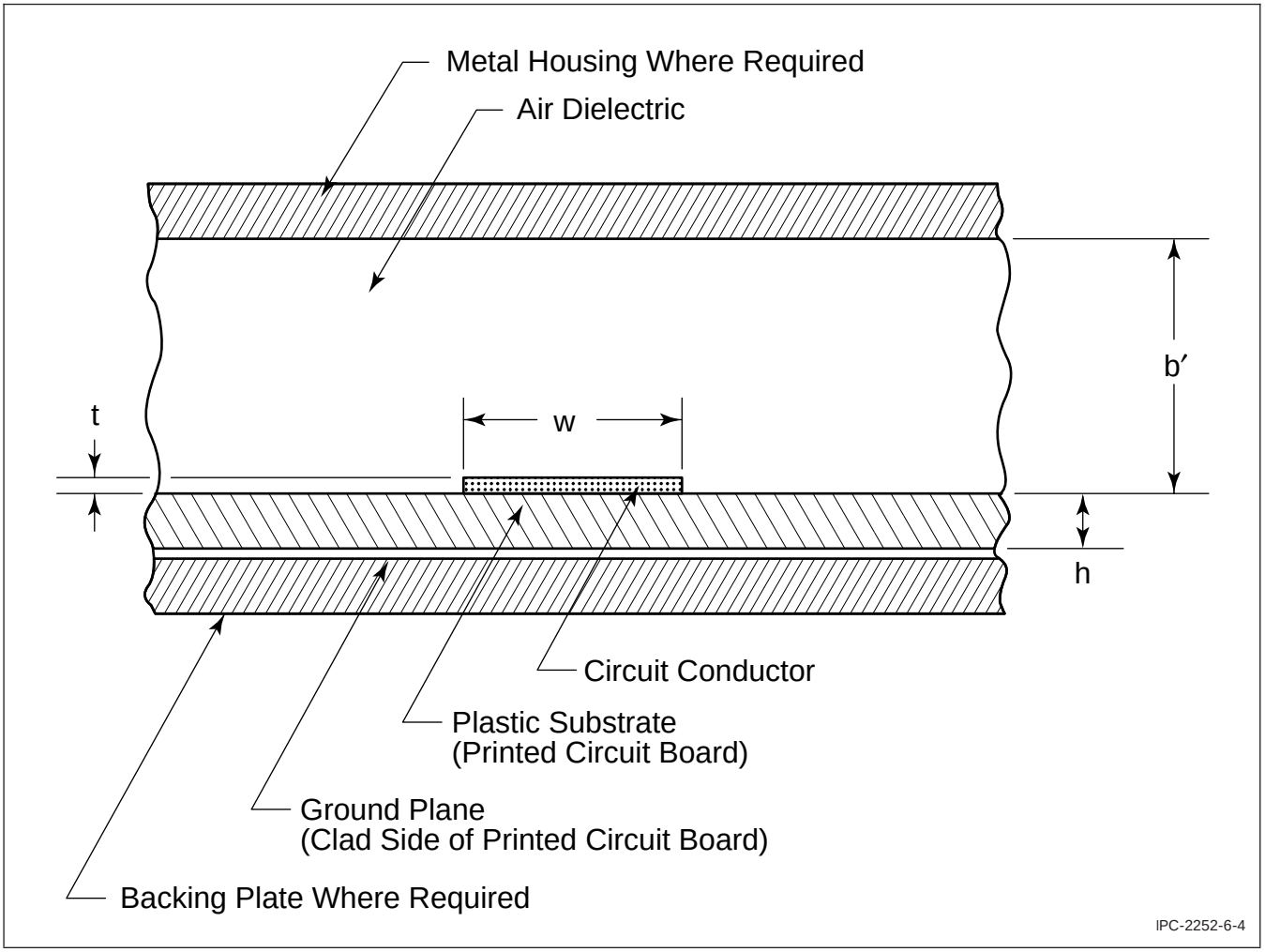

Figure 6-4 Cross-Sectional View of Microstrip Line with Metal Cover

For most practical printed wiring board applications, mixed dielectrics are used where one dielectric is air and the other is the substrate.

Before computing the characteristic impedance for a microstrip transmission line with finite thickness conductors and mixed dielectrics, the effective permittivity, $\varepsilon_{r,eff}$, must be calculated. To calculate $\varepsilon_{,r,eff}$, two auxiliary equations are required. The first auxiliary equation is [2, equation 4]:

$$a_u = 1 + \frac{1}{49} ln\left(\frac{u_r^4 + \frac{u_r^2}{2704}}{u_r^4 + 0.432}\right) + \frac{1}{18.7} ln\left[1 + \left(\frac{u_r}{18.1}\right)^3\right].$$

The second auxiliary equation is [2, equation 5]:

$$b_\varepsilon = 0.564\left(\frac{\varepsilon_r - 0.9}{\varepsilon_r + 3}\right)^{0.053}.$$

The static (frequency = 0 Hz, or dc) effective relative permittivity can be calculated using [2, equation 3]:

$$\varepsilon_{r,eff,dc}\,(u,\varepsilon_r) = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left(1 + \frac{10}{u_r}\right)^{-a_u b_\varepsilon}.$$

The accuracy of this model for the static effective relative permittivity is claimed [2] to be better than 0.2 % for $\varepsilon_r \leq 128$ and $0.01 \leq u \leq 100$. The characteristic impedance, corrected for mixed dielectric media and finite conductor thickness is [2, equation 8]:

$$Z_0(u,T,\varepsilon_r) = Z_{0,0,1}(u)\,\frac{1}{\sqrt{\varepsilon_{r,eff,dc}(u,\varepsilon_r)}},$$

and the static effective relative permittivity as a function of conductor thickness becomes [2, equation 9]:

$$\varepsilon_{r,eff,dc}(u,t,\varepsilon_r) = \varepsilon_{r,eff,dc}(u_r,\varepsilon_r)\left(\frac{Z_{0,0,1}(u_1)}{Z_{0,0,1}(u_r)}\right)^2.$$

The equations thus far do not consider frequency effects. To compute the frequency dependent effective relative permittivity and characteristic impedance of a microstrip transmission line, an additional equation is required. This equation is [4, equation 2]:

$$P(f) = P_1P_2\left[10^{-6}\ fh\left(0.1844 + P_3P_4\right)\right]^{1.5763}, \text{ and}$$

$$P_1 = 0.27488 + \left[0.6315 + 0.525\left(1.57 \times 10^{-9}\ fh + 1\right)^{-20}\right]u - 0.065683\ exp\left(-8.7513u\right)$$

$$P_2 = 0.33622\left[1 - exp\left(0.03442\varepsilon_r\right)\right]$$

$$P_3 = 0.0363\ exp\ (-4.6u)\left\{1 - exp\left[-\left(\frac{10^{-8}\ fh}{3.87}\right)^{4.97}\right]\right\}$$

$$P_4 = 1 + 2.751\left\{1 - exp\left[-\left(\frac{\varepsilon_r}{15.916}\right)^{8}\right]\right\}.$$

Using P(f), the frequency-dependent relative effective permittivity is [4, equation 1]:

$$\varepsilon_{r,eff}(f) = \varepsilon_r - \left(\frac{\varepsilon_r - \varepsilon_{r,eff,dc}}{1 + P(f)}\right).$$

The frequency-dependent characteristic impedance then becomes [2, equation 12]:

$$Z_0(f) = \frac{Z_{0,0,1}(u_r)}{\varepsilon_{r,eff,dc}(u_r,\varepsilon_r)}\sqrt{\frac{\varepsilon_{r,eff,dc}}{\varepsilon_{r,eff}(f)}}\ \frac{(\varepsilon_{r,eff}(f) - 1)}{(\varepsilon_{r,eff,dc} - 1)}$$

6.3.2 Attenuation in Microstrip The attenuation, in dB/m, due to dielectric and conductor losses in the microstrip line is [2, equation 38]:

$$\alpha = 8.68589\pi\ \frac{f\sqrt{e_{r,eff}(f)}}{c\ Q_0},$$

where Q_0 is the quasi-TEM mode quality factor that is given by [2, equation 37]:

$$\frac{1}{Q_0} = \frac{1}{Q_d} + \frac{1}{Q_c},$$

Q_c, is the microstrip inductive quality factor that is given by [2, equation 34]:

$$Q_c = \frac{\pi hf}{c}\ \frac{Z_{0,0,1}(u)}{R_s(\phi)}\ \frac{u}{K}.$$

and Q_d, is the microstrip capacitive quality factor and, for a microstrip line having an air dielectric above the signal line, is [2, equation 33]:

$$Q_d = \frac{(1 - q) + q\varepsilon_r}{q\varepsilon_r\ \tan\delta}.$$

The $R_S(\phi)$ is the skin effect resistance given in 6.1.2. The parameter q is the effective filling fraction for the mixed dielectrics (air plus substrate) of a microstrip transmission line [5]:

$$q = \frac{\varepsilon_{r,eff}(f) - 1}{\varepsilon_r - 1}.$$

The parameter K is the microstrip current distribution factor given by [2, equation 36]:

$$K = \exp\left(-1.2\left[\frac{Z_{0,0,1}(u)}{\eta_0}\right]^{0.7}\right).$$

1. S.B.Cohn, ''Problems in strip transmission lines,'' IEEE Transactions on Microwave Theory and Techniques, Vol. MTT-3, March 1955, pp. 119-126.
2. E. Hammerstad and O. Jensen, ''Accurate models for microstrip computer-aided design,'' IEEE Microwave Symposium Digest, May 1980, Washington, D.C., pp. 407-409.
3. S.B. Cohn, ''Characteristic impedance of the shielded-strip transmission line,'' IRE Transactions on Microwave Theory and Techniques, Vol. MTT-2, July 1954, pp. 52-57.
4. M. Kirschning and R.H. Jansen, ''Accurate model for effective dielectric constant of microstrip with validity up to millimetre-wave frequencies,'' Electronic Letters, Vol. 18, No. 6, March 1982, pp. 72-273.
5. K.C. Gupta, R. Garg, and I.J. Bahl, Microstrip Lines and Slotlines, Atrech House, Dedham, MA, USA, 1979.

7 DETAILED BOARD REQUIREMENTS

7.1 Machined Features

7.1.1 Dimensioning and Tolerancing Dimensioning and tolerancing of fabricated features are extremely important to each printed circuit board design. On a specification of hole diameter, for example, the nominal diameter and the bilateral tolerance might be given as 0.8 mm, +0.1 mm, -0.05 mm [0.031 in, +0.004 in, -0.002 in]. This example creates a tolerance band of 0.15 mm [0.006 in]. Bilateral tolerancing and true-position tolerancing (IPC-2615) are typically used.

Manufacturability can often be improved by true-position dimensioning and tolerancing which, simply stated, gives the manufacturer a tolerance budget that can be distributed between position and size in any proportion. Thus, the designer defines functionality requirements and gives the manufacturer the freedom to apply the majority of the tolerance to the least precise process.

IPC-2615 requires that a tolerance of position must specify M (maximum material condition), L (least material condition), or S (regardless of feature size). Drawings generated

prior to 1982 are assumed to imply maximum material condition with respect to an individual tolerance, datum reference(s), or both, where no condition is specified (Rule 2A - Past practice alternate position tolerance rule).

Ability to hold positional tolerances varies significantly according to material type (inherent dimensional stability), thickness, and overall part dimensions. A true-position diameter of 0.254 mm [0.01 in] is most common and readily attained. Manufacturability is adversely affected for tolerances tighter than about 0.152 mm [0.006 in]. Whenever appropriate, the maximum material condition should be specified to permit the manufacturer to balance hole diameter tolerances and positional tolerances to increase manufacturability.

Simply stated, maximum material condition requires that when a hole is produced at its smallest diameter (bottom of the tolerance band for the hole diameter), the stated true-position tolerance applies. However, holes produced at larger, acceptable diameters can often be positioned with less accuracy and still provide for fit and function. Thus, for larger holes, a bonus position tolerance is obtained that is equal to the acceptable increase in hole diameter relative to the minimum hole diameter. This bonus tolerance is added to the true position tolerance to establish the inspection tolerance.

When least material condition applies, the stated tolerance is when the hole is produced at its largest possible diameter. ''Regardless of feature size'' implies that the tolerance applies as stated, with no bonus tolerance and feature size tolerances based on the various process capabilities available.

Although true-position dimensioning and tolerancing can apply to most any conceivable feature, it is most appropriate and preferred when specifying locations of holes, pockets, and other similar features where the positions in both the x and y directions are each important. Consider, for example, interconnect holes that require some minimum annular ring, or holes that may be used in assembly for tooling or component installation. The radial deviation of the hole position from nominal will limit usability of a board.

Since true-position tolerance zones are mostly elliptical (cylindrical when considering the Z axis and circular when the x and y tolerances are nominally equal), they best describe the distribution of measurements that will meet assembly and performance requirements. In contrast, the square tolerance zone defined by bilateral tolerancing of the X and Y dimensions independently may exclude acceptable features, or include rejectable features, with a resulting negative impact on total system cost over the long run.

This is demonstrated in Figure 7-1, where we assume that the assembly process requires a radial deviation from nominal of 0.13 mm [0.005 in] or less. This is translated into a true position tolerance diameter of 0.25 mm [0.010 in]. If the 0.13 mm [0.005 in] radial tolerance is simply converted into a bilateral tolerance of ± 0.13 mm [0.005 in], a family of features will exist that do not meet the assembly requirements, but will be considered acceptable. In fact, over 21 % of the area of the square tolerance zone includes unacceptable feature locations and this may cause excessively high board rejection rates in assembly.

On the other hand, if a bilateral tolerance zone is simply inscribed in the circular tolerance zone (a very common error), an unnecessarily small bilateral tolerance is specified that excludes acceptable features. In this case, over 36 % of the circular (acceptable) tolerance zone is excluded, perhaps resulting in excessive part procurement costs. Note that the 21 % and 36 % ''error zones'' do not reflect 21 % or 36 % of the parts produced, since the distribution of machine error would be expected to be approximately normal, not uniform.

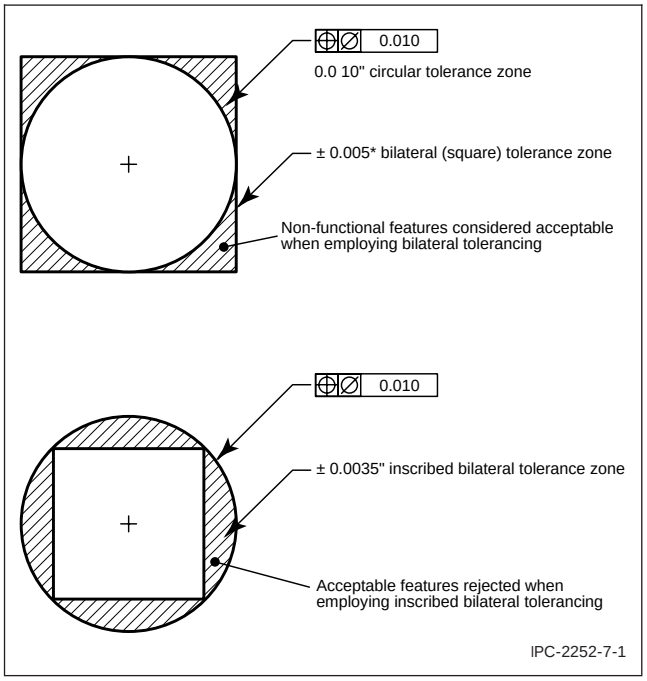

Figure 7-1 Comparison of Bilateral and True-Position Tolerancing Methods

7.1.2 Plated-Through Holes Hole diameter minimums are limited by the overall material thickness. A difficulty factor often cited is the aspect ratio (the ratio of material thickness to hole diameter). For example, a hole aspect ratio of 5:1 on a stripline circuit board 3.3 mm [0.130 in] thick overall would suggest a minimum hole diameter limit of 0.66 mm [0.026 in].

As a general rule, holes with aspect ratios of approximately 3 are easy to fabricate, of approximately 5 are difficult to fabricate, and of 10 are extremely difficult or impossible to fabricate, depending on the material thickness; that is, high aspect ratios provide less difficulty on thinner materials.

Higher aspect ratio holes are more difficult to drill. For the smaller drill sizes, less than 0.33 mm [0.013 in] diameter, drill breakage and hole roughness can be a substantial problem. In addition, higher aspect ratio holes are difficult to clean, activate, and plate. Plating distribution is not usually uniform throughout the hole volume due to the limited accessibility by the solution. This limited accessibility reduces mass transport of ions and molecules to the hole in chemical treating and rinsing, and complicates the primary current distributions in electroprocesses (plating, etching).

Hole diameters can be specified as before or after plating. Plating reduces hole diameter by twice the plating thickness. The tolerance on hole diameter after plating is limited by the tolerances of the drilling and plating processes. Tolerance bands (the sum of the plus and minus deviations from nominal) of 0.13 mm to 0.25 mm [0.005 in to 0.010 in] are most often seen, although tighter tolerances can be achieved. Generally, cost and difficulty of manufacturing boards increases as hole diameter tolerances are reduced. Note that for aspect ratios greater than 4:1, tolerances should be increased by up to 0.10 mm [0.004 in].

Hole size after plating can be difficult to predict accurately due to variations in plating current distribution. Hole size, hole density, and sizes and shapes of adjacent circuits and ground planes will affect metallization thickness in a particular hole due to variability in the local current density. Often specifying hole sizes before plating and specifying a minimum (but not maximum) plating thickness will improve manufacturability. Specifying a minimum plating thickness is most appropriate where plated-through-holes function as mode suppression grounding or as inner layer interconnection vias. For holes to be used in leaded components, an overall bilateral tolerance on hole size should be considered.

When electroplated tin/lead is to be reflowed or fused, hole size should only be specified as prior to reflow. During the reflow operation, the individual part design including pad size, hole size, material thickness, and trace thickness, will influence the amount of solder flow and any dimensional measurement subsequent to that process. Via holes used for mode suppression may or may not be partially or completely closed by plating.

7.1.2.1 Pinning/Ground Connections Press fit pins are used primarily for establishing ground connections on metal-backed substrates. The key to successful use of pin technology is having the proper interference fit (pin diameter > hole diameter) between the pin and the metal backing. Except for the roll pin, pins are solid and require an interference fit. Typically, for good grounding, the interference should be between 0.04 mm to 0.05 mm [0.0016 in to 0.002 in]. For example, if the pin diameter is 1.19 mm [0.047 in], then the drilled hole should be about 1.14 mm [0.045 in] in diameter. Fortunately, a 1.15 mm [0.0452 in] drill is just right for this application. When using press fit pins, the diameter should be chosen carefully so that standard or metric drill sizes can be used.

Types of pins commonly used:

1. *Roll Pins* Standard steel pins, tin plated for soldering (see Figure 7-2). Roll pins maintain a continuous pressure on the hole walls after insertion. However, they must be inserted in such a way that 0.75 mm to 1.0 mm [0.030 in to-0.040 in] is protruding above the surface of the circuitry. Care must be used in soldering to prevent flux and/or solder from getting inside the hollow portion of the pins.

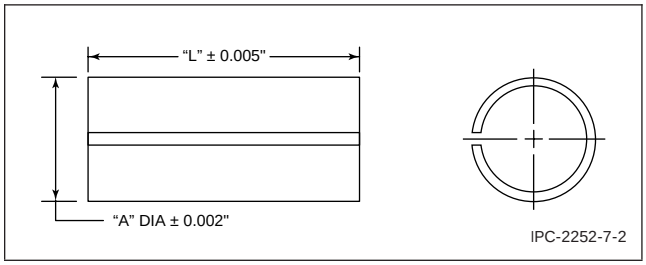

Figure 7-2 Roll Pin

2. *Solid Pins* Solid pins are typically brass with tin plate over copper plate to improve solderability. These pins are available in various diameters and lengths. Select from pin diameters to avoid requirements for special drill bit or reamer sizes. Solid pins are inserted flush with the circuit surface or can be left slightly above the surface, typically from 0.25 mm to 0.4 mm [0.010 in to 0.015 in]. The flush mounted pin allows for device leads to be soldered directly to the head of the pin, therefore allowing the shortest possible ground lead. Roll pins are shown in Figures 7-3 and 7-4.

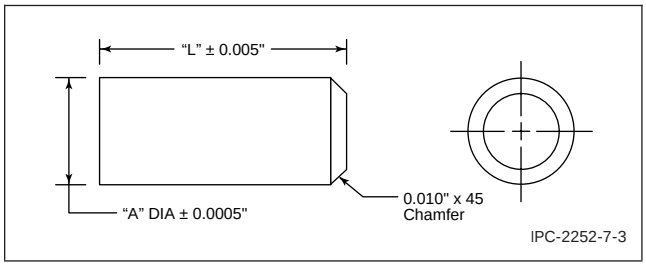

Figure 7-3 Straight Headless Pin (Solid)

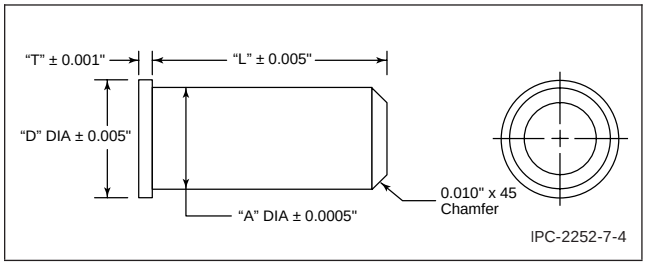

Figure 7-4 Straight Headed Pin (Solid)

Regardless of the type of pin used, all pins must be soldered to the circuitry for proper connection. Solder preforms, solder paste, or regular solder may be used for soldering. The soldering may be done using vapor phase, infrared, or hand soldering.

7.1.3 Unplated Holes Positional tolerances for unplated holes are the same as for plated holes. Hole diameters can be more tightly toleranced. Manufacturability is reduced for unilateral tolerances less than 0.10 mm [0.004 in] for diameters up to 0.75 mm [0.030 in], 0.13 mm [0.005 in] for diameters up to 1.5 mm [0.059 in], and 0.15 mm [0.006 in] for diameters greater than 1.5 mm [0.059 in]. Avoid specifying tight tolerances for hole sizes that are not standard drill sizes, since custom-sized drill bits usually have long lead times for delivery.

7.1.4 Depth Pockets and Slots Tolerances on feature locations are the same as for through-hole locations. Tolerances on feature sizes are limited by cutter tolerances and positional tolerances, and are typically ± 0.13 mm [0.005 in] for CNC drilling/routing machines and ± 0.075 mm [0.003 in] for CNC milling machines. Increased tolerances, up to ± 0.25 mm [0.00984 in], should be used for materials with thicknesses greater than 2.5 mm [0.0984 in]. Smaller tolerances may be obtained on labor intensive manual machines.

Depth tolerances are limited by the machine tolerance and, more importantly, by the material thickness tolerance, especially when specifying ''material removed.'' Typical depth tolerances are ± 0.56 mm [0.022 in] plus the material thickness tolerance. When appropriate, the material thickness tolerance can be ignored by specifying ''material remaining.'' If ''material removed'' is most important to your design, very small material thickness tolerances should be specified.

Since all pockets and slots are produced by cylindrical tools, corners must have a specified radius. Larger radii permit the use of larger cutting tools and this allows higher feed rates which reduce manufacturing costs. A 1.2 mm [0.047 in] radius is preferred, and a minimum of 0.8 mm [0.031 in] is recommended. Where ''square'' corners are required, one must be able to cut past the 90 degree corners in one direction thus leaving an ''ear-slot.''

7.1.5 Inner-Layer Access Machining An efficient means for fabricating bonded assembly access cavities requires two precision depth cuts, one from each cover board of the cavity. It is useful to permit a step in the access cavity sidewall of up to 0.50 mm [0.020 in]. This step is usually the result of oversizing that portion of the access cavity closest to the circuit layer. Note that such oversizing allows room for the bead of adhesive that is useful for sealing the bond line.

7.1.6 Periphery Parts (printed wiring boards) are usually cut from a larger board or a panel by CNC routing. This approach requires at least two internal non-plated tooling holes. Tooling hole diameters must be large enough to permit precise registration of the panel to the router. Generally, the tooling hole diameter should be at least equal to the material thickness, and no less than 0.8 mm [0.031 in] for thinner materials. For thicker material (>3.2 mm [0.125 in]), available board area may limit the tooling hole size. Periphery tolerances of ± 0.13 mm [0.005 in] are most common. Manufacturability will be reduced for tolerances less that ± 0.13 mm [0.005 in].

For high part quantities or peripheries that cannot be achieved with routing, such as on materials less than 0.8 mm [0.031 in] thick, one generally builds a punch and die or a steel rule die to stamp out the part periphery. Depending on shape complexity, size, and number of hits, the cost for this tool can range between hundreds and thousands of dollars. Very complex peripheries require a more expensive progressive punch and die set. For a steel rule die, tolerances of ± 0.18 mm [0.007 in] can usually be held. For a hard steel punch and die, tolerances of ± 0.05 mm [0.002 in] can be held. Other methods for cutting part peripheries such as electrodischarge machining (EDM), lasers and water jets are also used.

7.1.7 Numerically Controlled (NC) Equipment Most drilling, routing and milling equipment is typically controlled by numerical data supplied to the machine controller electronically. However, some older machines use paper tape to transfer the data. The format of the data is dictated by the capability of the controller and the equipment used. Most fabricators can use the data generated by computer-aided-design (CAD) software to drive their equipment directly or, if necessary, convert the CAD data to a format that can be accepted by their equipment. There are data formats adopted by the electronics industry to facilitate transfer and use of data, one such standard is the Gerber format.

7.1.8 Dimensional Inspection Dimensions of machined features can be verified using a variety of inspection tools such as pin gages, calipers, micrometers, depth gages, etc. Almost all fabrication facilities have either automatic inspection equipment or manual equipment fitted with precision digital readout devices.

7.2 Imaging Imaging, in this context, is the transfer of the artwork (see 7.2.1) image generated by the designer, onto the board to form the circuit. To transfer an image, a photoresponsive material (the photoresist, see 7.2.2) is first applied to the board. The photoresist is then exposed to light, through a photomask, and the excess resist removed. For positive resists, the exposed resist is removed whereas for negative resists the unexposed resist is removed. The

copper is then placed in an etchant and areas that are not protected by resist are removed. Because of different fabrication processes, the design geometry may not be accurately replicated onto the board unless appropriately compensated.

The uncompensated design geometries of the board circuitry, in the form of digital data, should be supplied to the fabricator who can then compensate that data for their fabrication processes to ensure that the design geometries are replicated in the finished board. The fabricator will normally select the sequence needed to fabricate the board from standard processes. Where lines and spaces are less than 0.25 mm [0.010 in] and require plating, pattern plate is almost always used. Pattern plate is the commonly used process whereby only the circuit pattern is plated. Most processes use a protective plate and this plate is removed after the etch if it does not provide the desired surface finish. Pattern plate uses positive-image artwork but to the designer this is not important, what is important is that the finer the lines and spaces required, the more the board will cost. Furthermore, there is a limit to the width of lines and spaces below which the board can only be produced by a facility with specialized equipment and knowledge.

For manufacturability, target location tolerance should consume no more than 10 % of the most demanding fabrication tolerance. Also it should be remembered that the board fabricator will compensate the artwork for their process to achieve the required geometries, and that spacing between conductors less than 0.125 mm [0.005 in] increases the cost of the board. How much the fabrication process adds to the cost of the board depends on the etch factor. The etch factor is defined here as the distance etched laterally into the copper divided by the distance etched vertically into the copper.

The etch factor is used to predict line width reduction. Etching typically reduces the width of conductors and increases the spacing between conductors. The etch factor is not only dependent on the etch process, but also on the geometries within the pattern to be etched.

The print (or drawing) of the artwork should include specifications of the smallest line and space widths contained in the circuitry and transmission line impedances if the board contains controlled impedance lines. Typically, additional fabrication costs are not incurred if the impedance tolerance is specified as ± 15 %. Tighter impedance tolerances will likely increase the cost of board fabrication.

7.2.1 Artwork In general, negative artwork is used for print and etch applications and positive artwork for pattern plating. Artwork should be supplied as a ''one-time,'' right reading, and emulsion-down. Artworks should never be expanded by the customer for etch back considerations. Modifying artworks should be handled by the vendor to fit particular manufacturing processes. Artwork supplied on CAD should meet Gerber format standards. Copies of the artwork should accompany CAD data whenever possible to aid in verifying plotted CAD artworks. Mylar film artwork will become dimensionally unstable in varying temperatures and humidity. Mylar film artwork expands and contracts with changes in temperature and relative humidity by 0.0025 % per °C and 0.0012 % per %RH. Thus, over a 25 cm [10 in] dimension, features can move by ± 0.008 mm [0.0003 in] with temperature and ± 0.015 mm [0.0006 in] with humidity in a well-controlled environment (temperature ± 1 °C and relative humidity ± 5%). Glass masters are always recommended when this amount of movement is intolerable. The circuit designer needs to understand that artwork is used to define the layer features. Small feature geometries increase the cost of a board because these features will require more sophisticated fabrication techniques to replicated the image onto the board. In the worst case, glass master photomasks may be required to make a board. The glass masters are both expensive and easily damaged if not properly handled.

7.2.2 Photoresist Photoresist is used to transfer the artwork images onto the copper, which after etching of the unwanted copper, results in the circuitry. Dry-film photoresist is typically used to transfer the design image onto the copper. Standard resists are approximately 0.05 mm [0.002 in] thick. Thicker, stronger resist 0.075 mm [0.003 in] is used when tenting over large features; thinner dry-film resist (down to 0.013 mm [0.0005 in] or liquid resist is used for fine line/gap imaging. As a general rule, gap widths in dry-film resists can be readily imaged down to twice the resist thickness. However, gap widths equal to the resist thickness are attainable with difficulty and a corresponding yield loss.

Thinner resists are more susceptible to pinholes caused by airborne particulates in the photo imaging area, scratches, and other handling damage. As a general rule, manufacturability will be reduced for line widths less than about 0.10 mm [0.004 in].

7.2.3 Annular Rings For isolated annular rings at the end of a plated-through hole, it is recommended that the width of the annular ring extend a minimum of 0.30 mm [0.012 in] from the hole edge or be 0.61 mm [0.024 in] larger in diameter than the hole. Given the variability of drilling, plating, and imaging processes, this could result in a nominal annular ring width of 0.15 mm [0.006 in]. To improve plated-through hole reliability during Z-axis expansion, annular rings, 0.38 mm [0.015 in] or larger are recommended. This size of annular ring is also recommended for plated-through holes in PTFE.

The use of unsupported plated-through holes that do not terminate at the surface of the board in an annular ring, pad area, or ground plane are discouraged. This is because

unsupported plating is not mechanically strong enough to prevent handling and assembly damage. Unsupported edge plating of cutouts and cavities is also strongly discouraged.

7.3 PTFE Activation Sodium etches, or bondizing, are treatments that ''activate'' PTFE, converting the hydrophobic (water repelling) surface into a hydrophilic (wettable) surface. Plasma etching is also used as a surface treatment for PTFE activation. No functional detectable changes to the electrical properties of the substrate have been reported, as long as the surfaces are properly cleaned after activation.

PTFE etching solutions contain metallic sodium complexed with hydrocarbons that are extremely reactive with oxygen in air or moisture and must be handled with special precautions to prevent contact with moisture and air. PTFE surface activation is required for any subsequent electroless plating, conductive coating, or adhesive bonding process, and tends to discolor (darken) the PTFE surface in a random manner.

The activated PTFE surface has a limited shelf life that is reduced by exposure to light (especially ultraviolet), contamination and mechanical scrubbing or rubbing of the surface. If you require parts having PTFE activation as a final treatment, they should be shipped in black plastic bags, stored in a clean, dry atmosphere, and used soon after receipt.

7.4 Metallization

7.4.1 Plated Edge Designs Edge plating is a popular technique in multilayer applications to reduce the number of mode suppression plated-through holes. Edge plating designs should include three to four tabs 6.4 mm [0.250 in] wide to hold the piece connected to the panel. This allows processing many pieces in panel form. Edge plating must wrap the top and bottom side of the piece by a minimum of 1.3 mm [0.050 in] to give a strong mechanical bond. Plating thickness should be 0.025 mm [0.001 in] minimum.

7.4.2 Copper Plating Before electrolytic plating, all exposed dielectric (such as, through-hole barrels, edges) and metal surfaces are covered with electroless copper or a conductive coating (see sec. 5.3.2.1). Copper is then electroplated to the required thickness in either a panel or pattern plate scheme.

As a general rule, panel plating is preferred where plating thickness uniformity is most critical, since the image does not influence the plating distribution. In addition, where thick metallization is required, panel plating permits heavy buildup of metal without bridging over the plating resist film. In contrast, pattern plating is preferred when line/gap tolerances are most critical, since the thickness and uniformity of copper to be etched away are dictated only by the copper cladding.

The mechanical properties of plated copper determine the thermal shock resistance and thermal cycle resistance of plated-through holes to cracking during soldering, assembly, and environmental thermal cycling. The copper must be ductile enough to withstand the high thermomechanical stresses generated at soldering temperature and strong enough to resist the fatigue failures resulting from smaller environmental thermomechanical stresses. For high reliability, it is recommended that the board fabricators using acid copper plating systems have the capability to electrodeposit copper having an elongation of at least 20 % and tensile strength of at least 2.76×10^8 Pa.

Plating thicknesses are usually specified as minimum thickness in the plated-through hole barrel. Frequently, print specifications will require a minimum of 0.025 mm [0.001 in] of copper on the sidewall of a plated-through hole. Keep in mind that a 0.025 mm [0.001 in] minimum plating in the hole may result in a 0.04 mm to 0.05 mm [0.0015 in to 0.002 in] thick plating on all other surfaces. Plating thicknesses greater than 0.05 mm [0.002 in] can create problems with etch precision unless pattern plating is used.

The hole pattern will affect metal distribution for panel and pattern plating. Isolated holes will plate faster than densely-packed hole patterns. The percent of metal covering the plated area will dictate metal thickness uniformity across the part. Thickness tolerances should be greater for parts where hole patterns or images are not uniformly distributed. Plated copper thickness tolerance of ± 0.013 mm [0.0005 in] are typical, and manufacturability will be reduced (depending on the part) for tolerances of ± 0.005 mm [0.0002 in] or less.

When total metallization or overall part thickness is specified, tolerances should reflect the sum of the plating tolerance, plus the copper foil thickness and/or dielectric thickness tolerances. Copper foil thickness is specified by copper weight per unit area (ounces/square foot) in IPC-MF-150.

Rolled copper has a tighter thickness tolerance (± 5 % by weight) than electrodeposited copper (± 10 % by weight). The referee method for evaluating thickness is weight on a $0.164 m^2$ [254 in^2] specimen. Thus foil thickness may vary appreciably across a panel and still meet the specification. Foil thickness variations of up to ± 0.005 mm [0.0002 in] for 1/2-oz. (17µm [0.00067 in] thick) copper have been observed.

Total metallization thickness is evaluated by microscopic examination of polished and etched microsections of coupons. Internal coupons are placed in areas near parts that are later cut out of the panel; internal coupons give the best indication of part thickness. If internal coupons are not used, coupons can be added to border area, or parts can be destructively tested.

7.5 Etching Final manufacturing tolerances are the sum of individual imaging and etching tolerances.

Gaps are more difficult to image and etch than lines. Whenever possible, for high circuit density applications, specify gaps larger than their associated line widths. Manufacturability is usually reduced for lines and gaps less than 0.10 mm [0.004 in] wide.

It is extremely difficult to achieve line widths less than twice the copper cladding (plus any panel plating) thickness. This implies a minimum feasible line width of 0.035 mm [0.0014 in] for 1/2-oz. (0.017 mm [0.00067 in]) copper, and 0.070 mm [0.0028 in] for 1-oz (0.035 mm [0.0014 in]) copper. Usually, it is best to minimize the required copper foil cladding thickness.

Isolated narrow lines with large associated gaps are easier to etch than a cluster of fine lines grouped closely together. Sharp corners where lines change direction are more difficult to image and etch than more gradual curved or 45 degree mitered corners.

During etching, the lateral undercutting of copper under the resist reduces line widths and increases gap widths by an amount proportional to the amount of copper cladding (and any panel plating) which must be removed to define the circuitry. The etch factor predicts the amount of undercutting that will occur and is typically equal to one-half the etched copper thickness per side when dry-film resists are employed.

There is also some variation in etch factor due to normal variations in the etch process parameters and the specific circuit pattern to be etched. Etch factor variation is typically ± 50 %, so recommended etch factors can be 0.018 mm ± 0.0075 mm [0.0007 in ± 0.0003 in] for 1/2-oz (0.017 mm [0.0007 in] thick) copper, and 0.035 mm ± 0.018 mm [0.0014 in ± 0.0007 in] for 1-oz (0.035 mm [0.0014 in]) copper.

Where metals like gold or tin/lead are used as the etch resist, undercutting is increased due to the galvanic attack of copper in contact with the more noble metal resist. When compared with dry-film resist, etch factors can be up to 100 % larger for gold resist and 50 % larger for tin/lead resist.

For heavy panel-plated parts, standard etching tolerances can be 150 % of the total metal thickness to be etched. Smaller tolerances will impact manufacturability engineering and interaction with the customer.

7.6 Bonding Two basic methods exist for bonding a microstrip circuit to a metal plate ground or heat sink. When the microstrip has metallization (copper foil for the circuitry) on one side only, an electrically nonconductive adhesive can be used. Thermoset and thermoplastic adhesives are satisfactory. For the second method, used when the microstrip circuit is metallized on both sides, an electrically conductive thermoset adhesive is the material of choice. Laminating with either conductive or nonconductive adhesives is done in an autoclave or a hydraulic press under conditions specified by the adhesive manufacturers.

Each bonding material and method has drawbacks as well as advantages. Tin/lead solders can be used as conductive adhesives under certain conditions, but delamination will result if solder melt temperatures are exceeded in subsequent processing. Nonconductive, low melting thermoplastic adhesives do not provide as strong a bond as that of a board pre-bonded to a metal plate. Thermoset adhesives will affect the electrical properties of the PTFE-based printed wiring board. Conductive adhesives cannot exploit the inherent dimensional stability of the PTFE substrate. However, when substrates are pre-bonded to the metal plate, machining of the assembly will not be as straightforward as it is for separate metal and dielectric parts. Also, pre-bonded materials add more steps and complexity to plating operations.

7.7 Multiple Material Multilayers A multilayer board can be made where layers of different materials are used. Using different materials helps to minimize the use of high cost materials, which typically are materials with permittivities outside the range of the permittivities of conventional epoxy-based laminates (that is, where $3.8 \leq \varepsilon_r \leq 4.6$). Building a multiple material multilayer board requires special knowledge, and it is recommended that the material suppliers be consulted before trying to build these types of boards.

7.8 Testing Tests for electrical opens and shorts in the board circuitry should be performed according to IPC-6018. The circuitry should also be tested to ensure that the desired electrical properties, such as capacitance, resistance, and characteristic impedance are provided. See IPC-9252 for guidance on measuring these electrical properties. Test plans must be developed for each specific design.

8 DEVICE ATTACHMENTS AND PACKAGING

8.1 Attaching the Circuit to the Housing The attachment of the circuit into the housing can be broken down into five different categories.

8.1.1 Mechanical Mounting Mechanical mounting incorporates various fasteners, such as, screws, bolts, washers, and rivets. Typically the printed wiring board contains a ground plane and the board is fastened to the housing such that the ground plane is in mechanical contact with the housing. The mechanical contact provides adequate electrical continuity between the circuit ground plane and the housing. The housing provides either chassis or earth ground. If the circuit ground planes are not at the surfaces

of the board, metal areas on the top of the board can become ground pads by connecting them to the buried ground planes using plated through holes. These ground pads can be, for example, 6.35 mm to 12.7 mm [0.25 in to 0.5 in] in diameter. It is recommended that three to six plated through holes are located within the ground pad and connect to the buried ground plane. The additional plated through holes provide a lower inductance connection between the ground pad and the buried ground plane. Furthermore, the use of fasteners may increase the risk of breaking the contact between the ground pad and buried ground, and this risk is reduced by extra plated through holes. To reduce inductance and increase contact strength, it is further recommended that the plated through hole connecting the ground pad to the buried ground plane be solid filled and have no thermal reliefs. This same fastening method can also be used even if the circuit does not have a ground plane. In this case, the housing becomes the circuit ground plane.

8.1.1.1 PTFE Considerations PTFE laminates are soft substrates. If the fasteners are tightened down too hard, the substrate will readily deform. Even if the circuit is fastened down with the appropriate force, the laminate will still cold flow due to the pressure around the fastener head. Consequently, with time, the circuit will become loose. A technique to overcome this problem is to use a heavy metal backed board where the dielectric is machined away from the mounting holes. One can use an aluminum, brass or copper plate on the back side of the circuit. The dielectric is machined away from the areas where the mounting fasteners hold the board to the housing in such a way that the head of the fastener is against the heavy metal rather than the soft dielectric material.

Since not all PTFE boards are designed with thick metal backing, another method is to take precautions when screwing the circuit into the housing. Since the material will cold flow if the screw head is in contact with the material, the pressure of the fastener can be distributed over a larger laminate area by using copper lands or washers. A proven method for attaching the board to the housing is the use of a Belleville spring washer, which not only distributes the pressure over a wider area, but also provides a strain relief from the spring action.

8.1.2 Epoxies (both conductive and nonconductive) Epoxies, both conductive and nonconductive, can be used to mount a board into a metal housing. Either epoxy can be used when there is no ground plane on the back side (side making contact with the housing) of the board. However, care must be taken with either epoxy to properly treat the bare laminate to assure a good bond between the epoxy and the laminate. Treatments that can be used are plasma or sodium etching. A conductive epoxy should be used when a ground plane is present on the back side of the board. Using a nonconductive epoxy on a board with a ground plane can cause floating grounds and other interconnecting problems.

Conductive epoxies are thermosetting resins filled with a metal powder, typically silver. A curing agent, such as an amine, is mixed with the resin prior to use. The surfaces to be bonded are brushed or dipped with the resin mixture. Any solvent used to dilute the resins must be evaporated (at a temperature below the curing temperature) before the two parts are pressed together. The assembly is baked for the manufacturer's recommended time and temperature to cure the adhesive. A jig or fixture may be required to hold the circuit board flat during the bake cycle.

Metal filled epoxies tend to be brittle and do not accommodate different thermal expansion between the housing and circuit board. Avoid them for applications that will see a large range of temperatures. It is important to select a conductive epoxy that meets the desired electrical requirements. It is also important to specify the proper mix of epoxy to metal filler. When applying the epoxy to a surface, it should be applied evenly. The quality of the electrical connection made with a metal filled epoxy should be checked with a milliohm meter to ensure that the epoxy has been properly cured. In addition, the RF performance of the epoxy connection should be checked over the frequency range that the board will be used to ensure the epoxy-metal mixture is correct.

Epoxy resin systems are available in a wide range of curing temperatures, and one which meets the environmental requirements should be chosen. Another consideration in selecting a resin system is its mechanical properties after cure. Hard or brittle resins will not withstand temperature cycling. What is preferred in the case of frequent temperature cycling is a resin system with good elongation and low tensile moduli. Attention to the curing agent should be paid. For example, some amines will react with copper and result in an under cured resin. The supplier of the resin can advise on this.

Some users of epoxy bonding systems have observed bond failure between aluminum and the adhesive with time. This problem may be avoided by plating the housing before bonding.

8.1.3 Thermoplastic Films Thermoplastic films described in 5.2.1 may also be used for mounting the circuit board into the housing. Such films are suitable only for circuit boards without a ground plane. Bonding procedures follow those described for multilayer circuits; however, fixturing may be more complex in this case. The objective is to ensure uniform pressure over the whole board area. The film should be cut slightly smaller than the board to allow for film flow at the edges.

Film bonded housings show excellent environmental resistance, including tolerance to thermal cycling, since all the

films have excellent elongation characteristics and low tensile moduli. For the high dielectric constant substrates, along with nonconductive epoxy mountings, film bonding is not recommended because the effective permittivity of the mixed dielectric media (laminate plus air plus epoxy) is lowered by the presence of the low permittivity thermoplastic film. See definition of Effective Permittivity in 1.3.

8.1.4 Soldering Soldering the finished circuit board into the metal housing is perhaps the most commonly used method for mounting a board to a housing. To mount the board, the back side of the circuit is solder plated or coated with solder by a reflow process. The base of the housing is also solder plated. If the housing is aluminum, which is frequently the case, surface preparation, for example copper or tin plating, must precede the solder coating.

To mount the board, the circuit board is put in position on the housing and the housing is heated above the solder melting temperature, and then cooled. For small parts, this is a simple operation. For large and complex shaped parts, some kind of jig or fixture may be required to ensure that the circuit board is held flat against the housing and that it makes good contact to the housing over its entire surface area. Heating may be done on a hot plate, in hot air, or an infrared oven. This method of attaching the board to the housing gives good electrical and thermal conductivity between the circuit board and the housing. The environmental reliability of this type of mounting is also good provided there is no entrapped air or solder flux between the board and the housing.

8.1.4.1 Temperature Caution Care must be used to avoid high temperatures during the solder process that may damage temperature sensitive devices, such as hybrids, voltage-controlled oscillators, relays, mixers, modulators/demodulators, etc. These devices may contain internally soldered components which become unsoldered in a subsequent solder process or are otherwise damaged by temperature. The temperature processing limits of each device should be checked prior to attaching it with a solder process.

8.1.5 Direct Bonding The direct bonding method is the newest technology. In this type of bonding, no bonding film is used and the circuit board has no ground plane. The circuit and housing assembly are placed in contact and taken above the melting point of the laminate while pressure is applied. The time, temperature and pressure of the bonding process are adjusted and controlled to ensure that the circuit board will bond to the housing. In the case of PTFE laminates, a temperature of 390 °C is recommended, which is well above the PTFE melting temperature of 327 °C. Pressures of $1.4x.10^6$ Pa [200 psi] and a dwell time of 15 minutes to 20 minutes should give an adequate bond. The temperature capabilities of some presses could make this method difficult to use for some applications. Another limitation is that plated through holes, from the circuit to the ground plane, are not easily attained. The effect of temperature on device attachment should be considered (see 8.1.4.1).

8.2 Connector Attachment This section describes the methods and demonstrates the techniques of mounting connectors to the board that will work and what the concerns are when using these methods. The engineer can use this information to help in mounting or connecting the chosen connector.

Most of the difficulties associated with making reliable connector mounts are due to the thermal expansion differences between the substrate and the connector that puts stress on the pin solder joint. The misalignment of the connector with respect to the pin will greatly aggravate the thermal expansion problem. For this reason, it is strongly recommended that the connector body be mounted directly to the circuit board itself rather than to the housing. Furthermore, it is very difficult to accurately align the pin to the connector if the connector body is attached to the housing. Also, if the connector were mounted to the housing, thermal expansion of the housing would become an issue.

8.2.1 Edge Connector In the edge mounted coaxial connector, the pin is first soldered to the exposed trace at the board edge. The access hole can also be filled with a plug of the dielectric which was punched out from the board. The plug should have a relief slot cut in the bottom to accommodate the pin solder joint. If enough care is taken to get a good smooth solder connection, the relief cut in the plug can be eliminated. The plug need not be bonded into place because the connector body will hold it into place. After the connector is assembled over the pin, the body is fastened to the board. To ensure that the connector body is correctly aligned with the pin, it is important to assemble and tighten the connector before the mounting screws are put in place. The mounting holes in the circuit board should be larger than the screw diameter (oversized holes) to allow for alignment of the connector to the pin.

Circuit boards which are mounted onto thick metal backers use a similar connector mounting technique. Again the pin is soldered to the metal trace, and the connector is assembled and tightened before screwing the body of the connector to the thick metal backer. In this case, the mounting screws are fitted into holes that have been drilled and tapped in the thick metal ground plane.

Soldering the pin in place can be difficult. Also, positioning the pin in the correct place and at right angles to the board can be difficult. To alleviate this problem, some people design a pin holding fixture or use the connector body as a fixture to hold the pin in place while soldering. If the connector itself is used as the mounting fixture, then

after soldering, the connector should be disassembled, re-assembled, and then screwed down to assure that the pin and body are in perfect alignment.

8.2.2 Surface Connector Figure 8-1 shows a method of mounting the pin of a surface connector to a buried land in a bonded stripline package. An access hole is put in the cover board prior to bonding. The pin is soldered to the exposed land and a plug of the dielectric material is cut to fit over the pin into the access hole. After plugging the hole, the connector is assembled and screwed down to the surface. The mounting holes are usually plated through for mode suppression at the transition between the board and the connector, and are made oversized to allow for alignment of the pin to the connector body. Another method used for mounting a connector is to solder plate all the pin lands and the heads of all the pins, then place all the pins into the cover board, position the pre-punched bonding film in place, and finally place the circuit board over the entire construction to hold everything in place during soldering. The bonding film and solder should be chosen that melt at approximately the same temperature. During the bonding operation, the solder will reflow and solder all the pins in place. This technique works well with large or small numbers of pins. The one major disadvantage is that inspection of the solder joint is impossible.

Figure 8-2 shows another method for attaching a surface connector to a circuit board. Here the access hole is put into the cover board and a hole is drilled through the copper land and dielectric of the circuit board to accommodate the pin. The pin is then inserted into the hole and soldered. The connector is assembled and screwed down from the circuit board side. Finally a dielectric plug is put into the cover board. This plug will require a method of holding it in place, which can be done by soldering a piece of thin copper metal over the plug to the ground plane.

8.3 Device Attachment For high volume production of microwave circuit assemblies, there is a need for a fast, reliable and efficient method of attaching discrete microwave components to the circuit board, whether these are simple two-lead devices such as resistors or diodes, or complex multi-lead microwave integrated circuits (MICs).

The methods used to achieve low resistance electrical connections and good mechanical integrity fall into two categories: true fusion welding where the metals of the package lead and the circuit land are melted together, and a form of diffusion where the joint is made without melting.

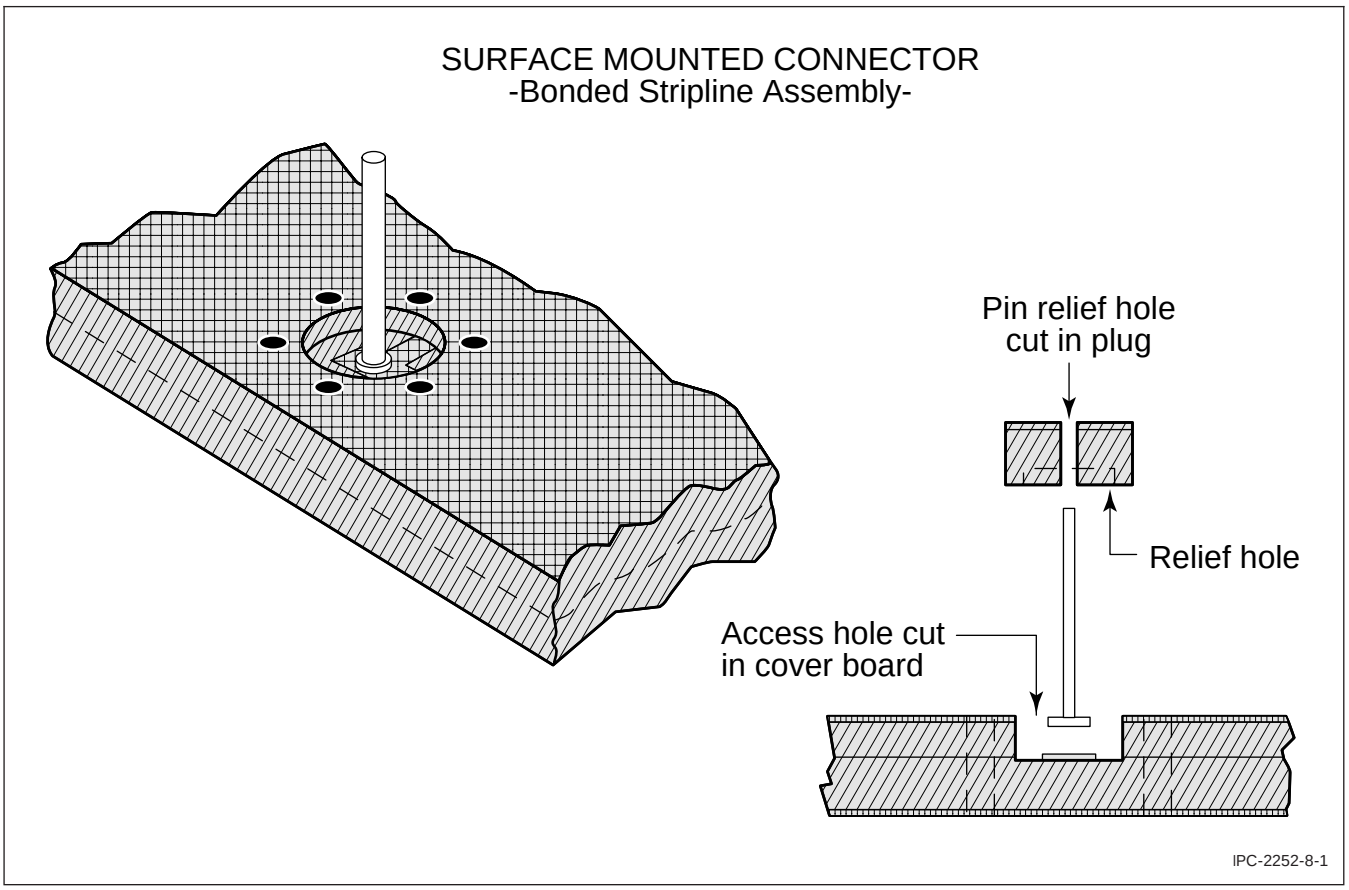

Figure 8-1 Mounting a Surface Connector to a Buried Land, Showing the Attachment of the Connector's Pin

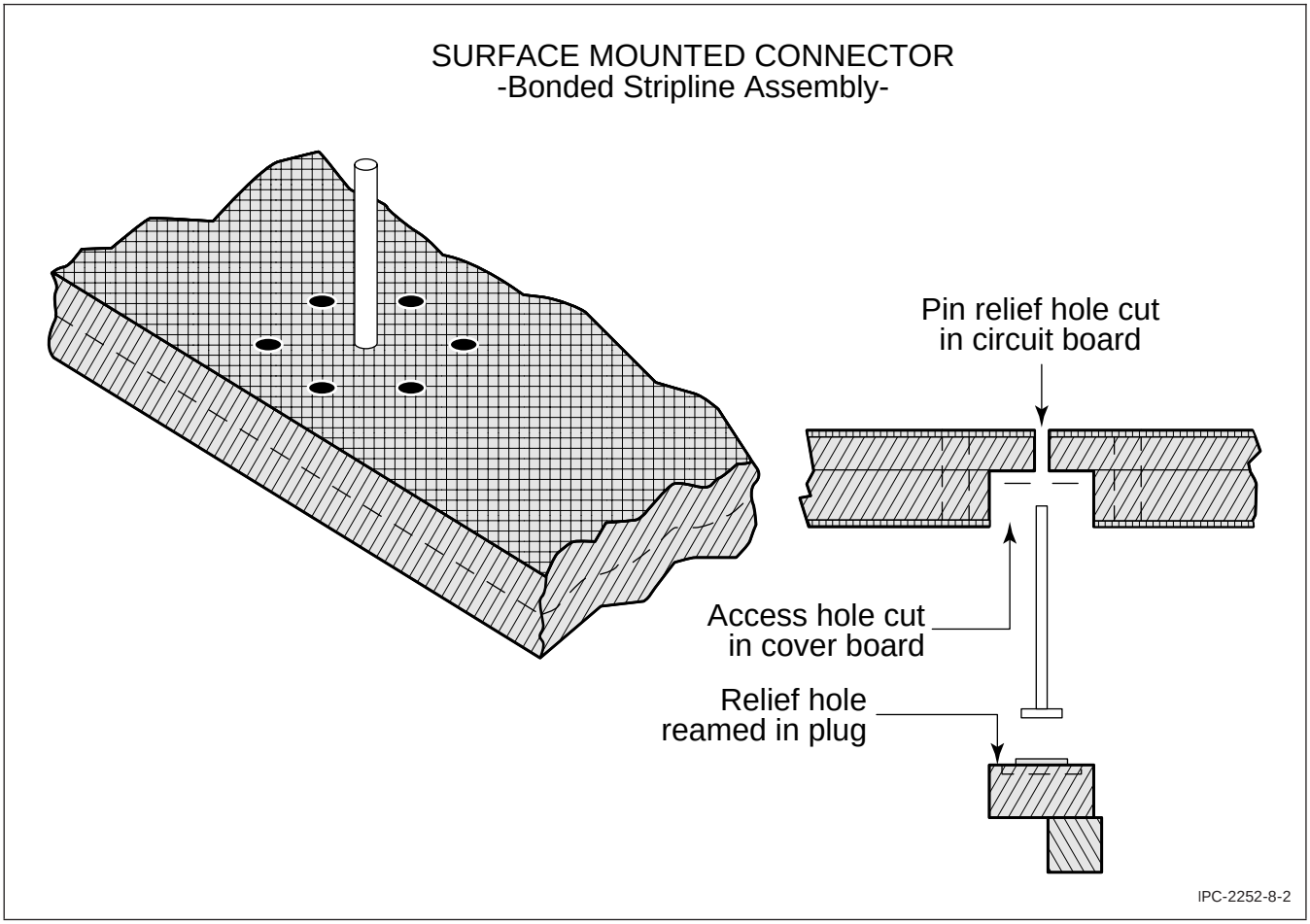

Figure 8-2 Alternative Mounting Method, Showing the Attachment of the Connector's Pin

8.3.1 Welded Bonds

8.3.1.1 Resistance Welding The package lead and circuit land are pressed together and a high current pulse (usually from a capacitor) is passed between them. Heat caused by the passage of the current through the resistance of the joint melts, and welds together, the package lead and the circuit land.

8.3.1.2 Parallel Gap Welding This is a specialized form of resistance welding. In this case the electrical energy is supplied to a pair of parallel electrodes which are in contact with the package lead. The weld depends upon conduction of heat that is generated in the package lead to the circuit land, which melts and welds together the package lead and the circuit land.

8.3.1.3 Percussive Arc Welding The package lead and circuit land are held a small distance apart forming a gap. An arc generated by applying a short pulse of RF energy ionizes the gas in the gap and is followed by a discharge from a capacitor that heats the surfaces of the two conductors. As the arc decays, a mechanical device forces the two heated surfaces together and completes the weld.

8.3.1.4 Laser Welding The package lead and circuit land are pressed together. Energy from a laser (which provides a source of intense, collimated, monochromatic light) is focused onto and is absorbed by the package lead and circuit land. The absorption of the laser energy raises the temperature of the package lead and circuit land to the fusion point, thus welding them together.

8.3.1.5 Soldering The package lead and circuit land are coated with a low melting point alloy and pressed together. Heat is applied either locally to the joint area (by a heating tool) or to the entire board (by infrared or oven heating) to melt the solder and weld the two components together. The effect of temperature on device attachment should be considered (see 8.1.4.1).

8.3.2 Diffusion Bonding

8.3.2.1 Ultrasonic Welding Diffusion of metal between the package lead and circuit land is induced by clamping the two together and applying mechanical energy in the form of ultrasonic sound vibration. The ultrasonic energy cleans and heats the metal surfaces by friction to provide the bond. Temperatures do not reach the melting point.

8.3.2.2 Thermal Compression Bonding Metal diffusion in this method is accomplished by heating and pressing together the cleaned surfaces of the package lead and circuit land. The temperature is insufficient to give a true fusion weld. The effect of temperature on device attachment should be considered (see 8.1.4.1).

8.3.2.3 Thermosonic Bonding This method is a combination of ultrasonic and thermal compression bonding. The work is preheated, and ultrasonic energy is supplied through a gold capillary. Again, the bond is achieved at temperatures below the fusion point of the metal. The effect of temperature on device attachment should be considered (see 8.1.4.1).

8.3.3 Device Attachment The methods most suitable for attaching devices to circuit boards are: ultrasonic wire bonding, thermosonic bonding, parallel gap welding, thermal compression bonding, and solder reflow.

8.3.3.1 Ultrasonic Wire Bonding This method relies on the ''scrubbing'' action of the bonding wire against the device lead or circuit board land to expose nascent metal surfaces and on deformation of the metal surface caused by pressure of the wire against the device lead or circuit land (which promotes diffusion of the metals). Aluminum wires, with their coating of abrasive oxide, are particularly effective in forming this type of diffusion bond. For example, cleaning of copper lands prior to bonding is not necessary because any oxide contamination of the land surface is rapidly removed by the motion of the wire.

8.3.3.2 Thermosonic (Ball) Bonding In this method, a gold capillary wire is agitated by an ultrasonic generator and pressed against the pre-heated device lead or circuit land. A ball of gold is formed at the protruding tip of the wire by a gas flame or electrical heater, and this ball forms the initial contact with the land. Plastic deformation of the gold ball caused by the contact pressure results in a ''nailhead'' shape typical of this type of wire bond.

8.3.3.3 Parallel Gap Welding Fusion welds are formed in this method by the resistive heating of gold foil or gold plated leads on the device. A short section of the device lead is pressed against the conductor land and then placed between two electrodes. A high current (typically 100 A) is passed between the electrodes to bond the device lead to the conductor land. Better control is achieved by confining the electrical contact to the device lead rather than passing current between the lead and the conductor. The amount of energy (which appears as heat) is determined by the magnitude and duration of the applied current.

8.3.3.4 Thermal Compression Bonding The device lead and the conductor land of the board are aligned and pressed together. Heat is supplied to the lead surface, and diffusion of the metal between the device lead and conductor land takes place, creating the bond. A modification of the parallel gap welder, in which the electrodes are replaced with a resistance-heated head, is the equipment normally used. Power input, duration and pressure control the quality of the bond. For laminates, pressure should not be greater than that required to ensure good thermal contact between the heating head, the device lead, and the conductor land.

Very clean surfaces are necessary to ensure proper diffusion of the metals. Gold tape or gold plated leads on the device, and gold or nickel/gold plating on the board lands are required for thermal compression bonds. The method is unsuitable for wire bonding because the device leads must be in the form of flat tapes. The flat tapes are necessary to provide sufficient contact area with the conductor lands for efficient heat transfer.

This method is not recommended. It requires a special selection of materials due to the high heat and pressure that are required.

8.3.3.5 Solder Reflow The solder reflow method requires that the device lead and the circuit land are first solder plated. The solder joint is then made by simply pressing the two components together and heating them sufficiently to melt or reflow the solder. The joint is allowed to cool until the solder refreezes. Minimal pressure, just enough to allow good thermal contact between the solder surfaces, is required. The effect of temperature on device attachment should be considered (see 8.1.4.1).

Soldering connections has the advantage of being usable in low volume and prototype production with reasonable efficiency, rework capability, and low capital investment. Equipment is now available that can perform reliable, repeatable solder connections in a largely automated fashion at low cost, thus facilitating the transition from the lab and prototype shop to the factory floor.

Tin/lead solders have been used in the printed circuit board industry for many years to make electrical connections between copper conductors and discrete components. More recently, low melting point indium based solders have been used in special applications where severe temperature constraints exist. For microwave circuit boards and laminates, soldered joints are probably most commonly used for component mounting.

9 QUALITY ASSURANCE

Quality assurance concepts should be considered in all aspects of microwave printed circuit board design. Quality assurance evaluations consist of the following:

a. Material inspection.

b. Qualification testing.

c. Quality conformance inspection.

d. Process control evaluations.

Quality assurance often requires the use of specific test procedures or evaluations to determine if a particular product meets the requirements of the customer or the specifications. The evaluations can be done using nondestructive tests, such as visual inspections, and/or destructive tests. The performance of RF/microwave circuits is sensitive to variations in the electrical properties of the printed wiring board, more so than are digital circuits.

Some quality evaluations are performed on test coupons instead of on the production printed wiring board because the test is destructive or the nature of the test requires a specific design that may not exist on the production board. These test coupons are fabricated on the same panel as the production board and, therefore, have been subject to the same processes as, and are representative of, the production board. However, the design and location of the test coupon on the panel is critical in order to assure that the coupons are truly representative of the production boards. An entire production board may also be used for destructive tests. Tests that require specific circuit configurations may also be performed on production boards if the appropriate circuitry is included in the design. Test coupon definition and location should be as defined in 9.1 unless otherwise defined on the master drawing.

Quality assurance evaluations and tests should meet the requirements of IPC-6018. Laminates used in the production of RF/microwave circuit boards should conform to the requirements specified in the IPC-4103 and be marked according to the designations given in the IPC-4103.

9.1 Quality Conformance Evaluations Quality conformance evaluations are performed on production boards and/or quality conformance test coupons. Coupon design, location, and frequency on production panels are defined in IPC-2221. Additional quality conformance test coupons may be added by the board fabricator. Traceability of quality conformance coupons should be identifiable to the specific production boards.

9.2 Reliability Unless otherwise specified, reliability inspection should consist of inspections specified in the drawing notes.

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