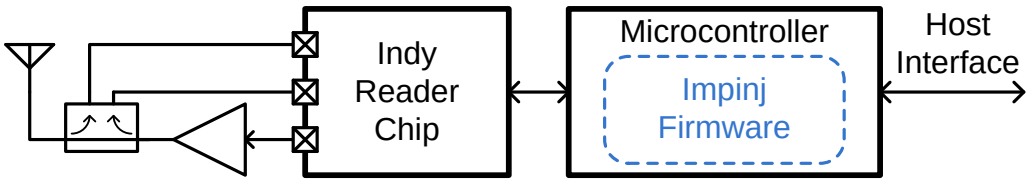
Indy® R2000 Reader Chip (IPJ-R2000)

Electrical, Mechanical, & Thermal Specification

Indy® R2000 Reader Chip Overview

Air Interface Protocol	EPCglobal UHF Class 1 Gen 2 / ISO 18000-63 (formerly 18000-6C) DSB, SSB, and PR-ASK transmit modulation modes Dense reader mode (DRM) ISO 18000-6B, Ipico, and iP-X version 1.07 not supported by Indy reference design
Transmit Output Power	Configurable up to 17 dBm. External power amplifier supported for high performance applications
Transmit Gain	Adjustable to > 25 dB
Modem	Configurable digital baseband
Operating Frequencies	860 – 960 MHz
Package	64-pin 9 mm x 9 mm x 0.85 mm sawn QFN
Power	Low power consumption, 1100 to 880 mW configuration dependent; 200µW standby
Process	0.18 µm SiGe BiCMOS
RSSI	Tag dependent, configurable bandwidth
RX Sensitivity	-110 dBm; -93 dBm (DRM); -84dBm (DRM) with +10dBm self-jammer
Supported Regions	All worldwide regions supported, including: US, Canada, and other regions following US FCC 47 CFG Ch. 1 Part 15 Europe and other regions following ETSI EN 302 208-1 (V1.4.1)

Figure 1-1. Indy R2000 System Block Diagram



For technical support, visit the Impinj support portal at support.impinj.com

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2 Introduction

The Impinj® Indy® R2000 UHF Gen 2 RFID reader chip is a highly integrated, high-performance, low power, SiGe BiCMOS device for EPC Gen2 / ISO18000-63 (formerly 18000-6C) applications. The Indy R2000 can also be programmed to support ISO18000-6B, iPico and iP-X protocols; however, the current reference design does not support these protocols. The Indy R2000 reader chip supports a zero intermediate frequency (ZIF) architecture in the worldwide UHF industrial, science, and medical (ISM) band. The Indy R2000 reader chip contains all of the RF and baseband blocks to interrogate and receive data from compatible RFID tags, specifically:

- Industry leading modem architecture uses modern digital signal processing which ensures high read reliability
- Exclusive Self-jammer Cancellation Technology ensures read reliability even with high antenna reflections
- Fully integrated voltage controlled oscillator (VCO) with world wide RFID coverage
- Integrated Power Amplifier (PA)
- High compression point quadrature downconverting mixer
- Integrated RF envelope detectors for forward and reverse power sense
- Integrated multipurpose Analog-to-Digital Converters (ADCs) and Digital-to-Analog Converters (DACs)
- Configurable digital baseband
- High speed synchronous serial bus or 4-bit parallel bus control

When used in the Indy R2000 Development Platform, which includes an example protocol processor and radio control implementation, the result is a fully functional UHF Gen 2 RFID reader with market leading performance.

2.1 Terminology

Table 1: Relevant Terminology

Term	Definition
ADC	Analog-to-Digital Converter
AGC	Automatic Gain Control
AM	Amplitude Modulation
ASK	Amplitude Shift Keying
AUX	Auxiliary
BPF	BandPass Filter
Class 0	Tags and readers conforming to MIT Auto-ID Center, Class 0 RFID Tag Protocol Specification
CORDIC	CO-ordinate Rotation DIgital Computer
CW	Continuous Wave
DAC	Digital-to-Analog Converter
DFT	Discrete Fourier Transform
DRM	Dense Reader Mode
DSB	Double Sideband
EOT	End of Transfer
EPC	Electronic Product Council
FCC	Federal Communications Commission (US Regulatory Body)
FIFO	First In, First Out

FIR	Finite Impulse Response
I	In-phase
IF	Intermediate Frequency
IIR	Infinite Impulse Response
I-Q	In-phase Quadrature
ISM	Industrial, Science, and Medical
ISO	International Standards Organization
ISO18000	Tags and Readers conforming to ISO/IEC FDIS 18000-6:2003(E)
LBT	Listen Before Talk
LFSR	Linear Feedback Shift Registers
LNA	Low Noise Amplifier
LO	Local Oscillator
LUT	Lookup Table
MSB	Most Significant Bit
MSps	Mega Samples per second
NCO	Numerically Controlled Oscillator
PA	Power Amplifier
PER	Packet Error Rate
PLL	Phase Locked Loop
PR	Phase Reversal
Q	Quadrature-phase
RF	Radio Frequency
RFID	Radio Frequency Identification
RSSI	Received Signal Strength Indicator
RX	Receiver
SJ	Self Jammer — also known as Tx carrier present at the Rx, typically from antenna reflection
SJC	Self Jammer Cancellation — circuitry that removes SJ from Rx port
SSB	Single Sideband
TBD	To Be Determined
TX	Transmitter
TCXO	Temperature Compensated Crystal Oscillator
UHF	Ultra High Frequency
VCO	Voltage Controlled Oscillator

2.2 Reference Documents

The Indy R2000 reader chip is fully compliant with the protocol specifications provided in Table 2, as well as with the local regulations referenced in Table 3.

Table 2: Protocol Specification Documents

Document
iPico, iP-X: Universal RFID protocol standard V1.07 July 2005
ISO/IEC FDIS 18000-6B Sept. 2004
ISO/IEC FDIS 18000-63 Jan. 2005

Table 3: Local Regulation Documents

Document
FCC 47 CFR Ch. 1, part 15
ETSI EN 302 208-1 V1.4.1

Table 4 lists supplemental information sources for the Indy R2000 reader chip. These can all be found in the R2000 Development Kit files, which are available on support.impinj.com here.

Table 4: Supplemental Documents

Document
Indy Development Platform Operation
Indy Firmware Datasheet
Indy Host Library API Reference Manual
Indy Host Interface Packet Definitions
Indy OEM Configuration
Indy Host Library SDK Getting Started Guide
Indy MAC Command Definitions
Indy MAC Register Set Definitions

2.3 About This Document

This document constitutes the electrical, mechanical, and thermal specifications for the Indy R2000 reader chip. It contains a functional overview, mechanical data, package signal locations, and targeted electrical specifications.

2.4 Indy R2000 Reader Chip Diagrams

Figure 2-1 provides a top level block diagram of the RF/analog parts of the Indy R2000 reader chip. The architecture is based on direct conversion for both the transmitter and receiver.

Figure 2-2 shows the R2000 sheet of the schematic for the R2000 Development Kit. Additional components such as the host microprocessor, PA, filters, etc. are contained in other sheets. This is shown as a representative example of how to integrate the R2000 into a design. For more details, see the kit documentation on support.impinj.com here.

Figure 2-1: Indy R2000 Reader Chip Top Level RF Block Diagram

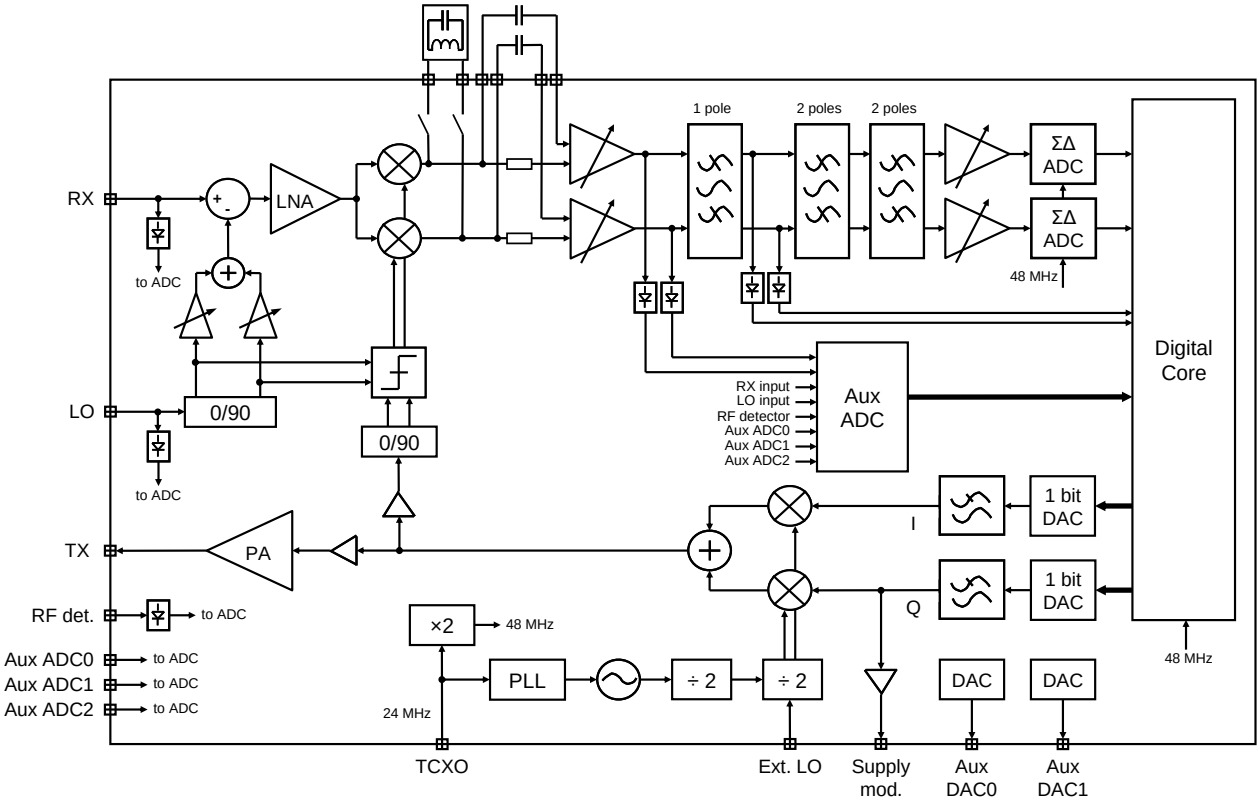
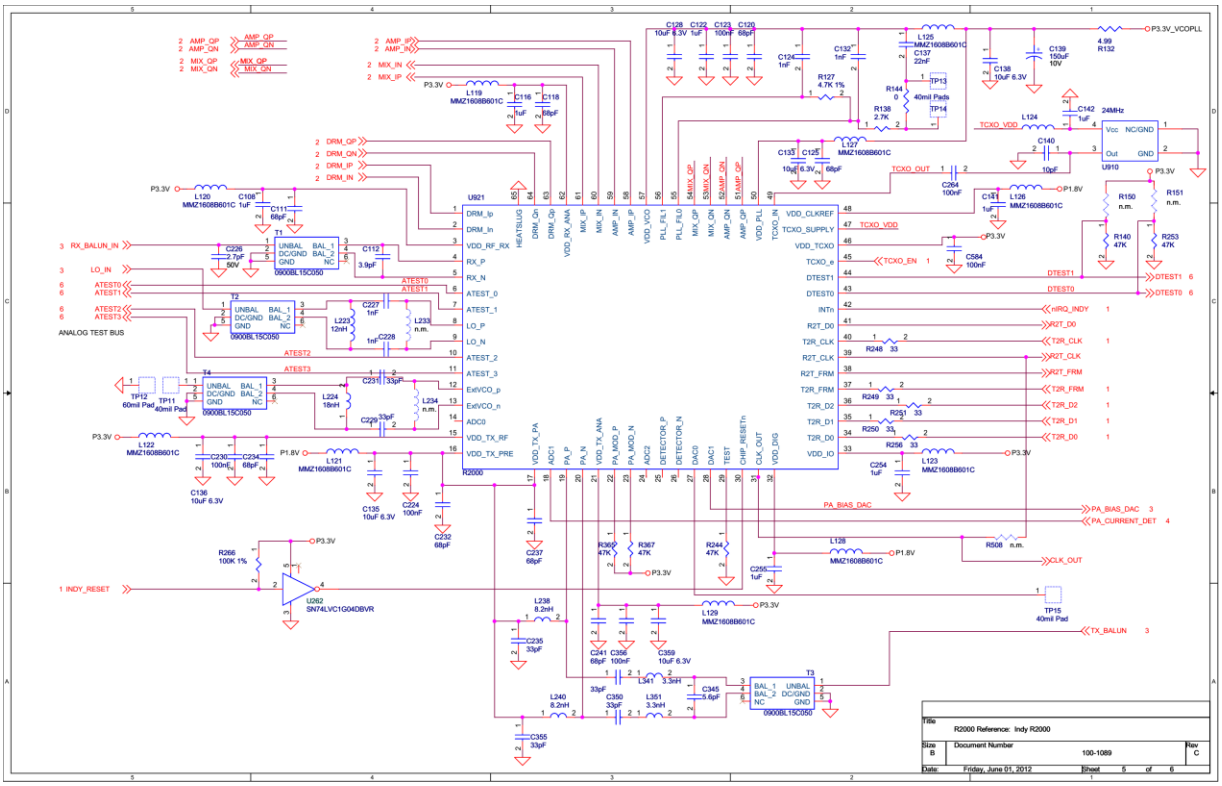


Figure 2-2: Indy R2000 Reader Chip Schematic Page in R2000 Development Kit



3 Pin Listing and Signal Definitions

The R2000 QFN package has 64 pins and one exposed ground paddle (e-pad). They are listed in Table 5.

Table 5: Pin Listing and Signal Definitions

Pin #	Pin Name	Type	Description
1	DRM_Ip	Analog Out	Mixer external DRM load, In-Phase (I)
2	DRM_In		
3	Vdd_rx_rf	Power	3.3 V supply for receive RF
4	RX_p	RF In	Differential receive RF Input
5	RX_n		
6	Atest0	Analog	Analog Test Bus
7	Atest1		
8	LO_p	RF In	Differential RF input from a high impedance tap on transmit path
9	LO_n		
10	Atest2	Analog	Analog Test Bus
11	Atest3		
12	ExtVCO_p	RF In	Differential external VCO input
13	ExtVCO_n		
14	ADC0	Analog In	Voltage input to AUX ADC
15	Vdd_tx_RF	Power	3.3 V supply for transmit RF, except for power amplifier
16	Vdd_tx_pre	Power	1.8 V supply for power amplifier pre-driver
17	Vdd_tx_pa	Power	1.8 V supply for power amplifier
18	ADC1	Analog In	Voltage input to AUX ADC
19	PA_p	RF Out	Transmit output for all modes
20	PA_n		
21	Vdd_tx_ana	Power	3.3V supply for transmit analog
22	PA_modp	Analog out	Differential output voltage of PA modulator DAC to apply amplitude modulation to the PA
23	PA_modn		
24	ADC2	Analog In	Voltage input to AUX ADC
25	Detector_p	RF In	Differential peak detector input
26	Detector_n		
27	DAC0	Analog Out	Output of AUX DAC
28	DAC1	Analog Out	Output of AUX DAC
29	TEST PIN	DNU	Reserved for Impinj usage. Tie to logic low.
30	CHIP_RESETn	Digital In	Chip reset, logic low.
31	CLK_out	DNU	Test pin. Leave floating.
32	Vdd_dig	Power	1.8 V supply for digital circuitry
33	Vdd_io	Power	3.3V supply for IOs

Pin #	Pin Name	Type	Description
34	DA0	Digital Bi	Bidirectional data interface
35	DA1		
36	DA2		
37	DA3		
38	ALE	Digital In	Address Latch Enable
39	CSn	Digital In	Chip select, active low
30	RDn	Digital Bi	Read strobe, active low
41	WRn	Digital In	Write strobe, active low
42	IRQn	Digital Bi	Interrupt, active low
43	Dtest0	Digital Bi	Digital test bus
44	Dtest1	Digital Bi	Digital test bus
45	TCXO_e	Digital In	TCXO supply switch enable, active high
46	Vdd_TCXO	Power	3.3 V supply input for TCXO supply switch
47	TCXO_supply	Output	3.3 V output from TCXO supply switch
48	Vdd_clkref	Power	1.8 V supply for clock reference input buffer
49	TCXO	Clock In	Reference clock from a 24 MHz AC coupled input
50	Vdd_pll	Power	3.3 V supply for phase locked loop
51	Amp_Qp	Analog In	Q post-mixer amplifier input
52	Amp_Qn		
53	Mix_Qn	Analog Out	Q Mixer output
54	Mix_Qp		
55	PLL_fil0	Analog	Nodes for external PLL filter
56	PLL_fil1		
57	Vdd_vco	Power	3.3 V supply for voltage controlled oscillator (VCO)
58	Amp_Ip	Analog In	I post-mixer amplifier input
59	Amp_In		
60	Mix_In	Analog Out	I Mixer output
61	Mix_Ip		
62	Vdd_rx_ana	Power	3.3V supply for receive analog
63	DRM_Qp	Analog Out	Mixer external DRM load, Q
64	DRM_Qn		
Paddle	GND	GND	Single Chip Ground

4 Electrical Specifications

4.1 Absolute Maximum Ratings

The absolute maximum ratings in Table 6 define limitations for electrical and thermal stresses. These limits prevent permanent damage to the Indy R2000 reader chip.

Caution: Operation outside these maximum ratings might result in permanent damage to the device.

Table 6: Absolute Maximum Ratings

Parameter	Conditions	Min.	Max.	Unit
Digital core supply voltage	Vdd_dig	-0.5	2.1	V
Digital I/O supply voltage	Vdd_io	-0.5	3.6	V
Analog PA supply voltage	Vdd_tx_pa/Vdd_tx_pre	-0.5	2.1	V
Analog clock ref supply voltage	Vdd_clkref	-0.5	2.1	V
Analog supply voltage	Vdd_pll, Vdd_rx_ana, Vdd_tx_ana, Vdd_tx_rf	-0.5	3.6	V
Analog VCO supply voltage	Vdd_vco	-0.5	3.6	V
Analog RF RX supply voltage	Vdd_rx_rf	-0.5	3.6	V
Maximum voltage on non-supply pins	Outputs Inputs	-0.5 -1.0	3.6 3.6	V V
RF input power	TX ports RF and IF ports	-	+23 +15	dBm (VSWR 2.1:1)
Storage temperature		-45	+125	ºC
Package MSL	Moisture sensitivity level 3			

4.2 Operating Conditions

This section describes operating voltage, frequency, and temperature specifications for the Indy R2000 reader chip. Table 7 provides the supported operating conditions:

Table 7: Operating Conditions

Parameter	Min.	Typ.	Max.	Unit	Conditions
Digital core supply voltage	1.7	1.8	1.9	V	Vdd_dig
Digital I/O supply voltage	3.135	3.3	3.465	V	Vdd_io
Analog PA supply voltage	1.7	1.8	1.9	V	Vdd_tx_pa/Vdd_tx_pre
Analog clock ref supply voltage	1.7	1.8	1.9	V	Vdd_clkref
Analog supply voltage	3.135	3.3	3.465	V	Vdd_pll, Vdd_rx_ana, Vdd_tx_ana, Vdd_tx_rf
Analog VCO supply voltage	3.135	3.3	3.465	V	Vdd_vco
Analog RF RX supply voltage	3.135	3.3	3.465	V	Vdd_rx_rf
Operating ambient temperature	-20	-	+85	ºC	Case temperature

4.3 Transceiver Functional Specifications

Table 8 provides power consumption specifications for the reader chip, and Table 9 provides receiver specifications with respect to voltage rails.

Table 8: Power Consumption Specifications in Mission Mode (Reading Tags) and Reset

Parameter	Min.	Typ.	Max.	Unit	Conditions
Power consumption while performing inventory, SJC off		1100		mW	at 17.5 dBm
		1000		mW	at 12 dBm
		875		mW	at 1.4 dBm
Power consumption while performing inventory, SJC on		1600		mW	at 17.5 dBm
		1500		mW	at 12 dBm
		1375		mW	at 1.4 dBm
Power consumption in reset		0.2		mW	

Note. Power consumption data is based on a combination of measurements taken on a small sample size using an engineering test fixture, and simulations of the chip.

Table 9: Indy R2000 Reader Chip — Receiver Specifications

Parameter	Min.	Typ.	Max.	Unit	Conditions
Input frequency	860		960	MHz	
Differential input impedance		50		Ω	Frequency = 900 MHz Note Recommended Balun in App Note
Differential input match		9		dB	S11
IIP2		+50		dBm	
IP1dB	-2		+6	dBm	RF high/low gain settings
LO leakage		-60		dB	At RF input
IF bandwidth		10		MHz	
Chip Sensitivity (1% PER)		-93		dBm	(ISO 18000-63 1% PER, FM0 40kbps)
		-79		dBm	(ISO 18000-63 1% PER, FM0 40kbps, +15dBm carrier)
		-93.5		dBm	(ISO 18000-63 1% PER, M4 62.5kbps)
		-80		dBm	(ISO 18000-63 1% PER, M4 62.5kbps, +15dBm carrier)
		-77		dBm	(ISO 18000-6B 1% PER, 40kbps)
Maximum carrier incident at RX port		+10		dBm	Gain: RF-LNA 7dB, IF-LNA 24dB.
Self-jammer Suppression		20		dB	+10 dBm self-jammer at RX port +10 dBm LO signal at chip interface
Maximum Interferer		+2		dBm	
In-channel RSSI dynamic range in high gain		-45 -120		dBm dBm	Maximum level Minimum level
RSSI register size		14		Bits	
Co-channel selectivity		-			Dependent on off-chip filter

Adjacent channel selectivity		-			Dependent on external adjacent channel filter
LO input power	-20	10	12	dBm	SJ cancellation limited to this level
Subsystem noise figure with +10 dBm self-jammer		25 41		dBm dBm	Gain: RF-LNA 7dB, IF-LNA 24dB. Gain: RF-LNA 1dB, IF-LNA 6dB.
Subsystem noise figure without self-jammer		18		dBm	Gain: RF-LNA 13dB, IF-LNA 24dB
LO input impedance		50		Ω	Frequency = 900 MHz

Table 10: Front-End Mixer Gain and IP1dB

RF LNA gain	1 dB		7 dB		13 dB	
	Gain [dB]	IP1dB [dBm]	Gain [dB]	IP1dB [dBm]	Gain [dB]	IP1dB [dBm]
w/o SJ, SJC disabled, external LO= +4dBm						
External LO, +4 dBm	-1.6	+6	4.4	+3	10.3	-2
Internal LO	-1	+4	5	+3	10.8	-2
External LO, high compression	-1	+9	5	+4		
Internal LO, high compression	-0.4	+8	5.6	+3		
SJC disabled, external LO= +12 dBm, I^2+Q^2						
SJ= +2 dBm		+10				
SJ= +2 dBm high compression		+10				
SJC enabled, external LO= +12 dBm, I^2+Q^2						
SJ= +10 dBm		+7		+6		
SJ= +10 dBm high compression		+10		+5		

*High compression is selected with register h450-8

Table 11: Indy R2000 Reader Chip — Transmitter Specifications

Parameter	Min.	Typ.	Max.	Unit	Conditions
TX differential load impedance		50		Ω	Frequency = 900 MHz Output port of the Balun
TX output power		+19 +19 +11	+20 +20 +17	dBm dBm dBm	Linear, P1dB Non Linear, Modulated 0% AM Non-linear Full Power
Linear mode OIP3		+29		dBm	
TX output power temperature variation		2.5		dB	CW with closed loop power control across -20 to 85 ºC
TX output power absolute tolerance		0.5		dB	With closed loop power control
TX output power range		30		dB	Linear mode (Analog Resolution)
TX output power step size		0.5		dB	Linear mode (Analog Range)
AM control signal to external PA		0.7		Vp	

Table 12: Indy R2000 Reader Chip External LO Input

Parameter	Min.	Typ.	Max.	Unit	Conditions
Input impedance		50		Ω	
Input frequency	860		960	MHz	
Input power level	-20	10	12	dBm	With SJC
Supply voltage		3.3		V	Vdd_tx_rf

Table 13: Indy R2000 Reader Chip Envelope Detectors

Parameter	Min.	Typ.	Max.	Unit	Conditions
Forward power detection	-10		+13	dBm	At LO input
Reverse power detection	-10		+13	dBm	At detector input
Wideband listen before talk	-10		+13	dBm	At RX input

Table 14: Indy R2000 Reader Chip Synthesizer

Parameter	Min.	Typ.	Max.	Unit	Conditions
Frequency Range	860		960	MHz	
Frequency Grid		25 100 250 125		kHz kHz kHz kHz	Europe (ETSI 300 220) Europe (ETSI 302 208) US (FCC) China
Reference Input Frequency		24		MHz	TCXO Specification
Reference Frequency Tolerance			10	ppm	TCXO Specification
Reference Input Level		0.8		Vp	
Reference Duty Cycle	40		60	%	
PLL settling time within 1% of frequency step		140	470	µs	100 KHz grid, recommended PLL loop filter configuration
TX Phase Noise		-124		dBc/Hz	Δf = 250 kHz
Broadband Noise		-144		dBc/Hz	Δf = 3.6MHz
TX In-band spurious emissions		-69		dBc	RBW = 3 kHz, average detector
TX Out-of-band spurious emissions measured with balun		-54 -42		dBm dBm	Below 1 GHz (ETSI) RBW = 120 kHz, peak detector Above 960 MHz (FCC) RBW = 1 MHz, average detector
RX Spurious emissions		 -57 -47		 dBm dBm	Measured with balun (and BPF) 30 MHz to 1 GHz 1 to 12.75 GHz

Table 15: Indy R2000 Reader Chip Clock Output, DACs, and ADCs

Parameter	Min.	Typ.	Max.	Unit	Conditions
Maximum load capacitance on CLK_out		10 10 10 10 10		pF pF pF pF pF	Output clock rate: 48 MHz 24 MHz 12 MHz 6 MHz 3 MHz
Antenna input detection range	0.3		2.7	V	
Antenna input detection resolution		8		bits	
Temperature sensor range	0.3		2.7	V	
Temperature sensor resolution		8		bits	
PA bias output range	0.3		2.7	V	
PA bias resolution		8		bits	SD DAC implementation
PA regulator ctrl output range	0.3		2.7	V	
PA regulator ctrl resolution		8		bits	SD DAC implementation

Table 16: Indy R2000 Reader Chip Digital Interface

Parameter	Min.	Typ.	Max.	Units	Conditions
Input high voltage	1.5		Vdd	V	
Input low voltage	0		0.9	V	
Output high voltage	2.3		Vdd	V	
Output low voltage	0		0.7	V	
Input leakage current	-10		10	µA	
Input pin capacitance			10	pF	

5 Functional Description

The transmitter supports both in-phase quadrature (IQ) vector modulation and polar modulation. The direct IQ up-conversion is intended for single sideband amplitude shift keying (SSB-ASK) and phase reversal amplitude shift keying (PR-ASK). The polar modulation is intended for double sideband amplitude shift keying (DSB-ASK). In both cases, the signals are generated in the digital domain and converted to analog signals by sigma-delta digital-to-analog converters (DACs) followed by reconstruction filters. The integrated power amplifier can be operated in three different modes:

- Class F with high output power and without internal amplitude modulation (AM)

The integrated power amplifier acts as a driver for an external power amplifier. The external power amplifier performs the amplitude modulation, but it does require an external modulator. This is likely to be done with DSB and not PR-ASK.

Class F with drain modulation using an external modulator

- Class A required for SSB-ASK and PR-ASK

An optional linear external power amplifier can be used to increase the output power to the maximum allowed level.

The Indy R2000 reader chip performs the baseband encoding and pulse-shaping via a lookup table to minimize latency. In the case of SSB-ASK transmission, a Hilbert filter shapes the baseband signal to create a complex IQ

signal with suppressed negative frequencies. The signal is then offset in frequency to center the SSB-ASK spectrum in the channel. Sigma-delta DACs convert the digital I and Q signals into the analog domain.

In DSB-ASK transmission, the Indy R2000 reader chip performs the baseband encoding and pulse shaping in the same manner as for SSB-ASK, but pre-distorts the shaped signal to compensate for non-linearity in the amplitude modulation transfer function. Sigma-delta DACs convert the pre-distorted, amplitude-modulated control signal into the analog domain using lookup tables.

The receiver is in principle a homodyne to ensure that as much as possible of the transmitter leakage falls on DC. You can either drive the receiver down-conversion mixer using the internal local oscillator (LO) signal, or by an external local oscillator signal, typically tapped off from the output of the external power amplifier. The receiver uses a single on-chip, low noise amplifier (LNA). If the system must accommodate a >+10 dBm jammer, an external attenuator is required to reduce the incident power to +10 dBm.

After down conversion, resettable AC-coupling capacitors remove the majority of the DC signal. The analog intermediate frequency (IF) filter provides coarse channel selectivity. It has programmable bandwidth to accommodate the large range of required data rates. The coarsely filtered I and Q signals are analog-to-digital converted. Automatic intermediate frequency gain stepping in the filter reduces the required dynamic range of the analog-to-digital converter (ADC). Sharp and well-controlled digital filtering supplements the coarse analog filtering. Digital logic also performs the demodulation.

The reader chip logic derives the clocks for the digital blocks from a 24 MHz reference frequency signal originating from an external temperature-compensated crystal oscillator (TCXO). The sigma-delta DACs run directly off the 24 MHz signal. The sigma-delta ADCs run off a 48 MHz clock generated by an integrated frequency doubler.

The Indy R2000 includes a fully integrated voltage-controlled oscillator (VCO). The loop filter is external so that the synthesizer meets the stringent phase noise requirements and allows flexibility. The reader chip logic derives the time reference required by the phase locked loop and the digital blocks from the 24-MHz reference frequency.

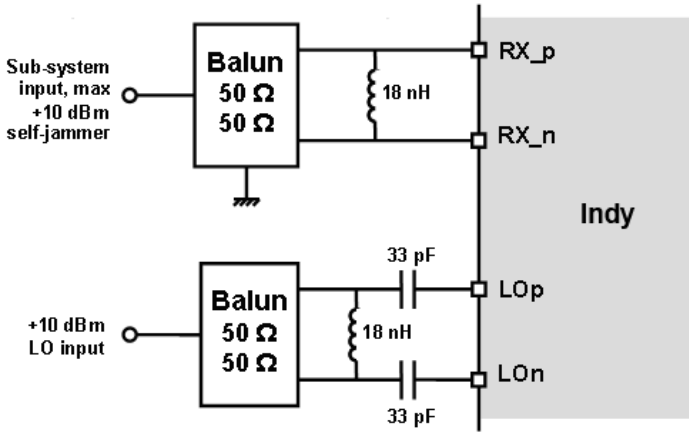
The Indy R2000 reader chip supports two interfaces—one low speed parallel interface with a data rate of up to 20 Mbps and one serial interface with data rates of 150 Mbps to (downstream), and up to 450 Mbps from (upstream) the Indy R2000 reader chip. The interfaces are multiplexed on the same pins, and the interface is determined during power-up. Both interfaces operate at 3.3 V. The Indy R2000 executes one low level instruction at a time from those written into a first in, first out buffer. All information is transferred via the register bank, and state machines control the reader chip.

5.1 Analog Receiver Data Path

5.1.1 Receiver Front-end Circuitry

The RF low noise amplifier and mixer can handle a +10 dBm self-jammer when the self-jammer cancellation is active. For the reader chip sub-system to accommodate a >+10 dBm self-jammer, you must add an external pad. The combined pad and balun losses should amount to the difference between the self-jammer power and 10 dBm. The local oscillator input must be +10 dBm in order for the self-jammer cancellation circuitry to have the ability to cancel the received +10 dBm self-jammer.

Figure 4-1: Receiver Front-end External Input Interface



5.1.2 Local Oscillator Input

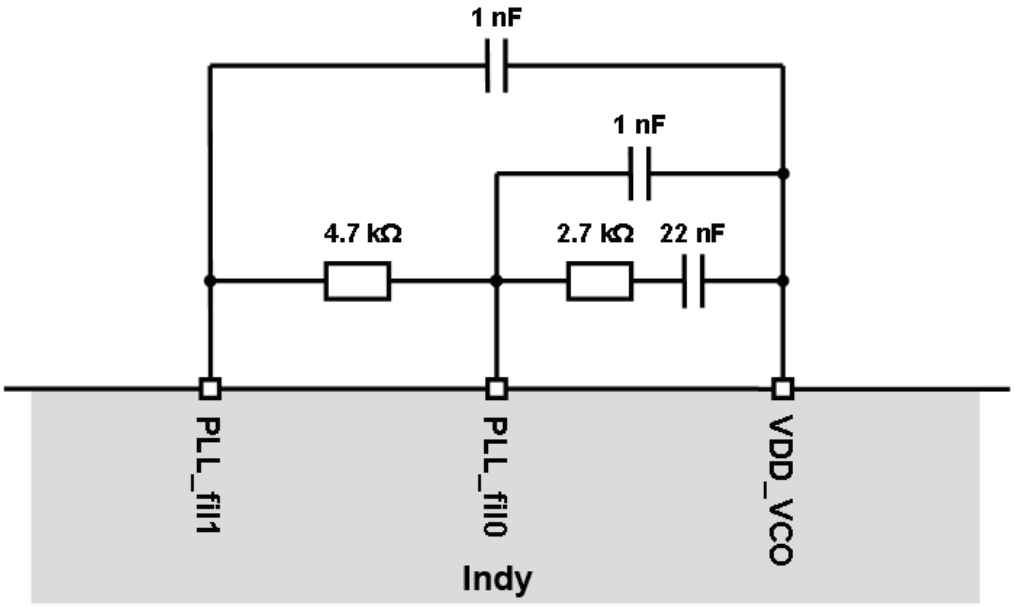
You may source the receiver local oscillator internally or externally as shown in Figure 4-1. If you do not use an external receiver local oscillator, the DC blocking capacitors, inductor, and balun are not required.

For proper self-jammer cancellation, the local oscillator input power level must exceed the maximum self-jammer level that requires cancellation. For more detail see section 5.3.

5.1.3 PLL Loop Filter

Figure 4-2 illustrates the recommended component values for the PLL loop filter.

Figure 4-2: PLL Loop Filter



5.1.4 Receive RF Interface

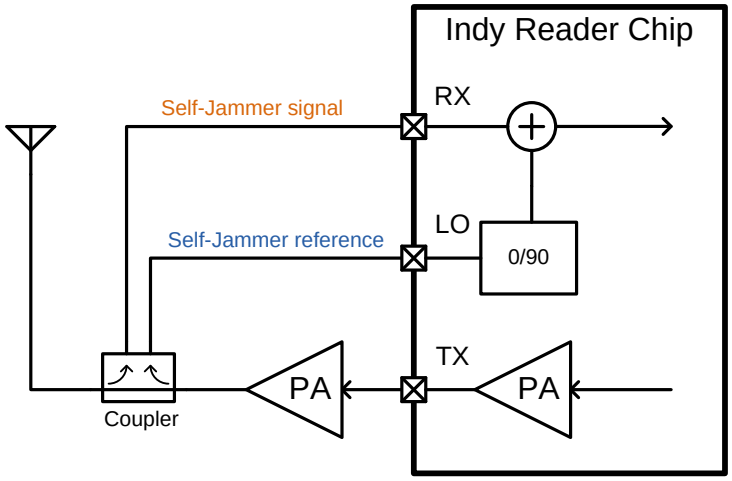
The Indy R2000 reader chip has differential RF and local oscillator ports to alleviate interference on the package bond-wires coming from the digital section of the chip.

The Indy R2000 receiver mixer also supports a high gain and a low gain mode with differing compression points. In order to switch between these modes, it is necessary to both correctly program the ANA_CTRL1 register as well as bias the output of the mixer to +3.3 V through 400 ohm resistors. You may switch these bias resistors in for low gain mode and out for high gain mode. Ensure that when switched out, the bias resistors do not create an unintended current summing node.

5.1.5 Self-Jammer Cancellation Block

The idea behind self-jammer cancellation is to tap a signal from somewhere along the transmit path and use it as a reference for suppressing the corresponding part of the received signal in the RF low noise amplifier. By doing so, both the self-jammer carrier and transmit amplitude and phase noise are simultaneously suppressed. By tapping the reference transmit signal after the external power amplifier, all transmit noise sources may be managed. As shown in the block diagram in Figure 4-3, the reference signal is shared with the receive mixer local oscillator input.

Figure 4-3: Self-Jammer Cancellation Architecture

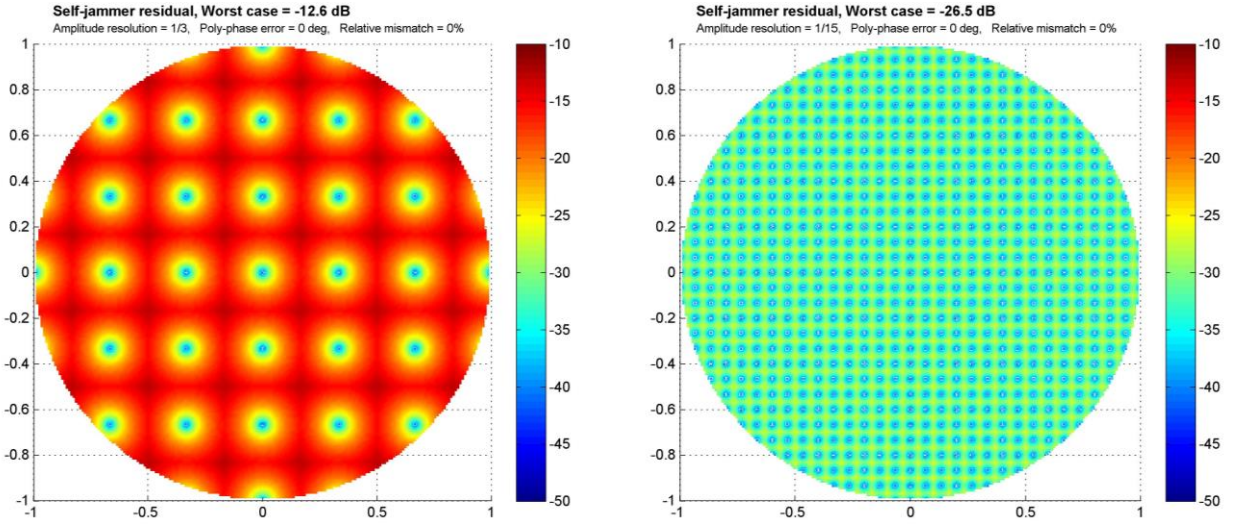


Ensure that the power level of the reference signal is equal to the largest self-jammer power level that you intend to cancel. From the real RF reference signal, a new complex reference signal is created using a very low noise, passive, 90-degree poly-phase filter. The output of the filter consists of four signals: +I, -I, +Q, and –Q. By adjusting the I and Q scaling, it is possible to let the cancellation signal achieve the same amplitude as the received self-jammer, but with a 180 degree phase shift.

In principle, the cancellation signal has the same amplitude and phase noise as the self-jammer. If the time delay between the reference transmit signal and the received self-jammer is small, it is possible to cancel not only the self-jammer carrier but also its noise by adding the cancellation signal to the received signal. The RF low noise amplifier performs this cancellation by adding currents. The noise added by all the blocks in the self-jammer cancellation path must be smaller than the targeted self-jammer noise after cancellation. For noise minimization purposes, capacitive coupling scales the reference signal. Switched binary weight capacitors determine the amount of capacitive coupling. This method has the side effect that the scaling of the reference signal becomes quantized in amplitude.

Figure 4-4 shows the ratio between the output and input for all possible signals. The circular areas illustrate complex constellation diagrams representing all possible signals relative to the full scale reference signal. The color shows the theoretical output after self-jammer cancellation relative to full scale for all possible self-jammer signals. When the received self-jammer has a phase and amplitude that matches one of the possible cancellation signals, the suppression is very good (shown in blue). When the received self-jammer falls between possible cancellation signals, the suppression is not as good (shown in red). With two bits per axis (i.e., four levels per axis ranging from zero to full scale), the worst case suppression is almost 13 dB. With four bits per axis, the worst case suppression is theoretically more than 26 dB. Indy R2000 implements four bits per axis, because with 26 dB suppression, other factors will start to dominate the actual noise suppression.

Figure 4-4: Theoretical Output After Self-jammer Cancellation Relative to Full Scale.



Minimizing the I and Q scaling factors optimizes the DC of the received signal. The normal receiver data path will be used and the control block taps the DC information after the digital channel filter. In order to maintain the DC information through the data path, the external AC-coupling capacitors must be temporarily bypassed. When the AC-coupling is bypassed, a 50 kΩ resistor is added at the intermediate frequency low noise amplifier (IF-LNA) input to improve the differential and common mode voltage handling of the IF-LNA. The external LC mixer is also disconnected in SJC calibration mode. The Indy R2000 state machine handles the disconnection of the AC coupling and the mixer load and the connection of the resistor at the IF-LNA input for SJC.

One complication of controlling the cancellation is that the relative orientation of the coordinate systems is not accurately known. If, for instance, the scaling of the +I signal is changed, this could result in a DC change in both the receiver I and Q signals. Another complication that must be handled by the calibration algorithm is that for strong self-jammer levels, the receiver will compress unless the cancellation provides at least 10 dB of self-jammer suppression. The calibration procedure can be split into three different modes (see also Figure 4-5):

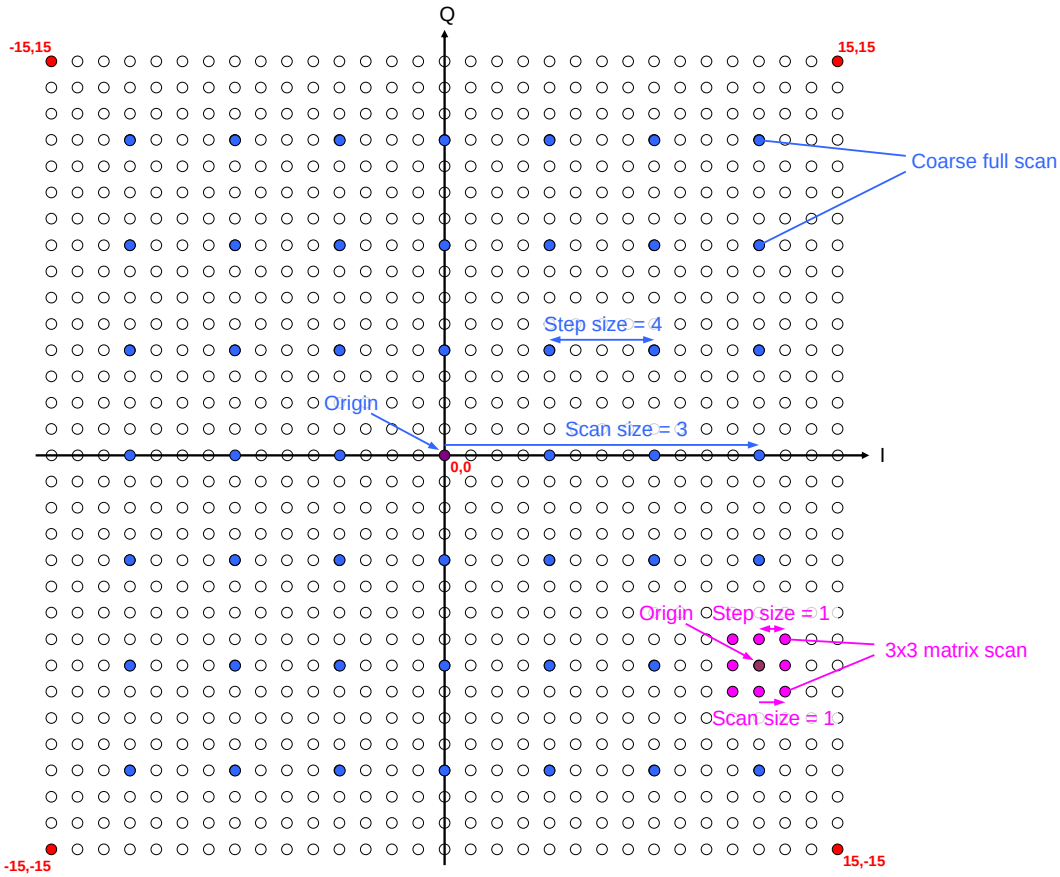
- Hold mode: current I and Q scaling values are held.
- Full scan mode: a coarse grid of settings are evaluated.
- Matrix scan mode: evaluate all 3x3 settings centered on the current setting.

The actual implementation is coded in a generic fashion so that the full scan mode and the matrix scan mode simply are two configurations of one general mode.

Because the DC signal caused by the self-jammer corresponds to a strong signal even after successful cancellation, it is important that the receiver data path gain is set low. Therefore all the receiver gain settings have been collected into two registers. During normal receiver operation, the gain settings are taken from ANA_RX_GAIN_NORM (register 0x450). During self-jammer cancellation scan, the gain is instead temporarily defined by ANA_RX_GAIN_SJC (register 0x451), if the “reduce gain” bit is set (register 0x152).

The optimum SJC setting is found by minimizing the magnitude of the complex signal after the digital filter selection multiplexer. In this way, the signal can either be filtered with the FIR or IIR channel filter, or not filtered at all by the channel filter. This approach means that the time delay from when a setting is changed until the result can be observed varies. To handle this variation, the settling time is programmable. The settling time is defined as the time the controller waits after a change of the settings until the magnitude measurement is started. The measurement time is also programmable to support tradeoff of measurement speed against accuracy. Both the settling time and measurement time are set by register 0x150.

Figure 4-5: Self-jammer Cancellation Grid and Calibration Examples



The scan type is defined by the origin, the scan size, and the scan step as described in Figure 4-5. For a full scan, the origin (register 0x151) is typically set to zero, the scan size to three, and step size to four (register 0x152). When the scan is triggered, the control block evaluates the self-jammer suppression for all the points corresponding to the blue settings. The value of the best setting is returned in register 0x154. To perform a 3x3 matrix scan around the previous best setting, the scan and step sizes are both set to one and the scan retriggered with the “Use current settings as origin” flag set. The configuration of the scans determines the calibration time. If the data path sample rate is 3 MSps and the digital filter is bypassed during SJC calibration, suitable settling and measurement durations are 16 and 8 samples, respectively. These sampling durations correspond to 5.3 and 2.6 µs. Performing a coarse full scan requires a total of 49 measurements, and take 392 µs. A single 3x3 matrix scan will take 72 µs. To ensure optimal settings, repeat the matrix scan a few times. Ideally, you should repeat the 3x3 matrix scan periodically to allow the system to track.

5.1.6 Receive Baseband Interface

The Indy R2000 uses an AC coupling interface between the mixer and the baseband low noise amplifier. This interface provides a high-pass filtering response to notch out the DC offset generated by the self-jamming signal from the transmitter.

An example schematic is shown in Figure 4-6. The R2000 reference design has higher order external DRM filters.

The design of the baseband interface meets the following requirements:

- The high-pass filtering corner must be low enough to prevent attenuating the received signal. Although the tag response modulation does not consist of any DC content, the low data rate modes can have significant signal content very close to DC.
- The high-pass filtering corner must be high enough so that the DC changes can converge quickly. There is a change of DC content going from modulated data transmission (interrogator transmit) to continuous wave (CW) transmission (interrogator receive). The DC changes must converge before the receive demodulator

can demodulate correctly. The DC level change occurs during transition from transmit to receive. Varying the time constant of the high-pass filtering or sample and holding the DC offset is allowed, provided the air interface protocol is not violated.

- The AC coupling capacitor and the bias resistance must form a low-pass filter for the bias thermal noise, provided the total integrated noise is a constant equal to KT/C. To reduce the input referred noise of the baseband low noise amplifier, you can either set the corner frequency high to reduce the in-channel spectral noise density, or set the corner frequency lower than the high-pass filtering in the baseband filter chain.
- A bandpass filter is implemented at this node for DRM operation. This filter provides immunity from adjacent and co-channel interferers. The topology shown in Figure 6 provides a 2nd order bandpass filter via the LC tank and internal elements; this filter can provide immunity from adjacent interferers up to 2dBm at the input of the Rx port.

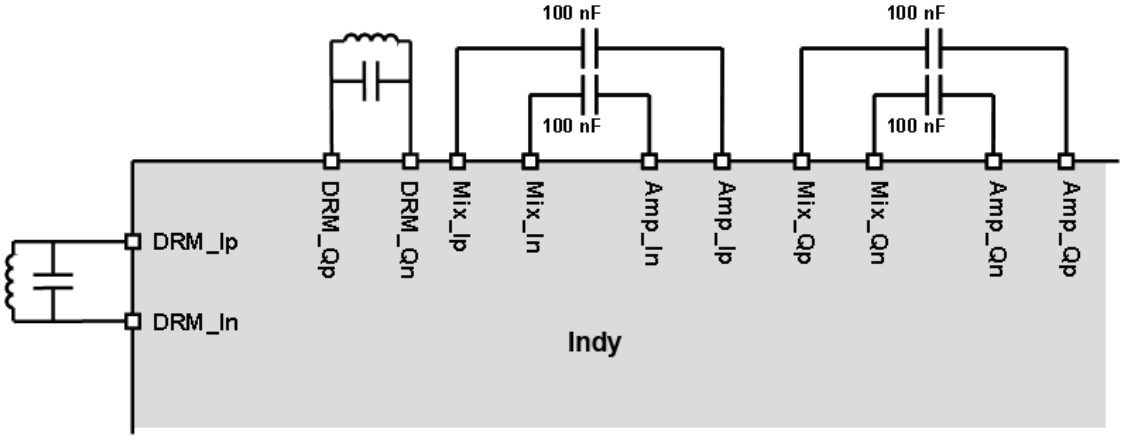
To increase the noise bandwidth corner, ensure the following requirements are met:

- The input impedance into the baseband amplifier must be high.
- The coupling capacitor can be small; however, the high-pass DC notch corner may be too high.

To lower the noise bandwidth, ensure the following requirements are met:

- The input impedance into the baseband amplifier can be low.
- The coupling capacitor must be large. The requirements are as follows:
  - The AC coupling capacitor must be charged within the protocol allowed wake-up time.[1]
  - The high-pass filter in the baseband filter chain must attenuate the noise under the receiver noise floor.
  - The choice of AC coupling capacitor size must be made in conjunction with the low noise baseband amplifier design.

Figure 4-6: Receiver Front-end External Output Interface, including DRM LC Load of Mixer



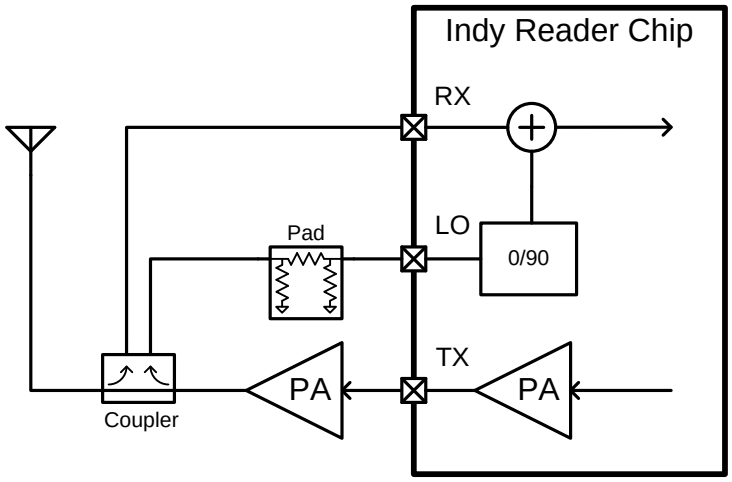
5.2 Antenna Configuration Scenarios

There are two different use scenarios for the Indy R2000 reader chip based on the antenna subsystem. The first one involves a single antenna configuration as shown in Figure 4-7. This diagram is simplified, and doesn't show filters, baluns, or matching. For more detail, see section 5.3. In this application, a directional coupler is used to isolate the transmit and receive paths. The antenna reflection of CW transmit power in receive mode dominates the receiver

[1] It is possible to improve the charging time for the AC coupling capacitor with the help of a low resistance switch to short the capacitor during the charging up phase. This approach will lower the time constant to enable a fast charge phase even with a big value AC coupling capacitor.

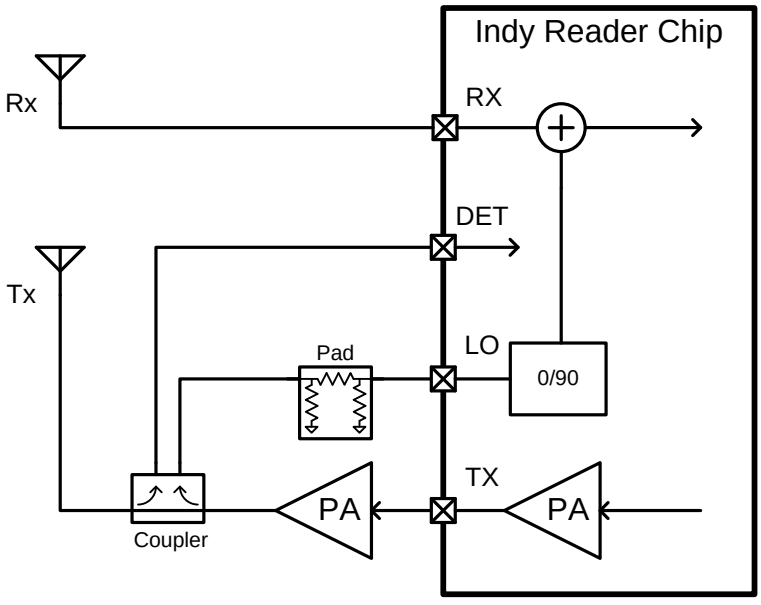
compression point requirement. A high impedance tap at the output of the PA is implemented to generate the LO_in signal used to drive the RX mixers.

Figure 4-7: Mono-static Antenna Scenario



A second scenario allows separate antenna connections for receive and transmit as shown in Figure 4-8. The isolation between the receive and transmit antenna is 25–30 dB; therefore, the in-band blocker caused by the CW transmit signal is on the order of +0 dBm. This scenario significantly reduces the compression requirements on the receiver and allows for a more sensitive receiver. A high impedance tap at the output of the PA is implemented to generate the LO_in signal used to drive the RX mixers.

Figure 4-8: Bi-static Antenna Scenario

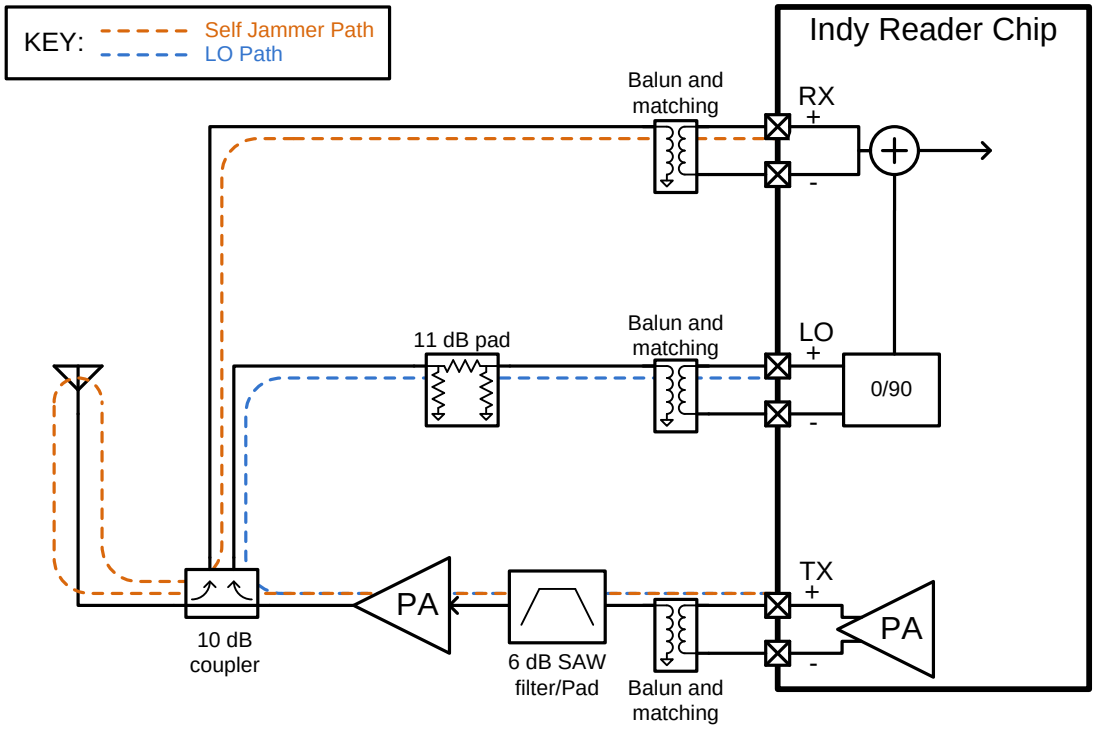


5.3 RF Transmit and Receive Path Configuration

The previous section provided a simplified explanation of the external circuitry required in the RF transmit and receive paths. It ignored topics such as differential signals, gains and losses in the paths, and matching. This section elaborates slightly on those concepts.

A more detailed view of a single antenna configuration is shown in Figure 4-9. Values shown are taken from the R2000 development kit. In this figure, the TX, RX, and LO ports are shown as differential, with a balun and associated matching networks to translate to single-ended signals. The LO and RX/Self-jammer paths are shown in blue and orange, respectively. The details of the LO and RX paths are shown in the following subsections.

Figure 4-9: Detailed TX and RX Path Block Diagram

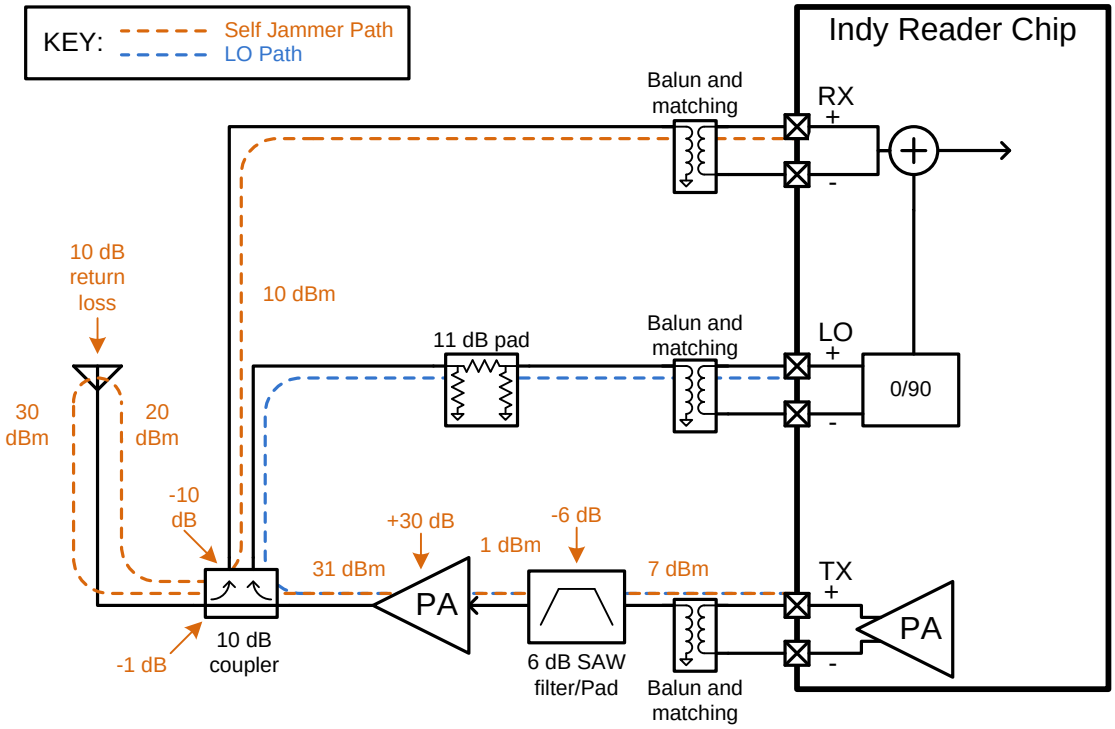


5.3.1 TX to RX (Self Jammer) Path

The TX to RX or "Self Jammer" path is the path taken by the transmitted high power signal that reflects back from the antenna (return loss) and back through the coupler towards the reader's RX port. Example losses and gains of this signal along the path are shown in Figure 4-10. These values are approximately based on the configuration used in the R2000 development kit and reference design. The path gains and losses are described below.

1. The TX signal exits the Indy Reader chip's differential TX pins at the user specified power level.
2. The signal passes through the TX balun and matching network, with a certain amount of loss, for a power level of 7 dBm.
3. The signal passes through the SAW filter or pad (depending on configuration), attenuated by 6 dB, for a power level of 1 dBm.
4. The signal is amplified by 30 dB by the external PA, for a power level of 31 dBm.
5. The signal passes through the directional coupler to the transmitted port, with a loss of 1 dB, for a power level of 30 dBm.
6. The antenna's 10 dB of return loss reflects the signal at a power level of 20 dBm.
7. The reflected signal passes through the directional coupler to the isolated port with a gain of 10 dB, for a power level of 10 dBm.
8. The 10 dBm signal passes through the balun and matching network, again with the balun's characteristic loss, and enters the Indy reader chip's differential RX port.
    - In some scenarios, a pad may be required to reduce the power level of the signal at the balun and RX port.

Figure 4-10: Detailed TX to RX (Self Jammer) Path Block Diagram

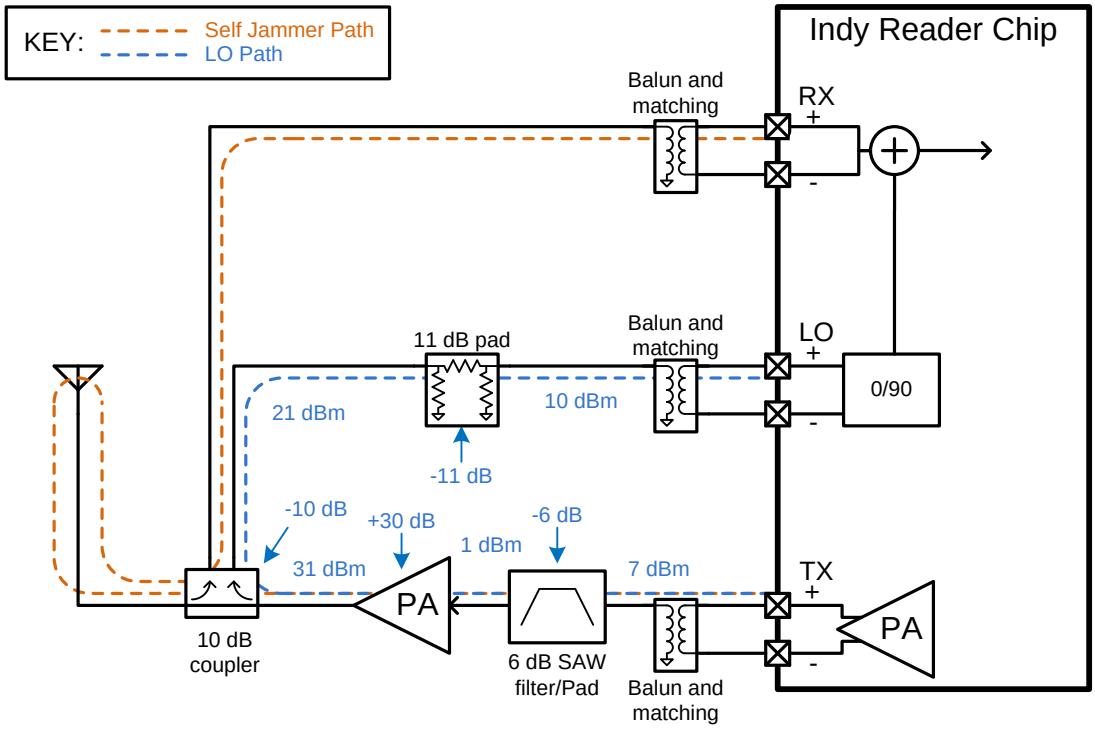


5.3.2 TX to LO (Self Jammer Cancellation) Path

The TX to LO or “Self Jammer Cancellation” path is the path taken by the transmitted high power signal that is coupled through the directional coupler towards the reader’s LO port. Example losses and gains of this signal along the path are shown in Figure 4-11. These values are approximately based on the configuration used in the R2000 development kit and reference design. The path gains and losses are described below. The gains and losses are the same as the TX to RX path until the signal hits the directional coupler.

1. The TX signal exits the Indy Reader chip’s differential TX pins at the user specified power level.
2. The signal passes through the TX balun and matching network, with a certain amount of loss, for a power level of 7 dBm.
3. The signal passes through the SAW filter or pad (depending on configuration), attenuated by 6 dB, for a power level of 1 dBm.
4. The signal is amplified by 30 dB by the external PA, for a power level of 31 dBm.
5. The signal passes through the directional coupler to the coupled port, with an attenuation of 10 dB, for a power level of 21 dBm.
6. The signal is attenuated by 11 dB by the pad, for a power level of 10 dBm.
    a. This attenuation is selected such that the amplitude of the LO signal will be equal to the maximum expected self jammer signal at the RX port, as described in section 5.1.5.
7. The 10 dBm signal passes through the balun and matching network, again with the balun’s characteristic loss, and enters the Indy reader chip’s differential LO port.

Figure 4-11: Detailed TX to LO (Self Jammer Cancellation) Path Block Diagram



5.4 RF Power Detection

There are power detectors at the input of the LO_in, Rx_in, and Detector signals in the Indy R2000. In the single antenna configuration (see Figure 4-7), the power detector at the LO_in signal performs the forward power detection function, and the power detector at the Rx_in signal is for the reverse power detection. The power detector at the Rx_in signal can also be used to implement a rough wideband LBT function with the transmitter turned off. A small RF amplifier may be switched on to slightly improve the sensitivity of the LBT detector. The peak detectors at the output of the IF amplifiers are connected to the auxiliary (AUX) ADC and can also be used to perform rough LBT.

In dual antenna configuration (see Figure 4-8), the power detector at the LO_in signal performs the forward power detection function. The power detector at the detector signal measures the reverse power detection via a directional coupler. The power detector at the Rx_in signal can be used to implement a rough wideband LBT function with the transmitter turned off. A small RF amplifier may be switched on to slightly improve the sensitivity of the LBT detector.

There are three power detection functions provided in the Indy R2000 reader chip, listed below.

5.4.1 Forward power detection for transmit power calibration

The power is tapped after the PA using the same high impedance node used to generate the RX LO signal. This power detection is part of the transmit power calibration as well as part of the PA regulator loop that controls the voltage supply for the PA.

5.4.2 Reverse power detection for measuring antenna reflection

If the controller detects a severe mismatch, the controller shuts down the transmit PA to avoid damage.

5.4.3 Rough wideband LBT

High power (~ -30 dBm) activity is detected in the complete receive band, as defined by the external band select filter, and in the IF band following the down-conversion mixers.

5.5 Transmitter Modes

The Indy R2000 reader chip can operate in one of three transmitter modes, based on the power requirements and the modulation scheme used. This section describes these modes.

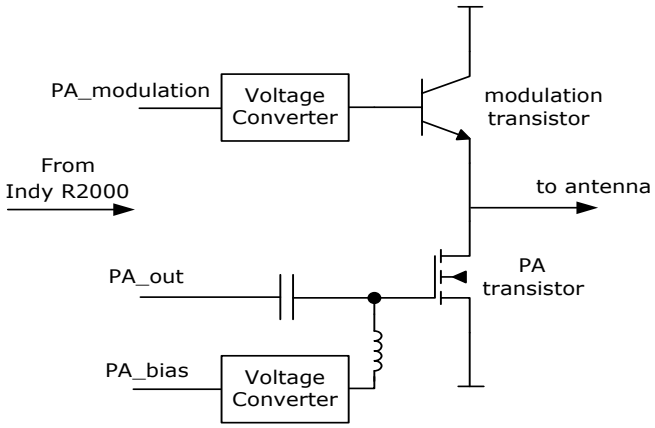
5.5.1 Linear Mode

This is the default mode of operation. The R2000 Development Kit operates in this mode. The internal power amplifier is biased class A (linear mode) for all transmit modulations.

5.5.2 Full Power Non-linear Mode (DSB-ASK)

To transmit the maximum allowable power of up to +30 dBm at the antenna, you must use an external PA. To improve the power efficiency of the system, the chip uses a Class-C polar modulation approach. In CW mode, the PA_out signal in the Indy R2000 drives the gate of the PA transistor into Class-C operation. A PA modulation DAC amplitude modulates the drain of the PA transistor. Discrete devices are used to interface between the two different voltage domains (see Figure 4-12). DSB-ASK is the only modulation supported in this mode.

Figure 4-12: Indy R2000 Reader Chip Transmit with External PA (DSB ASK)



5.5.3 Low Power Non-linear Mode (DSB-ASK)

The power control for this mode is similar to the full power mode, except that no external PA is used. Instead, an on-chip PA with lower output power is used. DSB-ASK is the only mode available in this configuration.

6 Frequency generation

6.1 Internal synthesizer

Figure 6-1 shows the VCO tuning curves.

Figure 6-1: VCO Tuning Curves

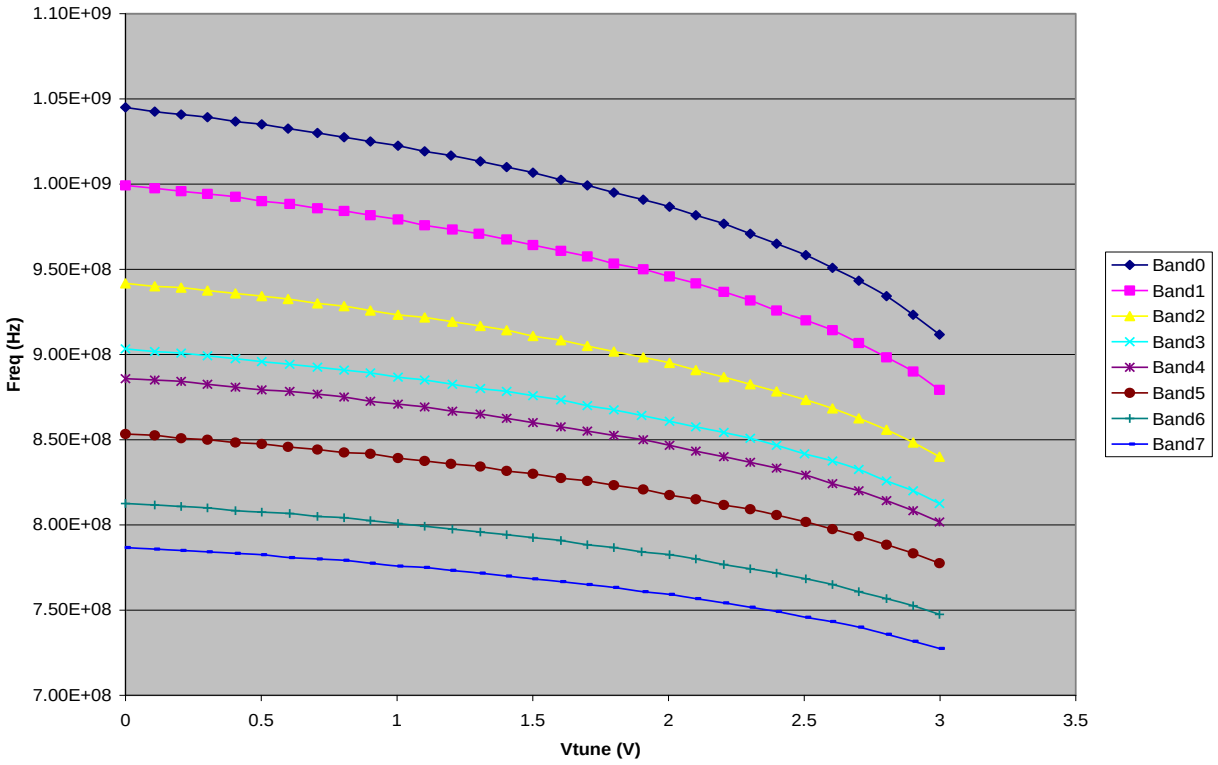


Figure 6-2 shows the phase noise at 900 MHz. The phase noise is -125 dBc/Hz at 250 kHz offset. The phase noise is measured at the output of the transmitter at an output power of +10 dBm. Table 17 shows the measured phase noise at 250 KHz offset versus current in the vdd_vco pin.

Table 17: Phase noise versus VCO current

Register $418	I(vdd_vco) [mA]	Phase noise [dBc/Hz]
1	15	-97.6
3	19	-115.7
0xB	25	-121.5
0x30	30	-123.5
0xC0	38	-125
0xF0	40	-125.2

Figure 6-2: Synthesizer Phase Noise

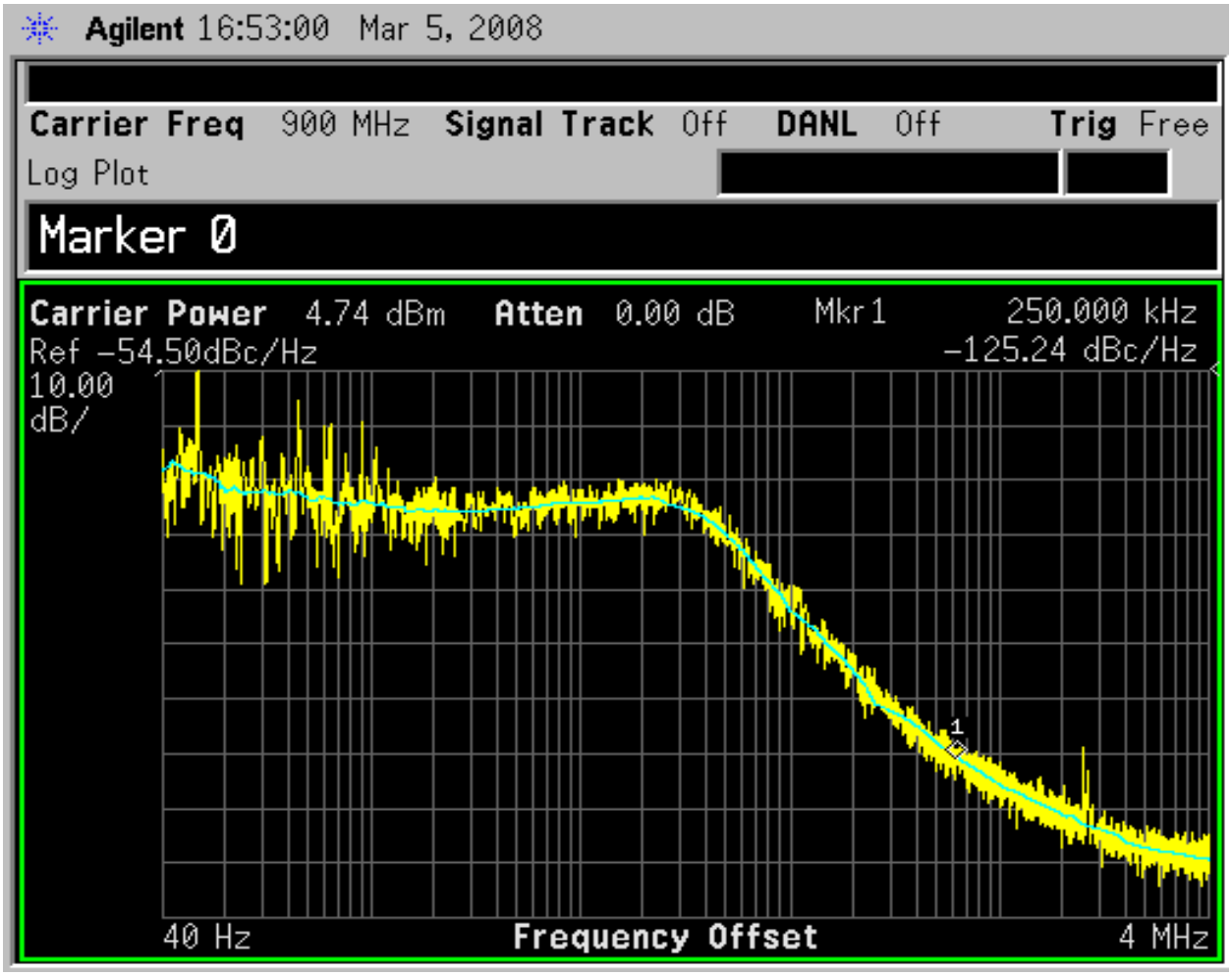
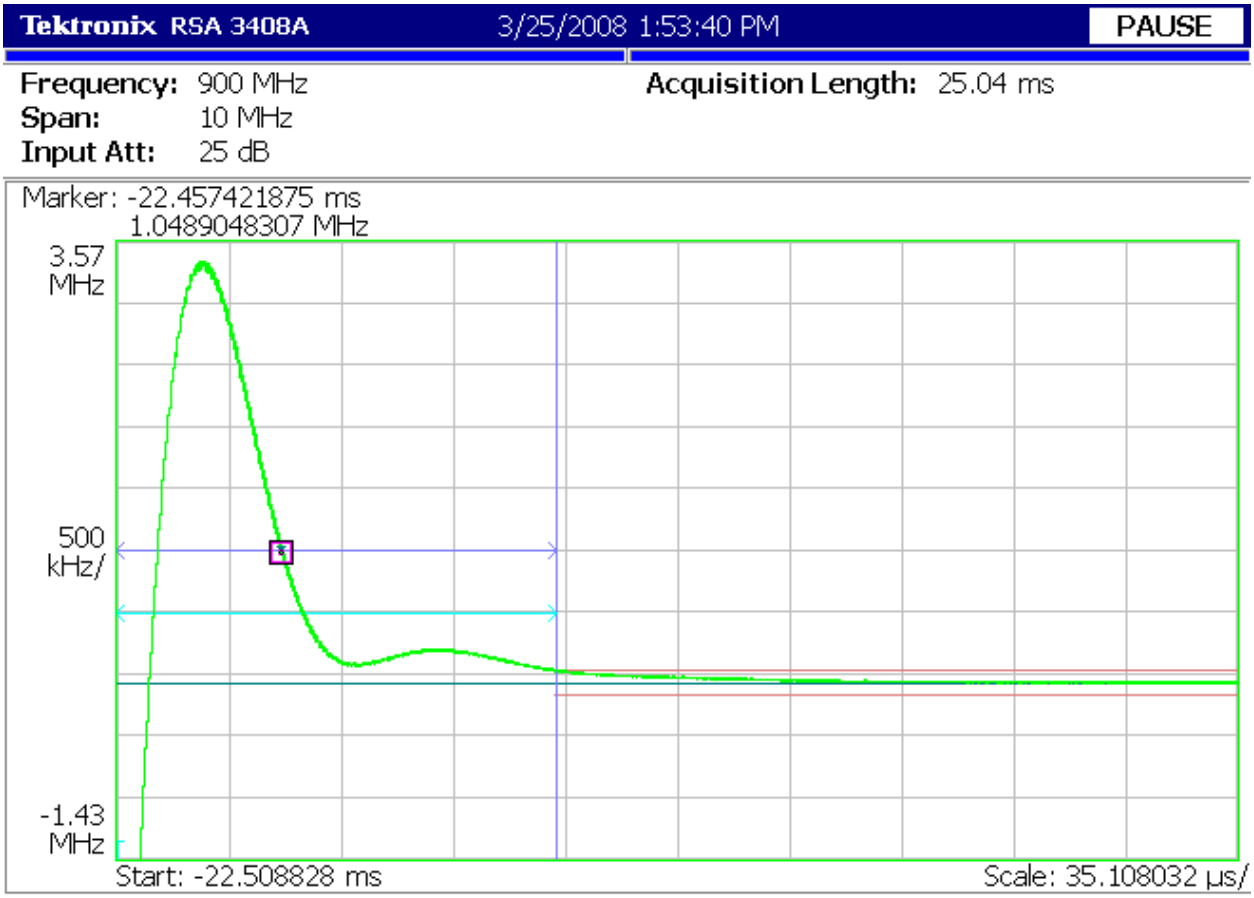


Figure 6-3 shows the PLL settling time with a reference frequency of 1 MHz, corresponding to a 250 kHz carrier frequency grid. The settling time to ±100 kHz is measured at approximately 140 μs. This measurement illustrates only the linear response of the PLL, that is, a PLL calibration is not performed. For this measurement the PLL is directly commanded to change frequencies by writing the M-divider value.

Figure 6-3: PLL Settling Time



Frequency Settling Time: 137.969 µs
(from Trigger: 137.969 µs **)**

7 Device Control and Programming

The Indy R2000 reader chip provides a high speed synchronous serial interface for programming the control settings and RFID protocol.

The interface to the microcontroller supports two different communication types:

- Low speed parallel interface (20 Mbps)
- High speed serial interface (150 Mbps downstream—to chip, and 450 Mbps upstream—from chip)

Both interfaces use the same pins and are configured through the following strapping options.

Note: The parallel interface is no longer supported for new designs. The high speed serial interface is recommended for all applications.

Table 18: Indy R2000 Modes

Mode	Pin Setting		Description
Normal mode, Parallel interface	SCAN_test = 0	Chip_resetn = 1 Dtest1 = 1	Indy R2000 is in normal operation mode using the parallel interface.
Normal mode, Serial interface	SCAN_test = 0	Chip_resetn = 1, Dtest1 = 0	Indy R2000 is in normal operation mode using the serial interface
Factory Test Mode	SCAN_test = 1	X	All analog blocks are disabled and the chip is put into factory test mode.

Table 19: Pin Functionality per Mode

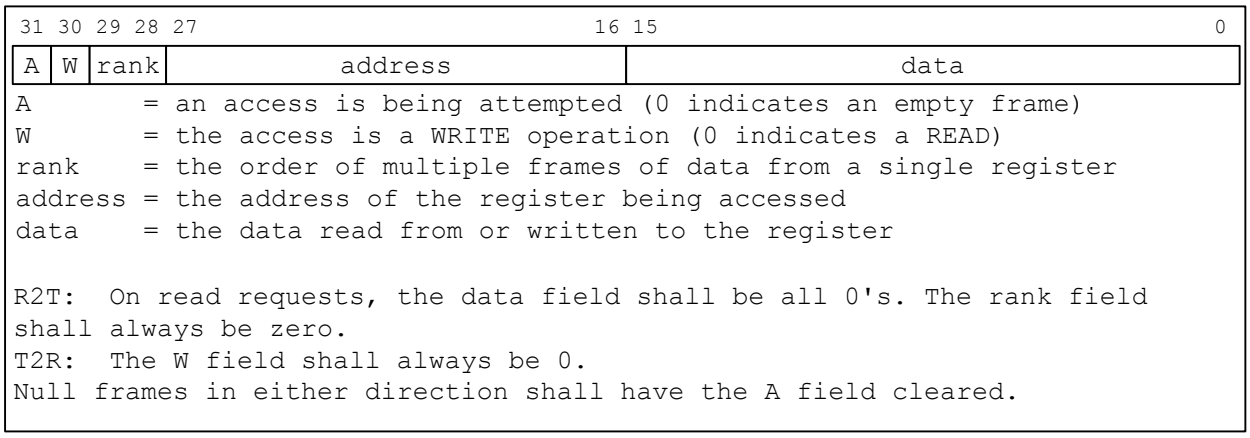
Pin Name	Parallel Interface	Serial Interface
DA3	DA3	t2r_frm
DA2	DA2	t2r_dat[2]
DA1	DA1	t2r_dat[1]
DA0	DA0	t2r_dat[0]
ALE	ALE	r2t_frm
CSn	CSn	r2t_clk
RDn	RDn	t2r_clk
WRn	WRn	r2t_dat

7.1 Serial Interface

The serial interface has four channels: one going to the Indy R2000 (R2T) and three going from the IndyR2000 (T2R). Each direction has its own clock and frame synchronization signals (R2T_CLK, T2R_CLK and T2R_FRM, R2T_FRM). The channels are denoted as R2T_D0 and T2R_D0-2.

The data is transferred in 32-bit frames delimited with the frame synchronization signal. The data is sent most significant bit (MSB) first, and the frame synchronization must occur one bit period before the MSB of the frame. When the Indy R2000 transfers data in response to a read request, it uses the lowest channel available. The chip can queue up to 16 read responses. The format of the data frame is shown in Figure 6-4.

Figure 6-4: Serial Interface Frame Format



The A parameter determines if this access has valid data or if it is an empty frame. The W parameter is set if the frame is a write operation. For T2R, this parameter is always set to zero. If the same source is read several times, the rank parameter determines the order of the incoming frames. For R2T transfers, this parameter is always set to zero. To perform a read request, the data field must be set to zero. With the serial interface, there is an additional possibility of auto-reading certain registers. When auto-reading is enabled each time, the source register is clocked

and the value is placed as a read request in the T2R FIFO. Figure 6-5 and Figure 6-6 show the timing parameters. Table 20 specifies the timing requirements for the serial interface.

Figure 6-5: Serial Interface T2R Timing

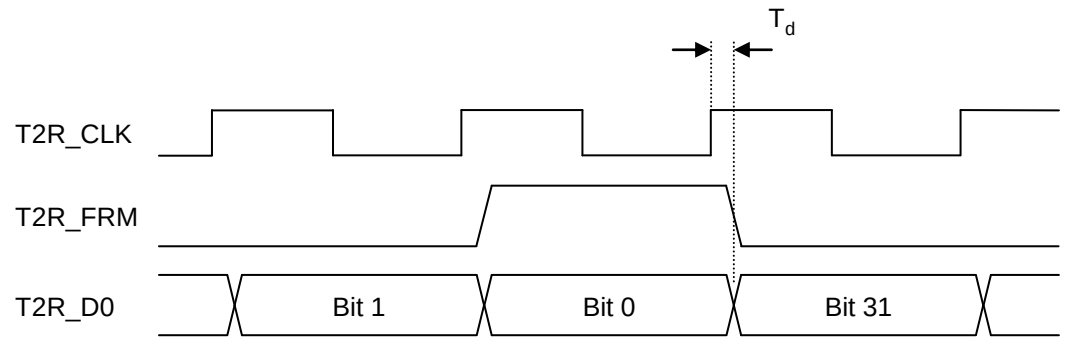


Figure 6-6: Serial Interface R2T Timing

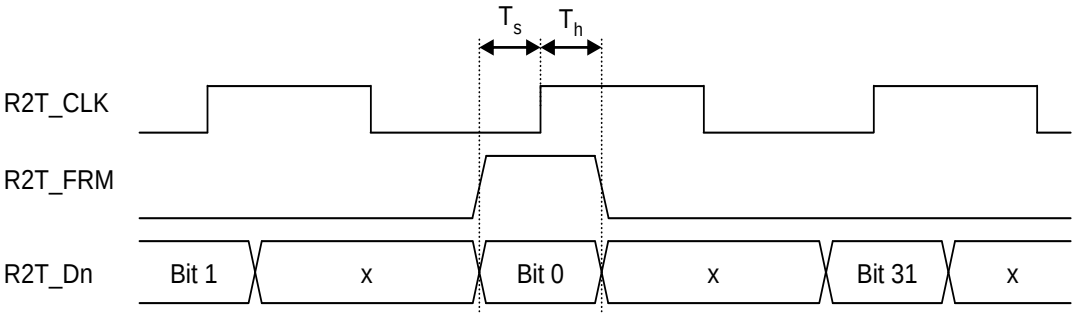


Table 20: Serial Interface Timing Requirements

Symbol	Parameter	Min	Typical	Max	Units
T_d	Data output delay	2.0		5.0	ns
T_s	Data setup time		1.0		ns
T_h	Data hold time		2.0		ns

7.1.1 Parallel Interface

The parallel interface is four bits wide with multiplexing of the data and address. The registers are double buffered to avoid mid-read updates. Figure 6-7 shows the read timing of the parallel interface, while Figure 6-8 shows the write timing.

Figure 6-7: Parallel Interface Read Timing

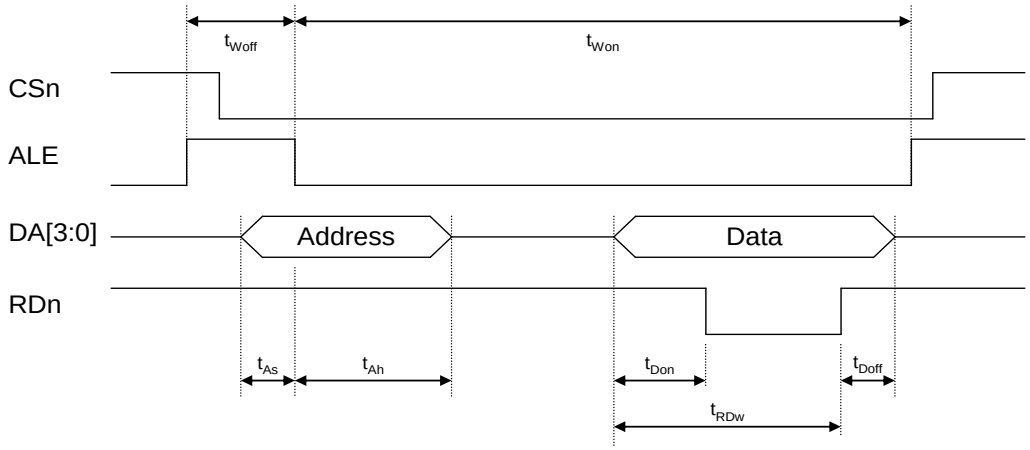


Figure 6-8: Parallel Interface Write Timing

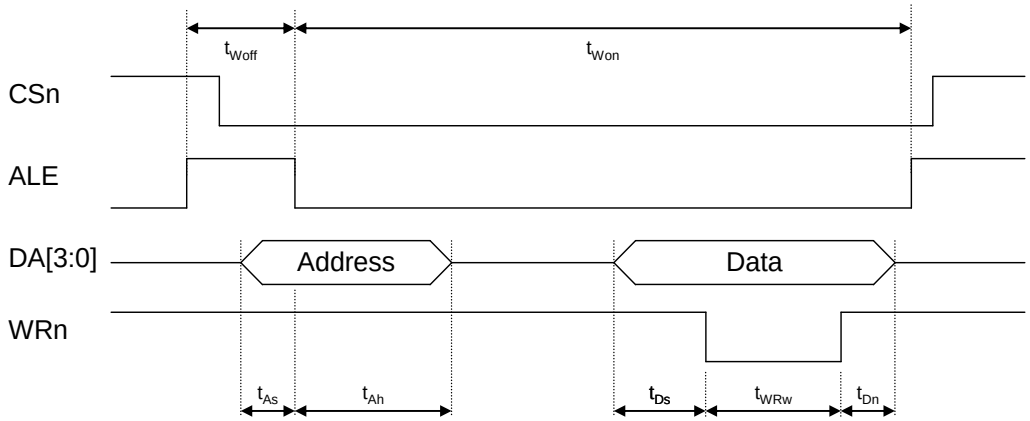


Table 21: Parallel Interface Timing Conditions

Symbol	Parameter	Min	Typ	Max	Units
t_{Won}	ALE pulse width	100			ns
t_{Woff}	ALE inactive width	100			ns
t_{As}	Address setup time	4			ns
t_{Ah}	Address hold time	0			ns
t_{RDw}/t_{WRw}	Read/Write strobe width	50			ns
t_{Don}	Data-on output delay	0		45	ns
t_{Doff}	Data-off output delay	0		45	ns
t_{Ds}	Data setup time	4			ns
t_{Dh}	Data hold time	0			ns

7.2 Register Map

Note that negative signed values are stored as two's complement. If the number is negative, two's complement conversion needs to be performed when converting between the bases. When converting to two's complement, the number of bits should be according to the bit column in Table 22.

Table 22: Register Map

Addr.	Name	R/W	Bit	Description	Reset	Type	Comment
000–03f	TX_I	R/W	11:0	TX amplitude data I	h0000	s1.10	TX look-up table (LUT) amplitude data for the I-output (signed), 64 registers.
040–07f	TX_Q	R/W	11:0	TX amplitude data Q	h0000	s1.10	TX look-up table (LUT) amplitude data for the Q-output (signed), 64 registers.

Addr.	Name	R/W	Bit	Description	Reset	Type	Comment
080–08f	TX_SD	R/W	15 14 13 12 11 10:5 4:0	Ends low flag for Manchester encoding Invert amplitude I Invert amplitude Q Enable I sign switching Enable Q sign switching LUT start address Number of samples	h0000		TX microcode table for user defined instructions, 16 registers. The “ends low” flag is used for Manchester encoding to determine whether the programmed symbol ends low. The invert amplitude flag inverts the LUT value stored, i.e., output = 1-LUT. The sign switching bits determine if the sign switches at the start of the instruction. The LUT start address is zero indexed.
090–09f	TX_HOLD	R/W	11:0	Hold value	h0000		TX microcode table for user defined instructions, 16 registers. Determines how long the last sample of the LUT command shall be held. Specified in TX clock cycles.
0a0	TX_SD_D0_0_A	R/W	15 14 13 12 11 10:5 4:0	Ends low flag for Manchester encoding Invert amplitude I Invert amplitude Q Enable I sign switching Enable Q sign switching LUT start address Number of samples	h0000		TX microcode for first part of data-0. This instruction is used when the previous symbol did not have its ends low flag set or if Manchester encoding is disabled.
0a1	TX_SD_D0_1_A	R/W	15 14 13 12 11 10:5 4:0	Ends low flag for Manchester encoding Invert amplitude I Invert amplitude Q Enable I sign switching Enable Q sign switching LUT start address Number of samples	h0000		TX microcode for second part of data-0. This instruction is used when the previous symbol did not have its ends low flag set or if Manchester encoding is disabled.
0a2	TX_SD_D1_0_A	R/W	15 14 13 12 11 10:5 4:0	Ends low flag for Manchester encoding Invert amplitude I Invert amplitude Q Enable I sign switching Enable Q sign switching LUT start address Number of samples	h0000		TX microcode for first part of data-1. This instruction is used when the previous symbol did not have its ends low flag set or if Manchester encoding is disabled.
0a3	TX_SD_D1_1_A	R/W	15 14 13 12 11 10:5 4:0	Ends low flag for Manchester encoding Invert amplitude I Invert amplitude Q Enable I sign switching Enable Q sign switching LUT start address Number of samples	h0000		TX microcode for second part of data-1. This instruction is used when the previous symbol did not have its ends low flag set or if Manchester encoding is disabled.
0a4	TX_SD_N0	R/W	15 14 13 12 11 10:5 4:0	Ends low flag for Manchester encoding Invert amplitude I Invert amplitude Q Enable I sign switching Enable Q sign switching LUT start address Number of samples	h0000		TX microcode for first part of the default symbol.

Addr.	Name	R/W	Bit	Description	Reset	Type	Comment
0a5	TX_SD_N1	R/W	15 14 13 12 11 10:5 4:0	Ends low flag for Manchester encoding Invert amplitude I Invert amplitude Q Enable I sign switching Enable Q sign switching LUT start address Number of samples	h0000		TX microcode for second part of the default symbol.
0a6	TX_SD_RU_A	R/W	15 14 13 12 11 10:5 4:0	Ends low flag for Manchester encoding Invert amplitude I Invert amplitude Q Enable I sign switching Enable Q sign switching LUT start address Number of samples	h0000		TX microcode for the ramp-up. This ramp-up is used under the following scenarios: Initial ramp-up in normal operation Manchester encoding EOT when the previous bit ended high
0a7	TX_SD_RD	R/W	15 14 13 12 11 10:5 4:0	Ends low flag for Manchester encoding Invert amplitude I Invert amplitude Q Enable I sign switching Enable Q sign switching LUT start address Number of samples	h0000		TX microcode for the ramp-down.
0a8	TX_SD_D0_0_B	R/W	15 14 13 12 11 10:5 4:0	Ends low flag for Manchester encoding Invert amplitude I Invert amplitude Q Enable I sign switching Enable Q sign switching LUT start address Number of samples	h0000		TX microcode for first part data-0 starting in the low state. This instruction is used when the previous symbol had its ends low flag set.
0a9	TX_SD_D0_1_B	R/W	15 14 13 12 11 10:5 4:0	Ends low flag for Manchester encoding Invert amplitude I Invert amplitude Q Enable I sign switching Enable Q sign switching LUT start address Number of samples	h0000		TX microcode for second part data-0 starting in the low state. This instruction is used when the previous symbol had its ends low flag set.
0aA	TX_SD_D1_0_B	R/W	15 14 13 12 11 10:5 4:0	Ends low flag for Manchester encoding Invert amplitude I Invert amplitude Q Enable I sign switching Enable Q sign switching LUT start address Number of samples	h0000		TX microcode for first part data-1 starting in the low state. This instruction is used when the previous symbol had its ends low flag set.
0aB	TX_SD_D1_1_B	R/W	15 14 13 12 11 10:5 4:0	Ends low flag for Manchester encoding Invert amplitude I Invert amplitude Q Enable I sign switching Enable Q sign switching LUT start address Number of samples	h0000		TX microcode for second part data-1 starting in the low state. This instruction is used when the previous symbol had its ends low flag set.

Addr.	Name	R/W	Bit	Description	Reset	Type	Comment
0Ac	TX_SD_RU_B	R/W	15 14 13 12 11 10:5 4:0	Ends low flag for Manchester encoding Invert amplitude I Invert amplitude Q Enable I sign switching Enable Q sign switching LUT start address Number of samples	h0000		This ramp-up is used under the following scenarios: Manchester encoding initial ramp-up Manchester encoding EOT when the previous bit ended low If the continuous reception h207[0] or alternate ramp-up is enabled h207[1].
0b0	TX_H_D0_0_A	R/W	11:0	Hold value	h0000		TX microcode for first part of data-0.
0b1	TX_H_D0_1_A	R/W	11:0	Hold value	h0000		TX microcode for second part of data-0.
0b2	TX_H_D1_0_A	R/W	11:0	Hold value	h0000		TX microcode for first part of data-1.
0b3	TX_H_D1_1_A	R/W	11:0	Hold value	h0000		TX microcode for second part of data-1.
0b4	TX_H_N0	R/W	11:0	Hold value	h0000		TX microcode for first part of the default symbol.
0b5	TX_H_N1	R/W	11:0	Hold value	h0000		TX microcode for second part of the default symbol.
0b6	TX_H_RU_A	R/W	11:0	Hold value	h0000		TX microcode for the ramp-up.
0b7	TX_H_RD	R/W	11:0	Hold value	h0000		TX microcode for the ramp-down.
0b8	TX_H_D0_0_B	R/W	11:0	Hold value	h0000		TX microcode for Manchester encoding.
0b9	TX_H_D0_1_B	R/W	11:0	Hold value	h0000		TX microcode for Manchester encoding.
0BA	TX_H_D1_0_B	R/W	11:0	Hold value	h0000		TX microcode for Manchester encoding.
0BB	TX_H_D1_1_B	R/W	11:0	Hold value	h0000		TX microcode for Manchester encoding.
0BC	TX_H_RU_B	R/W	11:0	Hold value	h0000		
0bF	TX_GO	R/W	0	Enable TX (`tx_go`)	h0000		The enable TX signal is used for starting the TX state machine.

Addr.	Name	R/W	Bit	Description	Reset	Type	Comment
0c0	TX_ENABLE	R/W	12 11 10 9 8 7:6 5:4 3:2 1 0	IQ correction Enable Bypass of Hilbert filter Hilbert filter order select Not used Not used IQ input select TX mode (Q) TX mode (I) SSB Enable Not used	h0000		Setup register for the TX data path. If IQ correction is enabled the latency of the data path is increased by one TX clock cycle. The Hilbert filter can be switched between two orders: 1 = 10^{th} order 0 = 22^{nd} order The IQ correction input select can be set to the following values: 11, 10 = Control output 01 = Bypass interpolation filter 00 = Enable interpolation filter TX mode can be set to the following values: 11 = Use predistortion 10 = Use output of power scaler 01 = Use Hilbert transformer 00 = Use Hilbert transformer and CORDIC.
0c1	TX_COEFF1	R/W	11:0	Hilbert coefficient 1	h0009	s1.10	Used for 22^{nd} order only, must be set to zero for the 10^{th} order filter.
0c2	TX_COEFF3	R/W	11:0	Hilbert coefficient 3	h0017	s1.10	Used for 22^{nd} order only, must be set to zero for the 10^{th} order filter.
0c3	TX_COEFF5	R/W	11:0	Hilbert coefficient 5	h0031	s1.10	Used for 22^{nd} order only, must be set to zero for the 10^{th} order filter.
0c4	TX_COEFF7	R/W	11:0	Hilbert coefficient 7	h005f	s1.10	
0c5	TX_COEFF9	R/W	11:0	Hilbert coefficient 9	h00c2	s1.10	
0c6	TX_COEFF11	R/W	11:0	Hilbert coefficient 11	h0284	s1.10	
0c7	TX_FREQ1	R/W	2:0	CORDIC offset	h0000	u1.18	Frequency offset value, bit 18:16. Specified as a fraction of 2π radians per TX clock cycle.
0c8	TX_FREQ2	R/W	15:0	CORDIC offset	h0000		Frequency offset value, bit 15:0. Specified as a fraction of 2π radians per TX clock cycle.
0c9	GEN_RATE	R/W	9:0	TX clock cycle duration	h0078		Specifies the TX clock cycle in 48 MHz clock cycles.
0ca	TX_TO	R/W	15:0	Final ramp-down, hold time	h0000		Time to wait after the final ramp-down before the PA is disabled. Specified in 48 MHz clock cycles.

Addr.	Name	R/W	Bit	Description	Reset	Type	Comment
0cb	TX_RU_TO	R/W	15:0	Initial ramp-up, hold time	h0000		Time to wait after initial ramp up (tag reset duration). Specified from start of ramp-up in 12 MHz clock cycles.
0cd	TX_PDIST_COEFF 0	R/W	15:0	Predistortion coefficient, c0	h0000	s6.9	
0ce	TX_PDIST_COEFF 1	R/W	15:0	Predistortion coefficient, c1	h0000	s6.9	
0cf	TX_PDIST_COEFF 2	R/W	15:0	Predistortion coefficient, c2	h0000	s6.9	
0d0	TX_PDIST_COEFF 3	R/W	15:0	Predistortion coefficient, c3	h0000	s6.9	
0d1	TX_PDIST_COEFF 4	R/W	15:0	Predistortion coefficient, c4	h0000	s6.9	
0d2	TX_PDIST_COEFF 5	R/W	15:0	Predistortion coefficient, c5	h0000	s6.9	
0d3	EOT_RU_TIME	R/W	11:0	CORDIC disable delay	h0000		Time to wait (in 48 MHz clock cycles) before re-centering the carrier in SSB mode after the EOT command has been read from the TX FIFO. Observe that this time must be shorter than the RX delay in the EOT command.
0d4	BIX_MAX	R/W	15:0		h0000		
0d5	PR_ASK_DELAY	R/W	15:8 7:0	PR-ASK delay 2 PR-ASK delay 1	h0000		For delaying the `txpsk_phase` signal. Specified in two parts, each is specified in 48 MHz clock cycles.
0d6	PA_EN_OFFSET	R/W	15:8 7:0	Delay after PA enable Delay after PA buffer enable	h0000		Provided to give PA parts a while to settle. Specified in 48 MHz cycles.
0D8	TXFILT_HOLD_EN _DELAY	R/W	15:0		h0000		Delay from start of EOT command until sample and hold in the TX filter is activated. Specified in 24 MHz cycles.
0D9	TXFILT_HOLD_ DISABLE_DELAY	R/W	15:0		h0000		Delay from the end of the RX cycle until the sample and hold in the TX filter is released. Specified in 24 MHz cycles.
0DA	TXFILT_HOLD_ PERIOD	R/W	15:0		h0000		Period of the refresh signal. Specified in 3 MHz cycles. The automatic refresh mechanism is disabled if the period is set to h0000.
0DB	RXLO_RU_DELAY	R/W	15:0	rxlo_ru_delay	h0000		Specified in 12 MHz clock cycles
0DC	RXLO_TX_DELAY	R/W	7:0	rxlo_tx_delay	h0000		Specified in 48 MHz clock cycles

Addr.	Name	R/W	Bit	Description	Reset	Type	Comment
0DD	RXLO_EOT_ DELAY	R/W	15:0	rxlo_eot_delay	h0000		Specified in 24 MHz clock cycles
0DE	TXDAC_BYPASS	R/W	7:6 5:4 3:2 0:1	DAC Q two pole select DAC I two pole select DAC Q select DAC I select	h00F0		0: SD-DAC 1: Bypass DAC 2: Constant 0 3: Constant 1
0DF	TX_DAC_DITHER	R/W	1 0	Enable I DAC dithering Enable Q DAC dithering	h0000		Setting either enable to one forces the LSB of the DAC input to one (1). This can not be overridden by register h0E9 and h0EB.
0e0	TX_DATA_I_VAL	R	11:0	TX data I	h0000	s1.10	For reading the I-input of the TX data path.
0e1	TX_DATA_I_MO	R/W	12 11:0	Enable manual override Override value for TX data I	h0000	s1.10	For overriding the I-input of the TX data path.
0e2	TX_DATA_Q_VAL	R	11:0	TX data Q	h0000	s1.10	For reading the Q-input of the TX data path.
0e3	TX_DATA_Q_MO	R/W	12 11:0	Enable manual override Override value for TX data Q	h0000	s1.10	For overriding the Q-input of the TX data path.
0e4	CORDIC_I_VAL	R	11:0	CORDIC input I	h0000	s1.10	For reading the I-input of the CORDIC.
0e5	CORDIC_I_MO	R/W	12 11:0	Enable manual override Override value for the I-input to the CORDIC	h0000	s1.10	For overriding the I-input of the CORDIC.
0e6	CORDIC_Q_VAL	R	11:0	CORDIC input Q	h0000	s1.10	For reading the Q-input of the CORDIC.
0e7	CORDIC_Q_MO	R/W	12 11:0	Enable manual override Override value for the Q-input to the CORDIC	h0000	s1.10	For overriding the Q-input of the CORDIC.
0e8	DAC_I_VAL	R	13:0	DAC I-input	h0000	s2.11	For reading the I-input of the DAC.
0e9	DAC_I_MO	R/W	14 13:0	Enable manual override Override value for the DAC I-input	h0000	s2.11	For overriding the I-input of the DAC.
0eA	DAC_Q_VAL	R	13:0	DAC Q-input	h0000	s2.11	For reading the Q-input of the DAC.
0eB	DAC_Q_MO	R/W	14 13:0	Enable manual override Override value for the DAC Q-input	h0000	s2.11	For overriding the Q-input of the DAC.
0eC	FREQ_OFF_EN_ VAL	R	0	TX freq. offset value from FSM	h0000		For reading the TX frequency offset enable bit.
0eD	FREQ_OFF_EN_ MO	R/W	1 0	Enable manual override Override value	h0000		For overriding the TX frequency offset enable bit.
0EE	PA_ENABLE_VAL	R	2 1 0	pa_buffer_e from FSM pa_driver_e from FSM pa_pa_e from FSM	h0000		Values of the PA enable signals as set by the FSM.
0EF	PA_ENABLE_MO	R/W	3 2 1 0	Enable manual override Override value pa_buffer_e Override value pa_driver_e Override value pa_pa_e	h0000		Override for the PA enable signals.

Addr.	Name	R/W	Bit	Description	Reset	Type	Comment
0F0	RXLO_ENABLE_ VAL	R	2 1 0	Internal LO from FSM External LO from FSM rxlo_enable from FSM	h0000		Values of the RXLO signals as set by the FSM.
0f1	RXLO_ENABLE	R/W	3 2 1 0	Enable Internal LO Enable External LO Enable MO of rxlo_enable Override value for rxlo_enable	h0000		Selection of RX LO signal (internal/external). Also for overriding the state-machine control of the rxlo_enable signal.
0F2	SH_ENABLE_VAL	R	0	txfilt_hold from FSM	h0000		
0F3	SH_ENABLE	R/W	1 0	Enable MO of sample and hold. txfilt_hold override value	h0000		
0FA	TX_PS_GAIN_I	R/W	11:0	Power scaler gain I	h0000	s1.10	Programming h400 corresponds to unity gain.
0FB	TX_PS_GAIN_Q	R/W	11:0	Power scaler gain Q	h0000	s1.10	Programming h400 corresponds to unity gain.
100	CTRL	R/W	1 0	IRQ enable (interrupt pin) Mission mode	h0000		Control register
101	IRQ_MASK	R/W	15:0	Interrupt mask	h0000		Masks only the interrupt pin not the interrupt status register.
102	LOCK_TO	R/W	15:0	PLL additional settling time	h0000		Time to wait after the PLL has locked before entering mission mode. Specified in 48 MHz clock cycles.
103	MODE	R/W	5 4 3 2 1 0	Enable Manchester encoding (TX) Enable 3 MHz second LO Enable `txpsk_phase`. ISO 18000 Not used Not used	h0000		Mode settings for Indy control block. The RX data path has to be configured separately. Bit 5 is affected by the SKU setting.
104	REVISION	R	15 14:12 11:0	Not used SKU bond option Digital core revision number	hx2A0		

Addr.	Name	R/W	Bit	Description	Reset	Type	Comment
105	T2R	R	15:0 15:12 11 10:8 7:0	Address for the T2R FIFO Not Used Data valid Number of valid bits Received data	h0000		Behavior depends on if a write(W) or read(R) is being performed. If being read, the T2R behavior(this row) is used. If being written, the R2T behavior (next row) is used. This register is auto-readable. Receive FIFO, 16 words deep. In the number of valid bits, 0 means full byte, 1 means 1 bit, etc.
	R2T				h0000		Transmit FIFO, 16 words deep.
	Data Command	W	15:12 11:8 7:4 3:0	Argument (arg2) Argument (arg1) Argument (arg0) Command selection (cmd)			The command selection sets the data command to be performed: cmd = b0000: Data-0 cmd = b0010: Data-1 cmd = b1000: Default symbol cmd = b1100: Byte or N-bits stored in arg 1 and arg0. arg2 determines the number of determines bits to send, where 0 = 8 bits. cmd = b1110: Send random sequence. Specified in 32-bit packets in arg2-arg0, zero = 4096 packets and one = 1 packet.
	Non-data command	W	15:11 10:9 8:6 5:2 1:0	Number of loops Lines to loop Lines to execute Start line Command selection			
	End of transfer cmd	W	15:4 3 2:0	RX delay Enable digital RX Command selection			The command selection shall be set to b01. For lines to execute and lines to loop a zero value means execute/loop one line. The start line is the offset in the microcode, starting in register h080.
	Measurement cmd	W	15:10 9 8 7:4 3 2:0	RSSI delay Enable digital RX Enable RSSI AUX ADC select Not used Command selection			The command selection shall be set to b011. RX delay is the delay (in 24 MHz clock cycles) to wait after the EOT command is read from the FIFO before enabling the digital part of the receiver. The command selection shall be set to b111. The AUX ADC select is the channel for the ADC to measure. Turning on the RSSI and the digital part of the receiver is optional. The RSSI measurement can be offset from the receiver start by specifying the RSSI delay.

Addr.	Name	R/W	Bit	Description	Reset	Type	Comment
106	DP_STAT	R	7:4 3:0	RX FIFO status TX FIFO status	h0000		Both the RX and the TX FIFO has 16 positions. The RX FIFO status is the number of free positions in the FIFO. Zero value of the status means both full FIFO and one position empty. The TX FIFO status is the number of occupied positions in the FIFO. The value hF means both full FIFO and one position empty.
	DP_CTRL	W	7 6:4 3 2:0	Flush RX FIFO RX FIFO watermark Flush TX FIFO TX FIFO watermark	h0044		The RX watermark is for overflow while the TX watermark is for underflow. The watermark is indicated through an interrupt. For the RX FIFO the interrupt is only asserted on writes to the FIFO and for the TX FIFO the interrupt is only asserted of reads. The watermarks are set to 4 by default. Writing the flush bit only clears the FIFO once.
107	ISR	R	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	SJC algorithm done Filter tuning done IF Filter too low IF Filter too high Lock detect change IF LNA too low IF LNA too high Non-empty RX FIFO AUX ADC done SDI RX FIFO overflow RX FIFO at watermark RX time-out RSSI done ADC input overdriven Read from TX FIFO TX FIFO at watermark	h0000		Read clears all nibbles of the interrupt register. Bits 15:12 are only readable and cleared through the indirect register map. This register is auto-readable. The TX and RX watermark interrupts occurs *only* when the number of entries in the FIFO is exactly at the offset specified by the watermark. Four more interrupts are available through the indirect memory. There are only cleared when the indirect memory is read.
108	DP_CTRL	R/W	7:0	Indirect address for DP_CTRL	h0044		FIFO Watermark programming. See direct register map for details.

Addr.	Name	R/W	Bit	Description	Reset	Type	Comment
109	AUTO_READ	R/W					Serial interface control
			14	Auto-read of soft demod data	h0000		Register h29C
			13	Auto-read of phase rotation angle			Register h276
			12	Auto-read of `pream_mag`			Register h2D6
			11	Auto-read of `rcorr_mag`			Register h2BC
			10	Auto-read WB `rssi_rt_values`			Register h287
			9	Auto-read NB `rssi_rt_values`			Register h286
			8	Auto-read of `rssi_blk_rt_log`			Register h288
			7	Auto-read of `rssi_blk_rt_lin`			Register h28A
			6	Auto-read of `rx_dec_q`			Register h214
			5	Auto-read of `rx_dec_i`			Register h212
			4	Auto-read of `rx_filt_q`			Register h263
			3	Auto-read of `rx_filt_i`			Register h261
			2	Auto-read of `rx_ph`			Register h273
			1	Auto-read of ISR			Register h107
			0	Auto-read of RX FIFO			Register h105
10a	DIS_T2R	R/W	3	Select frame format	h0000		Serial interface control. Select frame format: 1 = Two data words per frame. 0 = Four data words per frame. Observe that T2R_D2 must not be enabled when T2R_D1 is disabled.
			2	Enable low overhead frame			
			1	Disable T2R_D2			
			0	Disable T2R_D1			
10b	SEED_HIGH	R/W	15:0	LFSR seed high word	hA5A5		
10c	SEED_LOW	R/W	15:0	LFSR seed low word	h5A5A		
10D	AUTO_READ_DEC	R/W	15:8	Decimation of block averaged RSSI	h0000		The down-sampling factor is the register value+1. No filtering is performed, i.e., the effect of folding must be kept in mind.
			7:0	Decimation of RX data path auto read			
10e	CLKOUT_CTRL	R/W	3:0	Clock output setting	h0005		The clock output setting is decoded as follows: 0 = 48 MHz 1 = 24 MHz 2 = 12 MHz 3 = 6 MHz 4 = 3 MHz 5 = 1.5 MHz (default) 6 = Constant low output 7 = Constant high output
10F	AUTO_READ_DEC_RSSI	R/W	15:8	Decimation of WB RSSI auto-read	h0000		Auto-read decimation for RSSI registers. The down-sampling factor is the register value+1. No filtering is performed, i.e., the effect of folding must be kept in mind.
			7:0	Decimation of NB RSSI auto-read			
110	LOCK_DET_THOLD	R/W	7:0	PLL up/down pulse width threshold	h0000		The threshold for the high period of the up/down signal when the PLL is deemed unlocked. Specified in 48 MHz clock cycles.

Addr.	Name	R/W	Bit	Description	Reset	Type	Comment
111	LOCK_DETECT_CNT	R/W	15:0	Lock detect integration time	h0000		Number of comparison cycles until lock detect is asserted. Specified in 48 MHz cycles.
112	LOCK_DET_VAL	R	0	Lock detect signal from FSM	h0000		
113	LOCK_DET_MO	R/W	1 0	Enable manual override Override value	h0000		Override of the PLL lock detect signal from the FSM.
114	CLK_DBL_MO	R/W	8 7:0	Enable manual override Override value for clock doubler	h0000		Override of the clock doubler delay setting.
115	CLK_DBL_VALUE	R	7:0	Clock doubler value	h0000		Read back of clock doubler delay setting.
116	IF_TUNING_CTRL	R/W	3:2 1 0	Tuning speed Filter selection Start filter tuning	h0000		The tuning speed settings generates the following tuning rates: 0 = 100 kHz 1 = 50 kHz 2 = 25 kHz The filter selection determines which filter to tune: 1 = RX IF filter 0 = TX IF filter The start tuning bit is self-clearing.
117	IF_FILTER_RTUNE	R/W	13:8 7:6 5:0	tune_r_tx Not used tune_r_rx	h0000		R values for the tuning machine. Indirectly sets the bandwidth of the TX reconstruction filter and the RX IF filter.
118	FILTER_CAP_VAL	R	13:8 7:6 5:0	txfilt_cap Not used iffilt_cap			Result from filter tuning machine.
119	FILTER_CAP_MO	R/W	14 13:8 7 6 5:0	Enable MO of txfilt_cap Override value of txfilt_cap Not used Enable MO of iffilt_cap Override value of iffilt_cap	h0000		Override register for the capacitance values provided by the filter tuning state-machine.
11A	DCREM_VAL	R	3 2 1 0	mixer_lc_load value from logic dcrem_open_dc value from MUX dcrem_short value from MUX dcrem_open value from MUX			Read back of DC removal settings as set by the FSM.

Addr.	Name	R/W	Bit	Description	Reset	Type	Comment
11B	DCREM_MO	R/W	7 6 5 4 3 2 1 0	Enable override (mixer_lc_load) Enable override (dcrem_open_dc) Enable override (dcrem_short) Enable override (dcrem_open) Override value (mixer_lc_load) Override value (dcrem_open_dc) Override value (dcrem_short) Override value (dcrem_open)	h0000		Override register for the DC removal signals.
11C	MIXER_IFLNA_INTERF	R/W	15:4 3 2 1:0	dcrem_short pulse width Not used Enable external LC mixer load (mixer_load_select) Select IF-LNA input path (dcrem_select)	h0000		The dcrem_short pulse width is specified in 48 MHz periods. When it is set to zero no pulse is generated. IF-LNA input path: 0,1: External capacitor 2: Internal DC Path 3: Nothing connected.
130	ADC_OD_THRES	R/W	4:0	ADC input overdrive threshold	h000F		The number of consecutive samples of the same value before the “ADC overdriven” interrupt is issued. Specified in 48 MHz clock cycles.
131	IFLNA_TH_CNT	R/W	15:0	IF LNA too high threshold	hFFFF		IF LNA too high count. This determines how many 3 MHz clock cycles the too high signal from the peak detector needs to be asserted before asserting `if_lna_too_high`.
132	IFLNA_TL_CNT	R/W	15:0	IF LNA too low threshold	hFFFF		IF LNA too low count. This determines how many 3 MHz clock cycles the too low signal from the peak detector needs to be asserted before asserting `if_lna_too_low`.
133	IFLNA_RESET_CNT	R/W	15:0	IF LNA peak detector reset interval	h0000		The number of 3 MHz clock cycles between the reset pulses to the IF LNA peak detector.
134	IF_FILT_TH_CNT	R/W	15:0	IF filter too high threshold	hFFFF		IF filter too high count. This determines how many 3 MHz clock cycles the too high signal from the peak detector needs to be before asserting `if_filt_too_high`.
135	IF_FILT_TL_CNT	R/W	15:0	IF filter too low threshold	hFFFF		IF filter too low count. This determines how many 3 MHz clock cycles the too low signal from the peak detector needs to be before asserting `if_filt_too_low`.

Addr.	Name	R/W	Bit	Description	Reset	Type	Comment
136	IF_FILT_RESET_CNT	R/W	15:0	IF filter peak detector reset interval	h0000		The number of 3 MHz clock cycles between the reset pulses to the IF filter peak detector.
140	AUX_ADC_START	R	4 3:0	Start signal from FSM AUX ADC mux selection from FSM	h0000		
141	AUX_ADC_START	R/W	5 4 3:0	Enable manual start Manual start AUX ADC mux selection	h0000		For starting an AUX ADC measurement manually. The start bit is self-clearing.
142	AUX_ADC_DATA	R	7:0	AUX ADC Data	h0000		Data from the AUX ADC.
150	SJC_TIME	R/W	15:8 7:5 4:0	Settling time Not used Measurement time	h1010	u8.0 u5.0	Specified in 3 MHz clock cycles.
151	SJC_ORIGIN	R/W	12:8 7:5 4:0	Origin of Q scaling Not used Origin of I scaling	h0000	s4.0 s4.0	Center of scan matrix.
152	SJC_CONTROL	R/W	11:8 7 6:4 3 2 1 0	Scan size Not used Step size Enable rx_start automatically Use current settings as origin Reduce gain Trigger scan	h0110	u4.0 u3.0	Scan size: number of evaluation points around the origin. Set to one to get a 3x3 matrix. Not possible to program it to 0. Step size: when set to one the finest grid is used; larger settings result in a coarser grid. Not possible to program it to 0. Instead of taking the origin from register h151 the current setting (reg h154) can be used as origin if bit 2 is set. When the reduce gain bit is set the RX data path gain is automatically temporarily switched to the SJC gain settings (register 0x451 as opposed to the normal gain settings defined by register 0x450). The trigger bit is self-clearing.
153	SJC_BIAS_OFFSET	R/W	7:4 3:0	Q bias offset I bias offset	h0000	s3.0 s3.0	Offset applied to SJC current bias.
154	SJC_SCALING_OUT	R	12:8 7:5 4:0	Q scaling Not used I scaling		s4.0 s4.0	Returned scaling values.
155	SJC_SCALING_VAL	R	15:12 11:8 7:4 3:0	Qp scaling Qn scaling Ip scaling In scaling		u4.0 u4.0 u4.0 u4.0	Returned scaling values in analog notation.

Addr.	Name	R/W	Bit	Description	Reset	Type	Comment
156	SJC_SCALING_MO	R/W	15:12 11:8 7:4 3:0	Qp scaling Qn scaling Ip scaling In scaling	h0000	u4.0 u4.0 u4.0 u4.0	Manual override of applied SJC scaling. This register is affected by the SKU setting.
157	SJC_BIAS_VAL	R	7:4 3:0	Q biasing I biasing			SJC current biasing.
158	SJC_BIAS_MO	R/W	9 8 7:4 3:0	Enable manual override of scaling Enable manual override of biasing Override value of I SJC biasing Override value of Q SJC biasing	h0000		Override register for SJC signals from the algorithm.
160	IQ_CORR_C1	R/W	15:0	IQ correction forward gain, I	h0000	s1.14	
161	IQ_CORR_C2	R/W	15:0	IQ correction cross gain, I to Q	h0000	s1.14	
162	IQ_CORR_C3	R/W	15:0	IQ correction offset, I	h0000	s1.14	
163	IQ_CORR_D1	R/W	15:0	IQ correction forward gain, Q	h0000	s1.14	
164	IQ_CORR_D2	R/W	15:0	IQ correction cross gain, Q to I	h0000	s1.14	
165	IQ_CORR_D3	R/W	15:0	IQ correction offset, Q	h0000	s1.14	
200	RX_MAX	R/W	11:0	Expected number of bits	h0000		The number of bits that will be received from the tag. If this is set to zero then 2^{12}-1 bits will be received.
202	PREAM_SEARCH_WAIT	R/W	15:0	Preamble search delay	h0000		This is the delay between the start of the digital receiver and when the preamble can be found. Specified in 3 MHz clock cycles.
203	RX_TO	R/W	15:0	Receiver time-out	h0000		The time after the preamble search starts when the receiver will time-out. Specified in 3 MHz clock periods.
204	RX_START_VAL	R	0	Value of `rx_start` from FSM	h0000		
205	RX_START_MO	R/W	1 0	Enable manual override Override value for `rx_start`	h0000		For starting the digital part of the receiver manually.
206	TX_RELEASE_RX_BITS	R/W	11:0	Number of bits before end of receive packet to release the transmitter.	h0000		Enables pre-emptive transmission if this value is larger than 2. Can not be enabled if continuous reception is enabled in register h207.

Addr.	Name	R/W	Bit	Description	Reset	Type	Comment
207	IPICO	R/W	2 1 0	Disable Timeout Use alternative EOT ramp-up Enable continuous reception	h0000		Bit 0 enables continuous reception of packets/pages. Reception is started with the EOT command. This is used for iPico. To abort the reception set this bit to zero. Bit 1 forces the transmitter to use the TX_SD_RU_B symbol for the EOT command. Bit 2 disables receiver time-out. Should be set to one for continuous reception in iPico. Should however be zero when receiving multiple pages in iPico.
210	DEC_ENABLE	R/W	1 0	Enable decimate by 16 Enable programmable decimation	h0000		Bit 0 needs to be set in order for the setting in register h211 to take effect.
211	DEC_MUX_SEL	R/W	2:0	Decimation selection	h0000		Selection of decimation order: 0 = Decimate by 16 1 = Decimate by 32 2 = Decimate by 64 3 = Decimate by 128 4 = Decimate by 256 Values 5-7 also result in decimate-by-16
212	RX_DEC_I_VAL	R	15:0	I-output of decimation chain	h0000		For reading the I-output of the decimation chain (sign extended to 16 bits). This register is auto-readable.
213	RX_DEC_I_MO	R/W	14 13:0	Enable manual override Override value for decimation output I	h0000		For overriding the I-output of the decimation chain.
214	RX_DEC_Q_VAL	R	15:0	Q-output of decimation chain	h0000		For reading the Q-output of the decimation chain (sign extended to 16 bits). This register is auto-readable.
215	RX_DEC_Q_MO	R/W	14 13:0	Enable manual override Override value for decimation output Q	h0000		For overriding the Q-output of the decimation chain.
220	RX_CORDIC_A_1	R/W	0	CORDIC A offset, bit 16	h0000	s0.18	Frequency offset for RX CORDIC A. The CORDIC is disabled and by-passed if the offset value is set to zero.
221	RX_CORDIC_A_2	R/W	15:0	CORDIC A offset, bits 15:0	h0000		
222	RX_CORDIC_B_1	R/W	0	CORDIC B offset, bit 16	h0000	s0.18	Frequency offset for RX CORDIC B. The CORDIC is disabled and by-passed if the offset value is set to zero.
223	RX_CORDIC_B_2	R/W	15:0	CORDIC B offset, bits 15:0	h0000		

Addr.	Name	R/W	Bit	Description	Reset	Type	Comment
260	RX_FILTER_SEL	R/W	5:4 3 2 1 0	DC compensation decay factor DC compensation scaling Enable DC compensation (iPico) Filter bank selection Bypass RX channel filters	h0000		Decay factor: 0 = 1/32 1 = 1/64 2 = 1/128 3 = 1/256 DC compensation scaling: 0 = 0.5 1 = 0.625 Bank selection: 0 = Configuration A (regs h300 - h32E). 1 = Configuration B (regs h330 - h35E). Filter by-pass: 0 = Include filters. 1 = No filtering.
261	RX_FILT_I_VAL	R	15:0	RX filter I-output	h0000		The output value is sign extended to 16 bits. This register is auto-readable.
262	RX_FILT_I_MO	R/W	14 13:0	Enable manual override Override value of RX filter I-output	h0000		
263	RX_FILT_Q_VAL	R	15:0	RX filter Q-output	h0000		The output value is sign extended to 16 bits. This register is auto-readable.
264	RX_FILT_Q_MO	R/W	14 13:0	Enable manual override Override value of RX filter Q-output	h0000		
265	RX_IIR_VAL	R	0	rx_iir_hold signal from FSM	h0000		
266	RX_IIR_MO	R/W	1 0	Enable manual override Override value of `rx_iir_hold`	h0000		The FSM sets `rx_iir_hold` high when the remaining bits to be received is less than or equal to `rx_iir_hold_bits`.
270	RX_PH_RECOV_EN	R/W	0	Enable phase recovery	h0000		Bit 0 enables/disables the phase recovery.
271	REG_KS2	R/W	2:0	Phase recovery proportional gain	h0000		Proportional gain of the phase recovery: 0 = $8 * 2^{-10}$ 1 = $16 * 2^{-10}$ 2 = $32 * 2^{-10}$ 3 = $64 * 2^{-10}$ 4 = $128 * 2^{-10}$ 5 = $256 * 2^{-10}$ 6 = $512 * 2^{-10}$ 7 = 1

Addr.	Name	R/W	Bit	Description	Reset	Type	Comment
272	REG_KS1	R/W	2:0	Phase recovery integrator gain	b0000		Integrator gain of phase recovery: 0 = 1 * 2^{-10} 1 = 2 * 2^{-10} 2 = 4 * 2^{-10} 3 = 8 * 2^{-10} 4 = 16 * 2^{-10} 5 = 32 * 2^{-10} 6 = 64 * 2^{-10} 7 = 128 * 2^{-10}
273	RX_PH_VAL	R	15:0	Phase recovery output			This register is auto-readable.
274	RX_PH_MO	R/W	15:0	Override value of phase recovery output	h0000		This register is affected by the SKU setting.
275	RX_PH_MO_EN	R/W	0	Enable manual override	h0000		Enable manual override of phase recovery output.
276	RX_PH_ANGLE_VAL	R	7 6:0	Preamble found Phase recovery rotation angle		u0.7	This register is auto-readable.
277	RX_PH_ANGLE_MO	R/W	8 7 6:0	Enable manual override of angle Not used Override value of rotation angle	h0000	u0.7	Enable manual override of phase recovery rotation angle. The rotation is specified as a fraction of 2π.
280	RSSI_START_VAL	R	1 0	NB RSSI start value from FSM WB RSSI start value from FSM	h0000		
281	RSSI_START_MO	R/W	3 2 1 0	Enable manual start of NB RSSI Manual start of NB RSSI Enable manual start of WB RSSI Manual start of WB RSSI	h0000		The start bits are self-clearing.

Addr.	Name	R/W	Bit	Description	Reset	Type	Comment
282	RSSI_BLOCK_AVG	R/W	15:13 12:10 9:7 6 5:3 2:0	Averaging shift during timeout. Averaging of RT NB RSSI Averaging of RT WB RSSI Enable real-time RSSI Averaging of NB RSSI Averaging of WB RSSI	h0000		The real-time RSSI averaging can take the following values (both narrow- and wide-band): 0 = 1 sample. 1 = 2 samples. 2 = 4 samples. 3 = 8 samples. 4 = 16 samples. 5 = 32 samples. 6 = 64 samples. 7 = 128 samples. The normal narrow-band RSSI averaging can assume the following values: 0 = 8 samples. 1 = 16 samples. 2 = 32 samples. 3 = 64 samples. 4 = 128 samples. 5 = 256 samples. 6 = 512 samples. 7 = 1024 samples. The normal wide-band RSSI averaging can assume the following values: 0 = 32 samples. 1 = 64 samples. 2 = 128 samples. 3 = 256 samples. 4 = 512 samples. 5 = 1024 samples. 6 = 2048 samples 7 = 4096 samples.
283	RSSI_RUNNING_AVG	R/W	5:3 2:0	Running averaging of RT NB RSSI Running averaging of RT WB RSSI	h0000		The size of the running average of the real-time RSSI can take the following values (both narrow- and wide-band): 0 = 1 sample. 1 = 2 samples. 2 = 4 samples. 3 = 8 samples. 4 = 16 samples.
284	RSSI_LOG_SMALL	R	15:8 7:0	Narrow-band RSSI value in $\log_2$ Wide-band RSSI value in $\log_2$	h0000		Block average only. This is only updated on measurement commands and other triggers. Narrow band: 5 bits exponent, 3 bits mantissa. Wide band: 4 bits exponent, 4 bits mantissa.
285	RSSI_RT_AVG_LOG_SML	R	15:8 7:0	Real-time WB RSSI value in $\log_2$ Real-time NB RSSI value in $\log_2$	h0000		Running average over block average. This is the truncated version of registers h288 and h289. Narrow band: 5 bits exponent, 3 bits mantissa. Wide band: 4 bits exponent, 4 bits mantissa.

Addr.	Name	R/W	Bit	Description	Reset	Type	Comment
286	RSSI_RT_LOG_NB	R	13:0	Real-time NB RSSI value in $\log_2$	h0000		Block average only. 5 bits exponent, 9 bits mantissa. This register is auto-readable.
287	RSSI_RT_LOG_WB	R	13:0	Real-time WB RSSI value in $\log_2$	h0000		Block average only. 4 bits exponent, 10 bits mantissa. This register is auto-readable.
288	RSSI_RT_AVG_LOG_NB	R	13:0	Real-time NB RSSI value in $\log_2$	h0000		Running average over block average. 5 bits exponent, 9 bits mantissa. This register is auto-readable.
289	RSSI_RT_AVG_LOG_WB	R	13:0	Real-time WB RSSI value in $\log_2$	h0000		Running average over block average. 4 bits exponent, 10 bits mantissa.
28A	RSSI_RT_AVG_LIN_NB	R	13:0	Real-time NB RSSI linear value	h0000		Running average over block average. No floating point representation. This register is auto-readable.
28B	RSSI_RT_AVG_LIN_WB	R	13:0	Real-time WB RSSI linear value	h0000		Running average over block average. No floating point representation.
291	DEMOD_ENABLE	R/W	7:4 3 2 1 0	Miller out signal delay Not used Reduce matched filter sync delay Enable ISO demodulator Enable ISO demod clk generation	h0000		Miller out signal delay: A delay between the Miller subcarrier removal block and the preamble correlator and matched filter blocks. Used to optimize the phase of the sampling. Specified in clock cycles of a clock that runs eight times faster than the data path, i.e., f_{8x} = 48 MHz / dec_factor * 8.
292	SFILT_COEFF_1	R/W	15:8 7:0	Smoothing filter coefficient c_2 Smoothing filter coefficient c_1	h0000	s-1.8 s-1.8	The coefficients are numbered from c_1 to c_{16}
293	SFILT_COEFF_2	R/W	15:8 7:0	Smoothing filter coefficient c_4 Smoothing filter coefficient c_3	h0000	s-1.8 s-1.8	
294	SFILT_COEFF_3	R/W	15:8 7:0	Smoothing filter coefficient c_6 Smoothing filter coefficient c_5	h0000	s-1.8 s-1.8	
295	SFILT_COEFF_4	R/W	15:8 7:0	Smoothing filter coefficient c_8 Smoothing filter coefficient c_7	h0000	s-1.8 s-1.8	
296	SFILT_COEFF_5	R/W	15:8 7:0	Smoothing filter coefficient c_{10} Smoothing filter coefficient c_9	h0000	s-1.8 s-1.8	

Addr.	Name	R/W	Bit	Description	Reset	Type	Comment
297	SFILT_COEFF_6	R/W	15:8 7:0	Smoothing filter coefficient c_{12} Smoothing filter coefficient c_{11}	h0000	s-1.8 s-1.8	
298	SFILT_COEFF_7	R/W	15:8 7:0	Smoothing filter coefficient c_{14} Smoothing filter coefficient c_{13}	h0000	s-1.8 s-1.8	
299	SFILT_COEFF_8	R/W	15:8 7:0	Smoothing filter coefficient c_{16} Smoothing filter coefficient c_{15}	h0000	s-1.8 s-1.8	
29A	MATCH_FILT_VAL	R	12:10 9:2 1 0	Value of max_idx Value of max_mag Value of rclk_match_filt Value of pream_found	h0000		
29B	MATCH_FILT_MO	R/W	13 12:10 9:2 1 0	Enable manual override Override value of max_idx Override value of max_mag Override value of rclk_match_filt Override value of pream_found	h0000		
29C	MATCH_FILT_ SOFT	R	10:8 7:0	Selected matched filter index Selected matched filter magnitude			Soft demodulation data. This register is auto-readable.
2a0	DRATE_ENABLE	R/W	1 0	Enable data rate correction Hold correction on preamble found	h0000		
2a1–2ab	RCORR_TICKS	R/W	13:0	Clock rates of rate correlators	h0000		Number of 48 MHz clock ticks per oversampled demodulator clock period. The value is scaled with 2^4.
2b1–2bb	RCORR_LUT	R/W	13:0	Tick compensation LUT	h0000		
2bC	RCORR_MAG	R	6:0	Maximum magnitude of the rate estimation correlators	h0000		This register is auto-readable.
2bd	DRATE_CTRL	R/W	7 6 5 4:0	Rate estimation filter length Enable abs value in rate est restart Enable median filter in restart Peak hold counter	h0000		Selection of rate estimator filter length: 0 = 64 taps 1 = 96 taps The rate estimator filter bank coefficients are programmable and defined in registers h360-h365.
2be	DRATE_THRES	R/W	15:8 6:0	Rate estimator restart threshold Rate correction threshold	hFF00		If the rate estimator restart threshold is set to hFF the restart mechanism is disabled.
2bf	DRATE_CNT_ THRES	R/W	15:8 7:0	Above count threshold Below count threshold	h0000		The number of samples above/below the threshold required to set/reset rate est. flag.

Addr.	Name	R/W	Bit	Description	Reset	Type	Comment
2c0	FIFO_DELAY_SEL	R/W	2:0	Delay select	b0000		Delay between rate estimator and the rest of the demodulator: 0 = 0 samples. 1 = 32 samples. 2 = 64 samples. 3 = 96 samples. 4 = 128 samples. 5 = 160 samples. 6 = 192 samples. 7 = 224 samples.
2c1	DEMOD_DEFAULT_NUM_TICKS	R/W	13:0	Ticks per oversampled clock	h0000	s9.4	Number of 48 MHz clock ticks per oversampled demodulator clock period. This register is affected by the SKU setting.
2c2	GAD_PROP_GAIN_PREAM	R/W	9:0	Proportional gain, before the preamble is found	h0000	s3.6	Proportional timing recovery gain before the preamble is found.
2c3	GAD_INT_GAIN_PREAM	R/W	9:0	Integrator gain, before the preamble is found	h0000	s1.8	Integrator timing recovery gain before the preamble is found.
2c4	GAD_PROP_GAIN	R/W	9:0	Proportional gain, after the preamble is found	h0000	s3.6	Proportional timing recovery gain after the preamble is found.
2c5	GAD_INT_GAIN	R/W	9:0	Integrator gain, after the preamble is found	h0000	s1.8	Integrator timing recovery gain after the preamble is found.
2c6	GARDNER_CTRL	R/W	4 3 2 1 0	En GAD when rate est. has locked Reset GAD with rate estimator Enable median filter in GAD Enable reset of GAD loop filter (Enable clock generation reset)	h0008		When reset is enabled the loop filter and/or the clock generation is reset when the preamble is found. Bit 0 must always be zero for proper operation.
2c7	GARDNER_CTRL	R/W	5:4 3 2:0	NCO offset hit value Not used NCO hit value	h0000		For ISO 18000-6B/C: NCO_offset_hit_value=2 NCO_hit_value=4 For iPico: NCO_offset_hit_value=1 NCO_hit_value=2
2c8	TAG_RATE_PREAM	R	13:0	NCO input (sd_mod_in) at rising edge of pream_found		s9.4	The NCO runs at eight times the link frequency.
2c9	TAG_RATE_END	R	13:0	NCO input (sd_mod_in) at falling edge of pream_found		s9.4	
2d1	PREAM_CTRL	R/W	14:8 7 6:0	Miller sub-carrier phase Not used Preamble threshold	h0000		The preamble correlator coefficients are programmable and defined in registers h370-h37B. The demodulator matched filter coefficients are programmable and defined in registers h380-h397.

Addr.	Name	R/W	Bit	Description	Reset	Type	Comment
2d2	MILLER_CTRL	R/W	13 12:6 5:2 1 0	Miller subcarrier filter selection Miller M value Sub-carrier alignment delay Enable Miller clock Enable Miller sub-carrier removal	h0000		The valid range for Miller M values is from 2 to 64.
2d3	SFILT_OUTPUT	R	7:0	Smoothing filter output	h0000		Test point
2d4	DRATE_NCO_ INPUT	R	13:0	Data rate est. input to NCO	h0000		Test point
2d5	GAD_NCO_INPUT	R	10:0	GAD input to NCO	h0000		Test point
2d6	PREAM_MAG	R	6:0	Magnitude of the preamble correlator	h0000		This register is auto-readable.
2d7	PREAM_MAG_ PEAK	R	14:8 7 6:0	Running peak value Not used Magnitude when preamble found	h0000		Reset at the beginning of each RX slot. The running peak value is the maximum value of the preamble correlator. Once the preamble is found the low byte will hold the peak preamble correlator value that triggered the preamble found. This register can be used to evaluate the signal quality.
2d8	MILLER_COEFF_ A1_1	R/W	0	Bit 16 of IIR coefficient a_1	h0000	s1.15	
2d9	MILLER_COEFF_ A1_2	R/W	15:0	Bit 15:0 of IIR coefficient a_1	h0000		
2dA	MILLER_COEFF_ A2_1	R/W	0	Bit 16 of IIR coefficient a_2	h0000	s1.15	
2dB	MILLER_COEFF_ A2_2	R/W	15:0	Bit 15:0 of IIR coefficient a_2	h0000		
2dC	MILLER_COEFF_ S1_1	R/W	0	Bit 16 of IIR coefficient s_1	h0000	s1.15	
2dD	MILLER_COEFF_ S1_2	R/W	15:0	Bit 15:0 of IIR coefficient s_1	h0000		
2dE	BEGIN_PREAM_ SEARCH_VAL	R	0	begin_pream_search from FSM	h0000		
2DF	BEGIN_PREAM_ SEARCH_MO	R/W	1 0	Enable manual override Override value for begin_pream_search			Enables override of begin_pream_search.

Addr.	Name	R/W	Bit	Description	Reset	Type	Comment
300	RX_FIR_IIR_A	R/W	13:8 7:4 3:2 1 0	Number of bits to hold IIR Selection RX FIR filter length Not used Enable RX IIR filter Enable RX FIR filter	h0000		Selection RX FIR filter length: 0 = 36 taps 1 = 42 taps 2 = 48 taps 3 = 54 taps 4 = 60 taps 5 = 66 taps 6 = 72 taps 7 = 78 taps 8 = 84 taps The IIR filter output is set to zero whenever the filter is disabled.
301-32A	CF_COEFF_A	R/W	14:0	RX FIR filter coefficients	h0000	s0.14	Coefficients for the receive FIR channel filter. The coefficients are symmetric, i.e. c_0=c_{83}. 42 registers, h222 specifies c_0. For filters shorter than 84 taps, only the coefficients used (c_0 to $c_{\#taps-1}$) need to be specified.
32B	COEFF_A1_A	R/W	15:0	Bit 15:0 of IIR coefficient a_1	h0000	s1.15	Denominator coefficient.
32C	COEFF_A2_A	R/W	15:0	Bit 15:0 of IIR coefficient a_2	h0000		Denominator coefficient.
32D	COEFF_S1_A	R/W	15:0	Bit 15:0 of IIR coefficient s_1	h0000		
32E	COEFF_A1_A2_S1_A	R/W	2 1 0	Bit 16 of IIR scale factor s_1 Bit 16 of IIR coefficient a_2 Bit 16 of IIR coefficient a_1	h0000		
330	RX_FIR_IIR_B	R/W	13:8 7:4 3:2 1 0	Number of bits to hold IIR Selection RX FIR filter length Not used Enable RX IIR filter Enable RX FIR filter	h0000		Selection RX FIR filter length: 0 = 36 taps 1 = 42 taps 2 = 48 taps 3 = 54 taps 4 = 60 taps 5 = 66 taps 6 = 72 taps 7 = 78 taps 8 = 84 taps The IIR filter output is set to zero whenever the filter is disabled.
331-35A	CF_COEFF_B	R/W	14:0	RX FIR filter coefficients	h0000	s0.14	Coefficients for the receive FIR channel filter. The coefficients are symmetric, i.e. c_0=c_{83}. 42 registers, h222 specifies c_0. For filters shorter than 84 taps, only the coefficients used (c_0 to $c_{\#taps-1}$) need to be specified.
35B	COEFF_A1_B	R/W	15:0	Bit 15:0 of IIR coefficient a_1	h0000	s1.15	Denominator coefficient.
35C	COEFF_A2_B	R/W	15:0	Bit 15:0 of IIR coefficient a_2	h0000		Denominator coefficient.
35D	COEFF_S1_B	R/W	15:0	Bit 15:0 of IIR coefficient s_1	h0000		
35E	COEFF_A1_A2_S1_B	R/W	2 1 0	Bit 16 of IIR scale factor s_1 Bit 16 of IIR coefficient a_2 Bit 16 of IIR coefficient a_1	h0000		

Addr.	Name	R/W	Bit	Description	Reset	Type	Comment
360	DRATE_COEFF_C95_80	R/W	15:0	DRE coefficients c95 to c80	h0000	u0.0	Coefficients for the data rate estimation filter bank. 0 is mapped to -1 1 is mapped to +1
361	DRATE_COEFF_C79_64	R/W	15:0	DRE coefficients c79 to c64	h0000	u0.0	
362	DRATE_COEFF_C63_48	R/W	15:0	DRE coefficients c63 to c48	h0000	u0.0	
363	DRATE_COEFF_C47_32	R/W	15:0	DRE coefficients c47 to c32	h0000	u0.0	
364	DRATE_COEFF_C31_16	R/W	15:0	DRE coefficients c31 to c16	h0000	u0.0	
365	DRATE_COEFF_C15_0	R/W	15:0	DRE coefficients c15 to c0	h0000	u0.0	
370	PREAM_COEFF_C95_88	R/W	15:14 13:12 11:10 9:8 7:6 5:4 3:2 1:0	Preamble coefficient c95 Preamble coefficient c94 Preamble coefficient c93 Preamble coefficient c92 Preamble coefficient c91 Preamble coefficient c90 Preamble coefficient c89 Preamble coefficient c88	h0000	s0.0 s0.0 s0.0 s0.0 s0.0 s0.0 s0.0 s0.0	Coefficients for the preamble correlator.
371	PREAM_COEFF_C87_80	R/W	15:0	Preamble coefficients c87 to c80	h0000		
372	PREAM_COEFF_C79_72	R/W	15:0	Preamble coefficients c79 to c72	h0000		
373	PREAM_COEFF_C71_64	R/W	15:0	Preamble coefficients c71 to c64	h0000		
374	PREAM_COEFF_C63_56	R/W	15:0	Preamble coefficients c63 to c56	h0000		
375	PREAM_COEFF_C55_48	R/W	15:0	Preamble coefficients c55 to c48	h0000		
376	PREAM_COEFF_C47_40	R/W	15:0	Preamble coefficients c47 to c40	h0000		
377	PREAM_COEFF_C39_32	R/W	15:0	Preamble coefficients c39 to c32	h0000		
378	PREAM_COEFF_C31_24	R/W	15:0	Preamble coefficients c31 to c24	h0000		
379	PREAM_COEFF_C23_16	R/W	15:0	Preamble coefficients c23 to c16	h0000		
37A	PREAM_COEFF_C15_8	R/W	15:0	Preamble coefficients c15 to c8	h0000		
37B	PREAM_COEFF_C7_0	R/W	15:14 13:12 11:10 9:8 7:6 5:4 3:2 1:0	Preamble coefficient c7 Preamble coefficient c6 Preamble coefficient c5 Preamble coefficient c4 Preamble coefficient c3 Preamble coefficient c2 Preamble coefficient c1 Preamble coefficient c0	h0000	s0.0 s0.0 s0.0 s0.0 s0.0 s0.0 s0.0 s0.0	
380	DM000_COEFF_C23_16	R/W	15:0	Demodulator coefficients	h0000		Demodulator filter coefficients matched to bits 000. Leftmost bit is transmitted
381	DM000_COEFF_C15_8	R/W	15:0	Demodulator coefficients	h0000		

Addr.	Name	R/W	Bit	Description	Reset	Type	Comment
382	DM000_COEFF_C7_0	R/W	15:14 13:12 11:10 9:8 7:6 5:4 3:2 1:0	Demodulator coefficient c7 Demodulator coefficient c6 Demodulator coefficient c5 Demodulator coefficient c4 Demodulator coefficient c3 Demodulator coefficient c2 Demodulator coefficient c1 Demodulator coefficient c0	h0000	s0.0 s0.0 s0.0 s0.0 s0.0 s0.0 s0.0 s0.0	first.
383	DM001_COEFF_C23_16	R/W	15:0	Demodulator coefficients c23 to c16	h0000		Demodulator filter coefficients matched to bits 001. Leftmost bit is transmitted first.
384	DM001_COEFF_C15_8	R/W	15:0	Demodulator coefficients c15 to c8	h0000		
385	DM001_COEFF_C7_0	R/W	15:0	Demodulator coefficients c7 to c0	h0000		
386	DM010_COEFF_C23_16	R/W	15:0	Demodulator coefficients c23 to c16	h0000		Demodulator filter coefficients matched to bits 010. Leftmost bit is transmitted first.
387	DM010_COEFF_C15_8	R/W	15:0	Demodulator coefficients c15 to c8	h0000		
388	DM010_COEFF_C7_0	R/W	15:0	Demodulator coefficients c7 to c0	h0000		
389	DM011_COEFF_C23_16	R/W	15:0	Demodulator coefficients c23 to c16	h0000		Demodulator filter coefficients matched to bits 011. Leftmost bit is transmitted first.
38A	DM011_COEFF_C15_8	R/W	15:0	Demodulator coefficients c15 to c8	h0000		
38B	DM011_COEFF_C7_0	R/W	15:0	Demodulator coefficients c7 to c0	h0000		
38C	DM100_COEFF_C23_16	R/W	15:0	Demodulator coefficients c23 to c16	h0000		Demodulator filter coefficients matched to bits 100. Leftmost bit is transmitted first.
38D	DM100_COEFF_C15_8	R/W	15:0	Demodulator coefficients c15 to c8	h0000		
38E	DM100_COEFF_C7_0	R/W	15:0	Demodulator coefficients c7 to c0	h0000		
38F	DM101_COEFF_C23_16	R/W	15:0	Demodulator coefficients c23 to c16	h0000		Demodulator filter coefficients matched to bits 101. Leftmost bit is transmitted first.
390	DM101_COEFF_C15_8	R/W	15:0	Demodulator coefficients c15 to c8	h0000		
391	DM101_COEFF_C7_0	R/W	15:0	Demodulator coefficients c7 to c0	h0000		
392	DM110_COEFF_C23_16	R/W	15:0	Demodulator coefficients c23 to c16	h0000		Demodulator filter coefficients matched to bits 110. Leftmost bit is transmitted first.
393	DM110_COEFF_C15_8	R/W	15:0	Demodulator coefficients c15 to c8	h0000		
394	DM110_COEFF_C7_0	R/W	15:0	Demodulator coefficients c7 to c0	h0000		
395	DM111_COEFF_C23_16	R/W	15:0	Demodulator coefficients c23 to c16	h0000		Demodulator filter coefficients matched to bits 111. Leftmost bit is transmitted first.
396	DM111_COEFF_C15_8	R/W	15:0	Demodulator coefficients c15 to c8	h0000		
397	DM111_COEFF_C7_0	R/W	15:0	Demodulator coefficients c7 to c0	h0000		

Addr.	Name	R/W	Bit	Description	Reset	Type	Comment
400	ANA_EN1	R/W	12 11 10 9 8 7 6 5 4 3 2 1 0	lna_e mix_lo_e rflna_pdet_e rf_pdet_e lo_pdet_e iflna_e iflna_pdet_e iffilt_pdet_e iffilt_e rxtun_e ifagc_e rxadc_e txfilt_e	h0000		Analog enable signals. lna_e: Enable RF LNA rflna_pdet_e: Enable RF LNA peak detector lo_pdet_e: Enable LO peak detector iflna_e: Enable IF LNA iflna_pdet_e: Enable IF LNA peak detector iffilt_pdet_e: Enable IF FILTER peak detector iffilt_e: Enable IF filter rxtun_e: Enable analog filter tuning block ifagc_e: Enable IF AGC rxadc_e: Enable RX ADC txfilt_e: Enable TX filter Bit 1 is affected by the SKU setting.
401	ANA_EN2	R/W	6 5 4 3 2 1 0	txlo_en_ext txlo_div_e txlo_i_e txlo_q_e txmix_ssb_e txmix_pski_e txmix_pskq_e	h0000		Analog enable signals. txlo_en_ext: Enable external VCO txlo_div_e: Enable IQ divider txlo_i_e: Enable TX LO I txlo_q_e: Enable TX LO Q txmix_ssb_e: Enable SSB mode txmix_pski_e: Enable I modulator txmix_pskq_e: Enable Q modulator
402	ANA_EN3	R/W	9 8 7 6 5 4 3 2 1 0	dac1_e dac0_e modbuf_e pll_ne pll_re pll_pdcpe vco_e vco_detector_e vco_buffert_e vco_divider_e	h0000		Analog enable signals. dac1_e: Enable AUX DAC 1 dac0_e: Enable AUX DAC 0 modbuf_e: Enable modulation output buffer pll_ne: Enable PLL N divider pll_re: Enable PLL R divider pll_pdcpe: Enable PLL PD and CP. vco_e: Enable VCO vco_detector_e: Enable VCO detector vco_buffert_e: Enable VCO buffer vco_divider_e: Enable VCO divider

Addr.	Name	R/W	Bit	Description	Reset	Type	Comment
410	ANA_CTRL1	R/W	8:7 6:5 4 3:2 1:0	lflna_res Not used lo_drive_reduced_current iflna_pdet_lo iflna_pdet_hi	h0000		Analog control signals. lflna_res (impedance) settings: 0 = 10 kOhm 1 = 5 kOhm 2 = 3.3 kOhm 3 = 2.5kOhm If the lo_drive_reduced_current is enabled the LO drive current is reduced by approximately 7mA. The iflna_pdet_lo setting generates the following thresholds: 0 = 50 mV 1 = 100 mV 2 = 200 mV 3 = 400 mV The iflna_pdet_hi setting generates the following thresholds: 0 = 200 mV 1 = 600 mV 2 = 1.0 V 3 = 1.2 V
411	ANA_CTRL2	R/W	9:2 1 0	lflna_dccorr iffilt_bp iffilt_iqswap	h0000		Analog control signals. lflna_dccorr (dcofffset correction) settings: 0 = 0 mV I channel diff. offset 1 = 10 mV I channel diff. offset 2 = 20 mV I channel diff. offset 3 = 30 mV I channel diff. offset 4 = -10 mV I channel diff. offset 8 = -20 mV I channel diff. offset 12 = -30 mV I channel diff. offset 16 = 10 mV Q channel diff. offset 32 = 20 mV Q channel diff. offset 48 = 30 mV Q channel diff. offset 64 = -10 mV Q channel diff. offset 128 = -20 mV Q channel diff. offset 192 = -30 mV Q channel diff. offset iffilt_bp changes the RX filter from low-pass mode to band-pass mode. iffilt_iqswap swaps the I/Q signals at the input of the RX filter. Bit 1 is affected by the SKU setting.

Addr.	Name	R/W	Bit	Description	Reset	Type	Comment
412	ANA_CTRL3	R/W	5:4 3:2 1:0	lffilt_pdet_lo lffilt_pdet_hi ifagc_lim	h0000		Analog control signals. The ifagc_lim setting generates the following clipping levels: 0 = 770 mV 1 = 580 mV 2 = 500 mV 3 = 400 mV
413	ANA_CTRL4	R/W	7 6 5 4:3 2:0	rxadc_lime rxadc_clkinv rxadc_pr txfilt_2p txfilt_gain	h0000		Analog control signals. rxadc_lime enables the limiting function in the ADC. rxadc_clkinv enables triggering on the falling edge of the clock instead of rising. rxadc_pr enables the dithering function. The txfilt_2p setting enables the TX-filter 2-pole mode. txfilt_gain default setting is 3.
414	ANA_CTRL5	R/W	12:10 9:7 6:3 2:0	txlo_bias txmix_gain txmix_pwr txmix_bias	h0000		Analog control signals. txlo_bias control bias of the LO buffer, default setting is 3. txmix_gain control V2I gain, default setting is 3. txmix_pwr setting controls the mixer gain: 2 = -20 dB 3 = -18 dB 8 = -12 dB 11 = -10 dB txmix_bias has default setting 2.
415	ANA_CTRL6	R/W	12:9 8:3 2:0	pa_ssb pa_power pa_in_match	h0000		Analog control signals. pa_ssb sets different operation modes for the PA: 15 = Linear mode 0 = Non-linear mode pa_power controls the gain in linear mode: 3 = 13 dB 31 = 17 dB pa_in_match sets the mixer load center frequency, default setting is 4.

Addr.	Name	R/W	Bit	Description	Reset	Type	Comment
416	ANA_CTRL7	R/W	14:10 9:5 4:0	pa_mid_match pa_bufbias pa_drvbias	h410F		Analog control signals. pa_mid_match sets the PA driver load center frequency, default setting is h10. pa_bufbias sets the PA buffer bias, default setting is hF. pa_drvbias sets the PA driver bias, default setting is h8.
417	ANA_CTRL8	R/W	7:5 4:0	vco_band pa_pabias	h01A7		Analog control signals. vco_band setting: 0 = Maximum frequency 7 = Minimum frequency pa_pabias sets the bias of the PA output stage, default setting in SSB mode is hD and default setting in PSK is h7.
418	ANA_CTRL9	R/W	8:0	vco_bias	h0000		Analog control signals. vco_bias setting: 0x0 = Minimum current 0x100 = Maximum current
419	ANA_CTRL10	R/W	13:4 3:2 1:0	pll_r pll_inv pll_reset	h0184		Analog control signals. pll_r is the divider ratio of the R-divider in the PLL. pll_inv setting: 0 = test mode 1 = normal mode 2 = inverted feedback loop pll_reset decides the width of the charge pump pulse. Pll_reset setting: 00 = max width 11 = min width
41a	ANA_CTRL11	R/W	15:8 7:0	dac1_data dac0_data	h0000		Analog control signals. Input value to AUX DAC 1 and 0 respectively.

Addr.	Name	R/W	Bit	Description	Reset	Type	Comment
41b	SPARE_OUT	R/W	15:12 11:8 7:3 2:0	Spare output Dithering clock division, N Dithering offset Dithering Mode	h0000		Dithering clock division: 0: Clock disabled 1: 24 MHz 2: 12 MHz 3: 6 MHz 4: 3 MHz 5: 1.5 MHz 6: 750 kHz 7: 375 kHz 8: 188 kHz 9: 94 kHz 10: 47 kHz 11: 23 kHz 12: 12 kHz 13: 6 kHz 14: 3 kHz 15: 1.5 kHz Dithering Mode: 0: Discreet dithering: Feedback 1: Discreet dithering: DTEST0 2: Discreet dithering: ADC dithering (LFSR) 3: Discreet dithering: TX ΣΔ (I output) 4: Random dithering 5: Ramp dithering
41b	SPARE_OUT	R/W	15:9 8:7 6:4 3:0	Spare output Dithering source Dithering clock division, N Dithering offset	h0000		Dithering Source: 0: Feedback 1: DTEST0 2: ADC dithering (LFSR) 3: TX ΣΔ (I output) Dithering clock division: 0: Clock disabled 1: 24 MHz 2: 12 MHz 3: 6 MHz 4: 3 MHz 5: 1.5 MHz 6: 750 kHz 7: 375 kHz
41C	ANA_PLL_CTRL1	R/W	0	pll_n[16]	h0000		Analog control signals. pll_n is the divider ratio of the N-divider in the PLL.
41D	ANA_PLL_CTRL2	R/W	15:0	pll_n[15:0]	h0E4C		Analog control signals. pll_n is the divider ratio of the N-divider in the PLL.
420	ANA_INPUT1	R	6 5 4 3 2 1 0	vco_amp_hi vco_amp_lo iffilter_amp_hi iffilter_amp_lo Filter tuning finished (rxtun_stop) iflna_amp_hi iflna_amp_lo			Analog input signals: vco_amp_hi: VCO amplitude too high vco_amp_lo: VCO amplitude too low iflna_amp_hi: IF LNA amplitude too high iflna_amp_lo: IF LNA amplitude too low
421	ANA_INPUT2	R	7:0	Chip revision			Indy revision.
422	SPARE_IN	R	15:0	Spare input			

Addr.	Name	R/W	Bit	Description	Reset	Type	Comment
430	ANA_TEST1	R/W	11 10 9 8 7 6 5 4 3 2 1 0	rxadc_intest_i_i rxadc_intest_i_q pll_test_up pll_test_down iflna_itest iflna_qtest ifagc_iintest ifagc_qintest rxadc_intest_q_i rxadc_intest_q_q txfilt_itest txfilt_qtest			Analog test signals. pll_test_up: Set PLL charge pump up pll_test_down: Set PLL charge pump down iflna_itest: Enable IF LNA test I iflna_qtest: Enable IF LNA test Q ifagc_iintest: Enable IF AGC input test I ifagc_qintest: Enable IF AGC input test Q: rxadc_intest_q_i Enable RX ADC input test rxadc_intest_q_q I: rxadc_intest_i_i Enable RX ADC input test rxadc_intest_i_q Q txfilt_itest: Enable TX filter test I txfilt_qtest: Enable TX filter test Q
431	ANA_TEST2	R/W	1 0	adc_test atest_e			Analog test signals adc_test: Enables test feedback of AUX ADC atest_e: Enable analog test bus
43F	ANA_PWR_CTRL	R/W	4 3 2:0	Disable analog power shell Not used Gain level	h0000		When the analog power shell is enabled (default) the values for pa_power, pa_mid_match and txmix_pwr are taken from the LUT (regs h440-h44F) based on the gain level setting. When the analog power shell is disabled the values for pa_power, pa_mid_match, txmix_pwr, pa_ssb, txmix_gain and txfilt_gain are taken form their corresponding values in registers h413-h416. The setting of the gain level has then no effect.
440	ANA_PWR_CTRL_LUT0a	R/W	14:9 8:4 3:0	pa_power (reg h415, bits 8:3) pa_mid_match (reg h416, bits 14:10) txmix_pwr (reg h414, bits 6:3)			Gain dependent settings for gain level 0 (min power).
441	ANA_PWR_CTRL_LUT1a	R/W	14:0				Gain dependent settings for GL 1.
442	ANA_PWR_CTRL_LUT2a	R/W	14:0				Gain dependent settings for GL 2.
443	ANA_PWR_CTRL_LUT3a	R/W	14:0				Gain dependent settings for GL 3.
444	ANA_PWR_CTRL_LUT4a	R/W	14:0				Gain dependent settings for GL 4.

Addr.	Name	R/W	Bit	Description	Reset	Type	Comment
445	ANA_PWR_CTRL_LUT5a	R/W	14:0				Gain dependent settings for GL 5.
446	ANA_PWR_CTRL_LUT6a	R/W	14:0				Gain dependent settings for GL 6.
447	ANA_PWR_CTRL_LUT7a	R/W	14:0				Gain dependent settings for gain level 7 (max power).
448	ANA_PWR_CTRL_LUT0b	R/W	9:6 5:3 2:0	pa_ssb (reg h415, bits 12:9) txmix_gain (reg h414), bits 9:7) txfilt_gain (reg h413, bits 2:0)			Gain dependent settings for gain level 0 (min power).
449	ANA_PWR_CTRL_LUT1b	R/W	9:0				Gain dependent settings for GL 1.
44A	ANA_PWR_CTRL_LUT2b	R/W	9:0				Gain dependent settings for GL 2.
44B	ANA_PWR_CTRL_LUT3b	R/W	9:0				Gain dependent settings for GL 3.
44C	ANA_PWR_CTRL_LUT4b	R/W	9:0				Gain dependent settings for GL 4.
44D	ANA_PWR_CTRL_LUT5b	R/W	9:0				Gain dependent settings for GL 5.
44E	ANA_PWR_CTRL_LUT6b	R/W	9:0				Gain dependent settings for GL 6.
44F	ANA_PWR_CTRL_LUT7b	R/W	9:0				Gain dependent settings for gain level 7 (max power).
450	ANA_RX_GAIN_NORM	R/W	8 7:6 5:3 2:0	rflna_high_comp_norm rflna_gain_norm iflna_gain_norm ifagc_gain_norm	h0000		The rflna_gain setting generates the following RF-LNA gains: 0 = 1 dB 2 = 7 dB 3 = 13 dB The high compression mode of the RFLNA can only be combined with the 1 and 7 dB gain settings. The iflna_gain setting generates the following IF-LNA gains: 0 = 24 dB 1 = 18 dB 3 = 12 dB 7 = 6 dB The ifagc_gain setting generates the following AGC gain values: 0 = -12 dB 4 = -6 dB 6 = 0 dB 7 = 6 dB
451	ANA_RX_GAIN_SJC	R/W	8 7:6 5:3 2:0	rflna_high_comp_sjc rflna_gain_sjc iflna_gain_sjc ifagc_gain_sjc	h0000		Gain settings used during self-jammer cancellation setting optimization.
500	DTEST_INPUT	R	1 0	DTEST1 DTEST0			Only updated when the output is disabled in register 0x501.

Addr.	Name	R/W	Bit	Description	Reset	Type	Comment
501	DTEST_CTRL	R/W	1 0	DTEST1 pin output enable DTEST0 pin output enable	h0000		The MUX select signals are defined in the MAS.
502	DTEST_SELECT	R/W	14:8 7 6:0	DTEST1 mux select Not used DTEST0 mux select	h0000		The mux select signals are defined in the MAS.

Table 23: Register Map Type Definition

	Signed	Unsigned
Maximum Value	2^X-2^{-Y}	
Minimum Value	-2^X	0

Table 24: Conversion Table

Conversion to	Signed		Unsigned
	Positive Value	Negative Value	
Binary Value	(binary value)*2^{-Y}	-(2s_compl(binary value))*2^{-Y}	(binary value)*2^{-Y}
Decimal Value	(decimal value)*2^Y	2s_compl(abs(decimal value)*2^Y)	(decimal value)*2^Y

8 Performance Characteristics - Preliminary

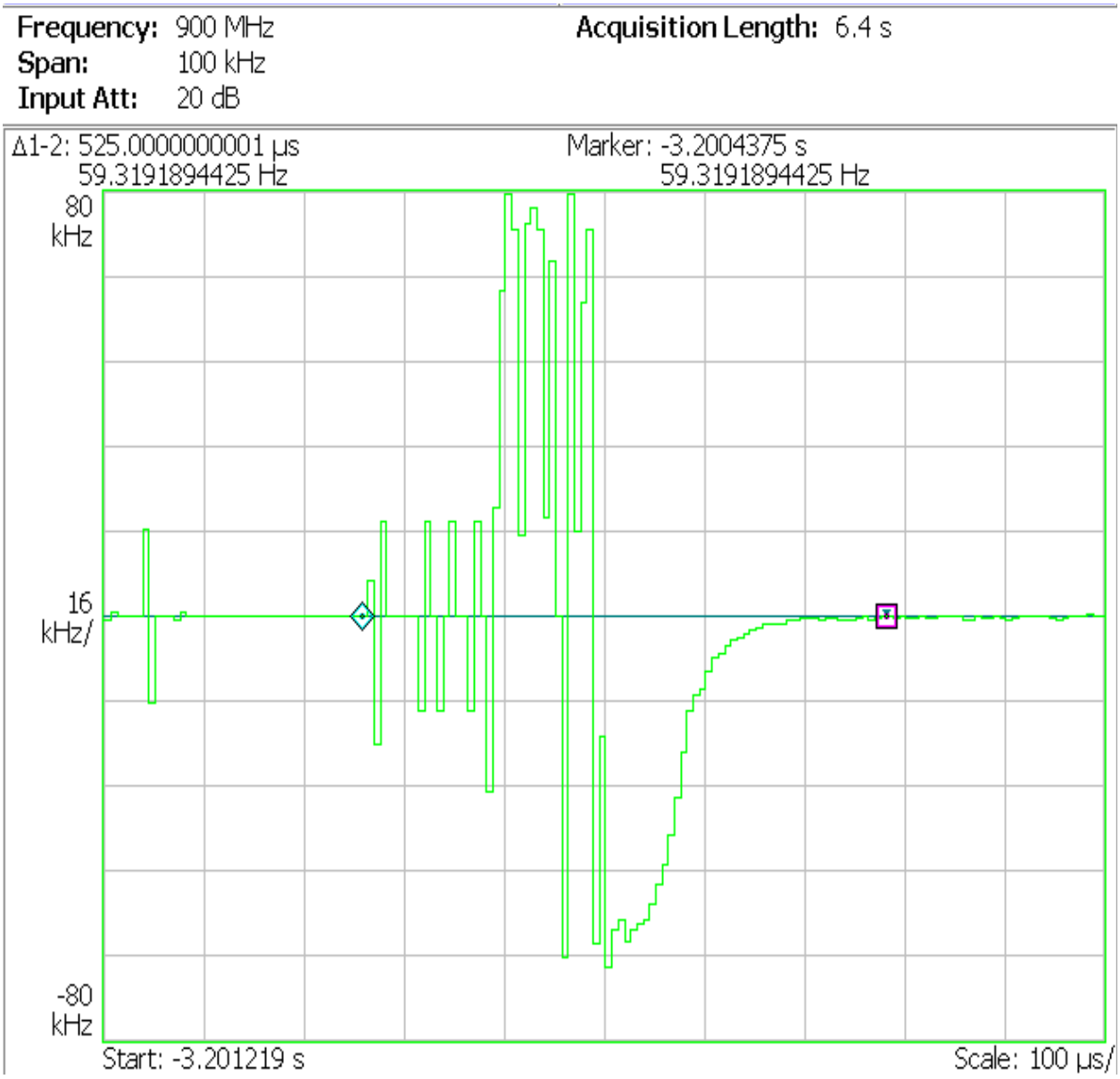
Performance characteristics include the following:

- RF to IF Conversion Gain and Gain Flatness
- Carrier Settling Time
- Transmit Output Spectral Testing
- Gain Control Resolution and Dynamic Range
- ADC Testing
- ADC Dynamic Range and Linearity
- Aux. DAC Testing

8.1 Carrier Settling Time

This test was done using a real time spectrum analyzer. The analyzer has the capability to measure RF transients. This plot shows a settling time of approximately 200 μs.

Figure 8-1: Carrier Settling Time



8.2 Rx Sensitivity Summary

Table 25 below is a summary of the ISO 18000-63 (formerly 18000-6C) sensitivity measurements. All data is for IFLNA_gain= 24 dB, IFAGC_gain= 6 dB. Sensitivity is defined as the tag power that produces a 1% Packet Error Rate (PER).

Table 25: ISO 18000-63 sensitivity summary

Encoding	Bit rate [Kbps]	Link frequency [KHz]	Offset [%]	Drift [%]	w/o self-jammer		+10dBm self-jammer and SJC enabled	
					RF_gain 1dB	RF_gain 13dB	RF_gain 1dB	RF_gain 13dB
FM0	40	40	0	0	-89	-92	-78	-78
FM0	40	40	+4	+5	-88	-88	-80	-80
FM0	40	40	-4	-3	-88	-88	-77	-77
FM0	160	160	0	0	-86	-89	-78	-79
FM0	320	320	0	0	-83	-87	-75	-77
FM0	640	640	0	0	-71	-71	-71	-71
M=2	320	640	0	0	-80	-85	-73	-74
M=4	62.5	250	0	0	-88	-91	-80	-82
M=4	62.5	250	+10	+5	-88	-91	-80	-81
M=4	62.5	250	-10	-5	-88	-92	-81	-82
M=4	75	300	0	0	-87	-91	-80	-81
M=4	160	640	0	0	-83	-88	-76	-77
M=8	80	640	0	0	-84	-88	-78	-79
M=16	40	640	0	0	-84	-88	-77	-79
M=32	20	640	0	0	-71	-71	-71	-71

8.3 Transmit Output Spectral Summary

The following figures show transmit frequency spectra in various configurations.

Figure 8-2: DSB-ASK, tari=25 µs, X=0.5 and 1.0

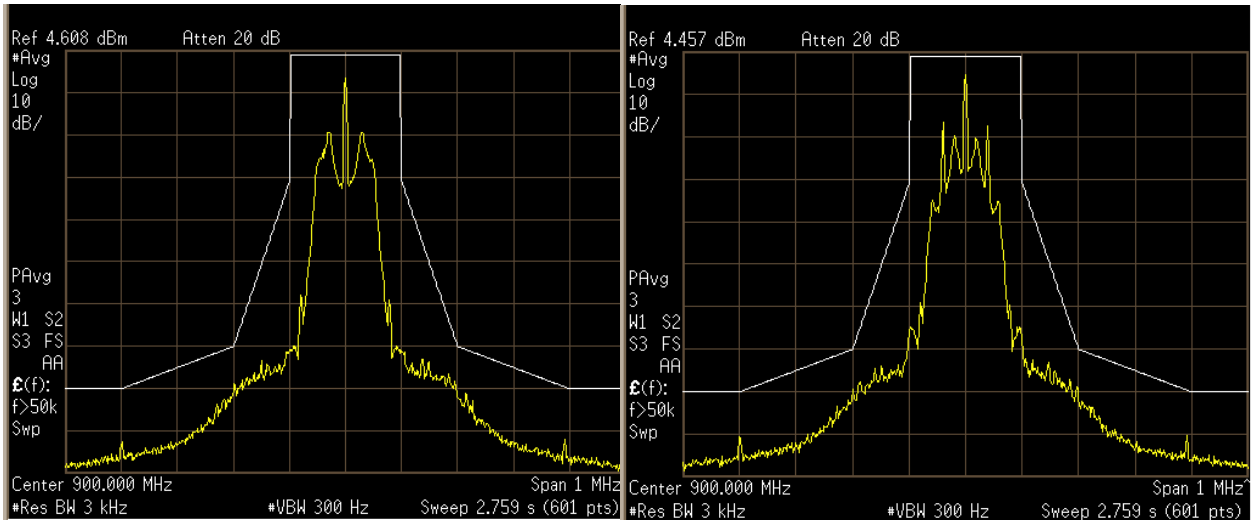


Figure 8-3: PR-ASK, tari=25 µs, X=0.5 and 1.0

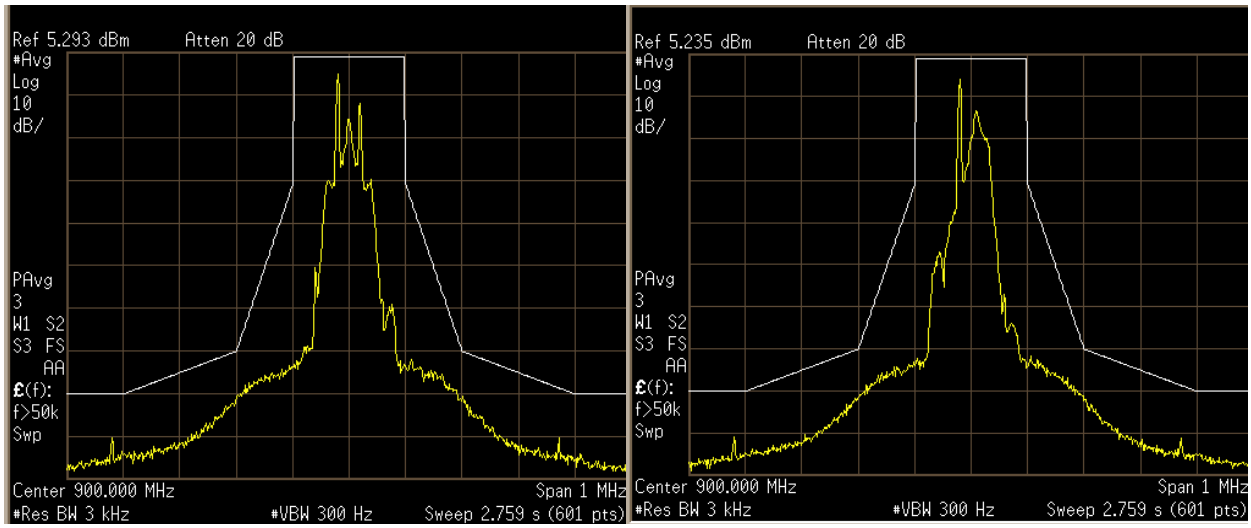


Figure 8-4: DSB-ASK, tari=12.5 µs, X=0.5 and 1.0

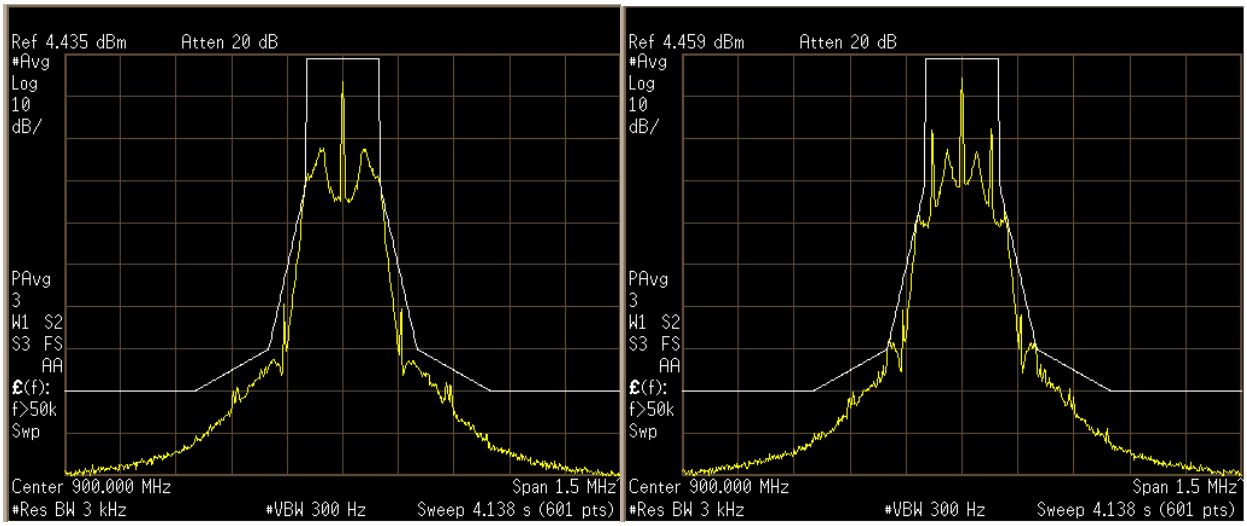


Figure 8-5: PR-ASK, tari=12.5 µs, X=0.5 and 1.0

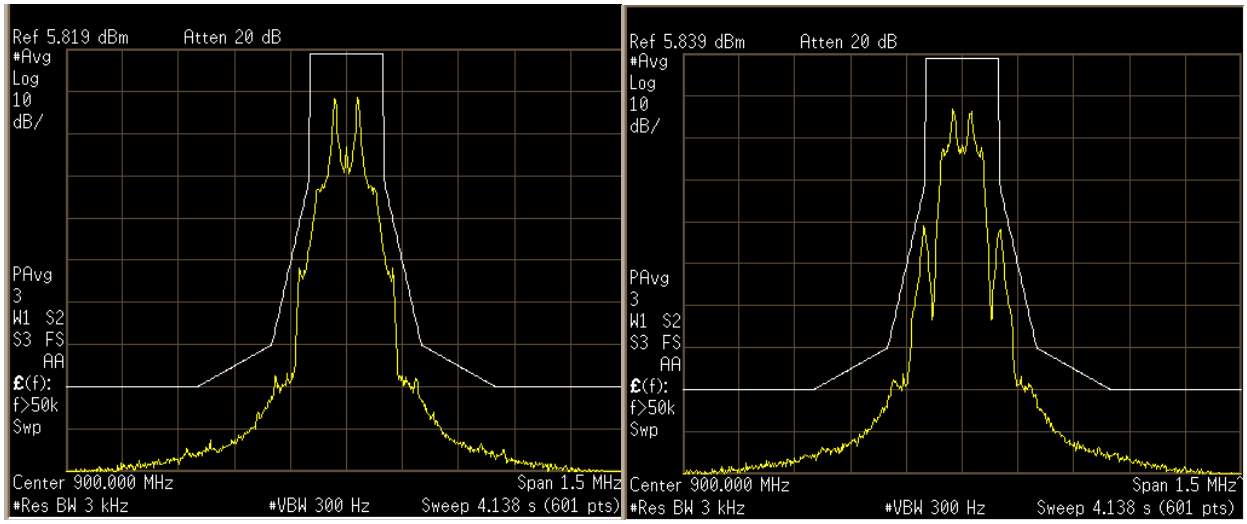


Figure 8-6: DSB-ASK, tari=6.25 µs, X=0.5 and 1.0

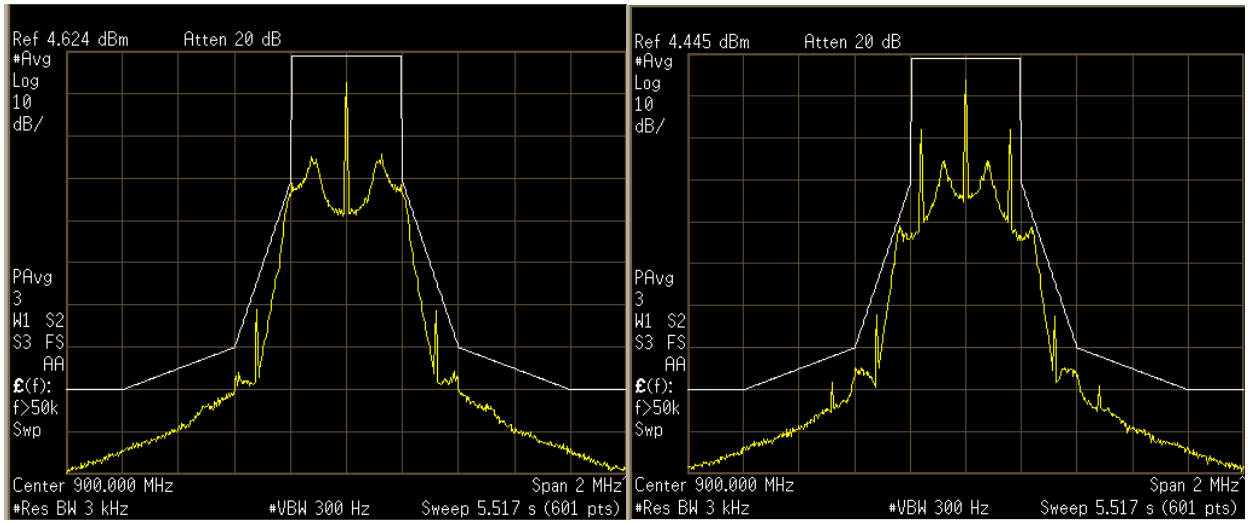


Figure 8-7: PR-ASK, tari=6.25 µs, X=0.5 and 1.0

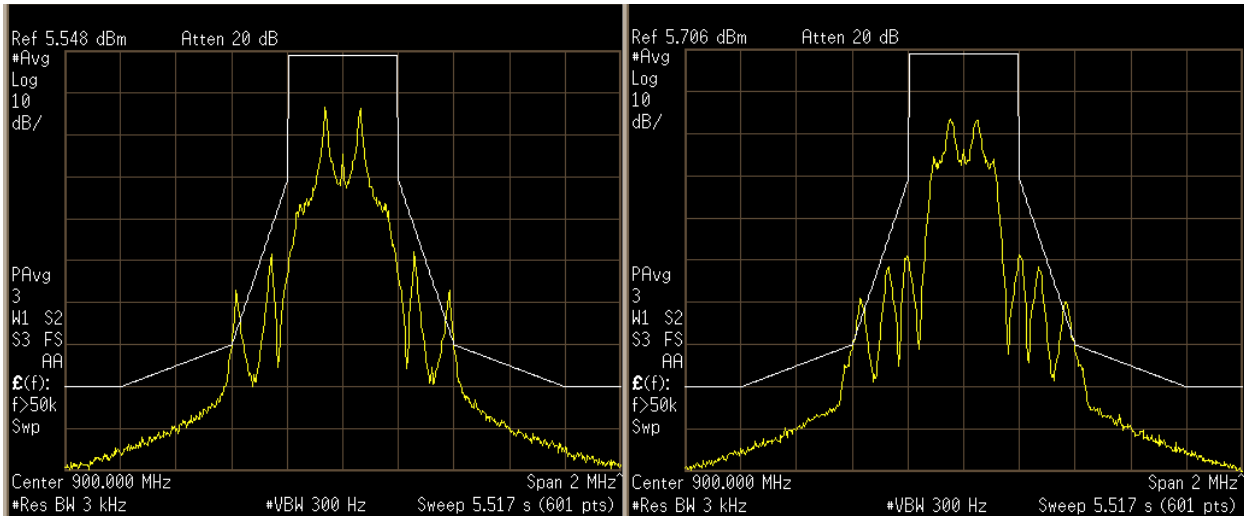
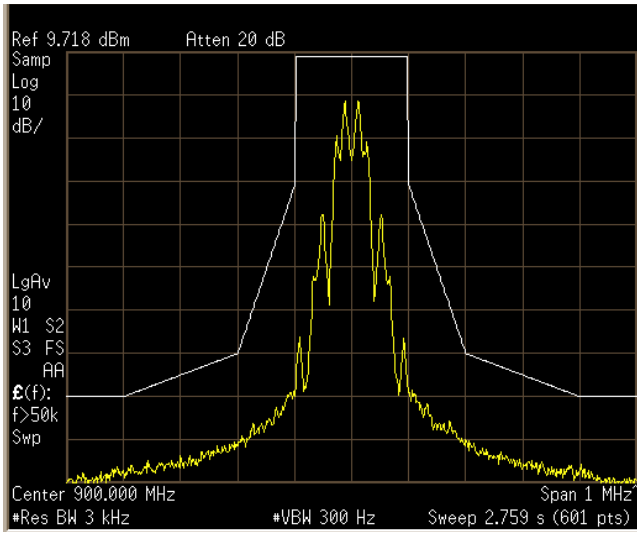


Figure 8-8: PR-ASK, tari=25 µs, X=1.0 turbo mode (+15 dBm CW power)



8.4 Analog (gross) power control

Figure 8-9 shows the output power versus the control state as defined in register 0x43F. The inter-stage matching (register 0x415) is adjusted for each frequency with values of 3, 4 and 7 for 860, 900 and 960 MHz, respectively. The approximate step of 2 dB of output power for each state is illustrated.

Figure 8-9: Output Power versus Analog Control State

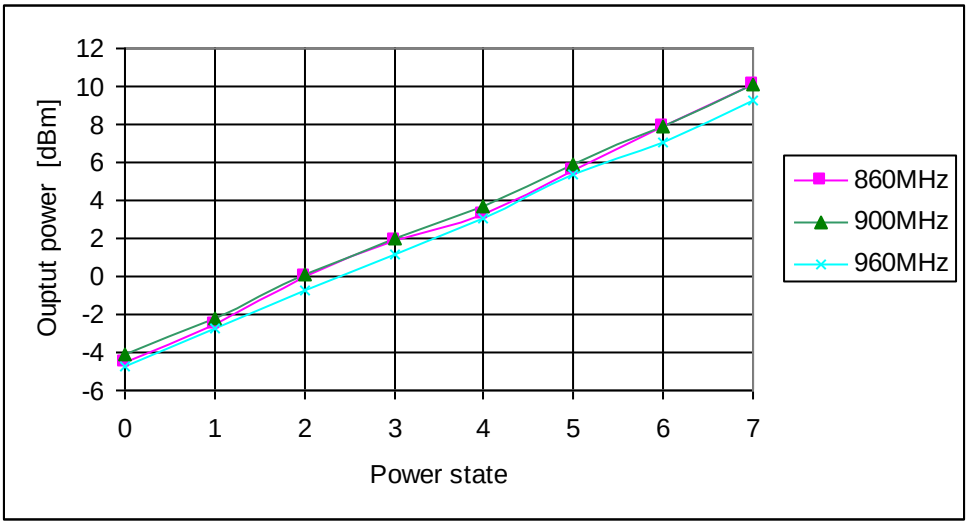
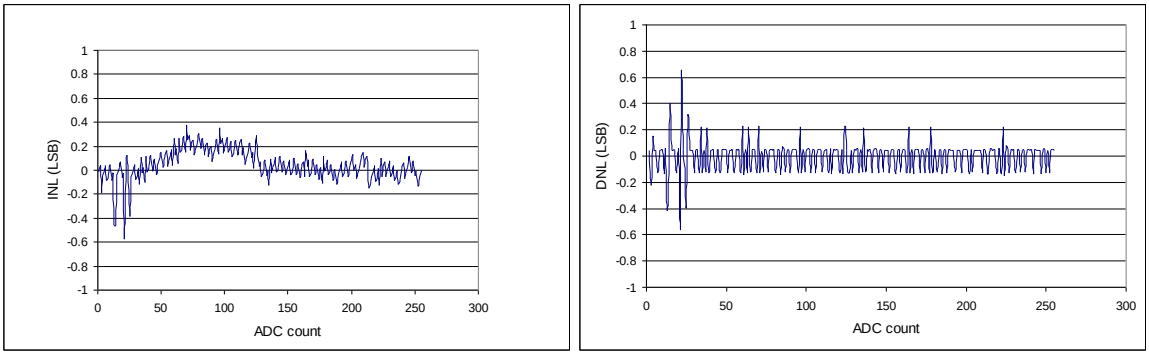


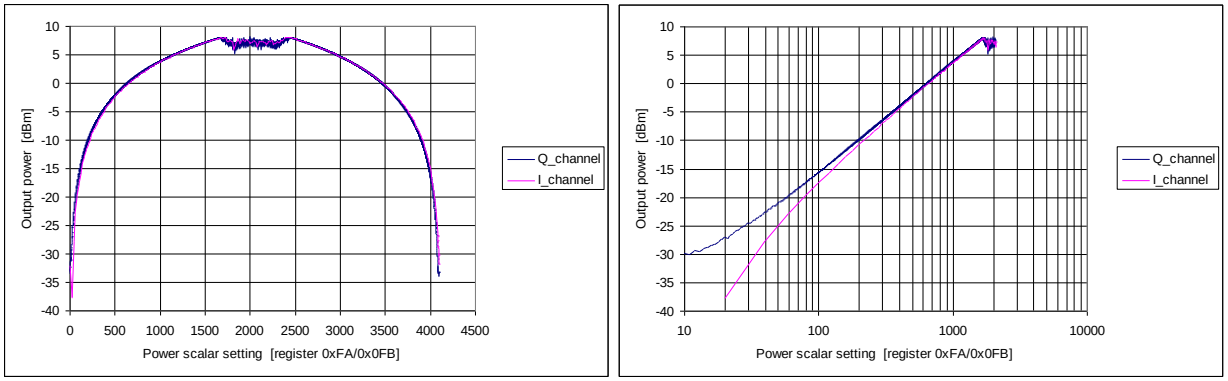
Figure 8-10: INL and DNL for Auxiliary ADC



8.5 Digital power control

Figure 8-11 shows the output power versus the power scalar setting set on registers 0x0FA and 0x0FB for the I and Q channel respectively. Plots in linear and logarithmic scale are shown. There is a 6dB pad at the output of the test board. A scalar value of 0x400 (1024-decimal) gives an output power of approximately +10dBm.

Figure 8-11: Output Power versus Scalar State



8.6 ADC Testing

Figure 8-12 shows the ADC count versus input voltage. Figure 8-13 shows the integral and differential non linearity.

Figure 8-12: ADC Count versus Input Voltage

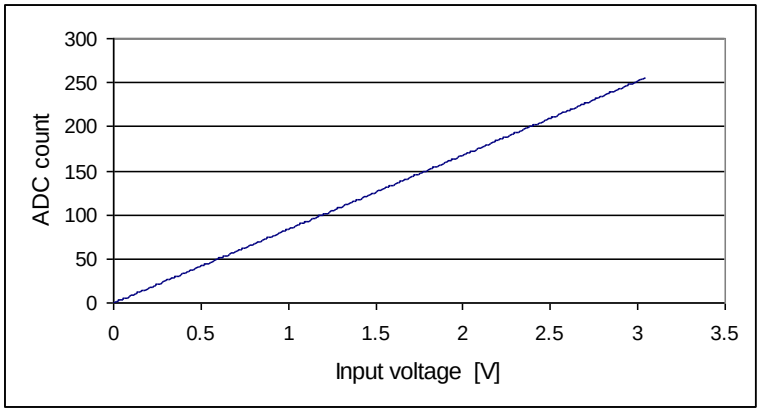
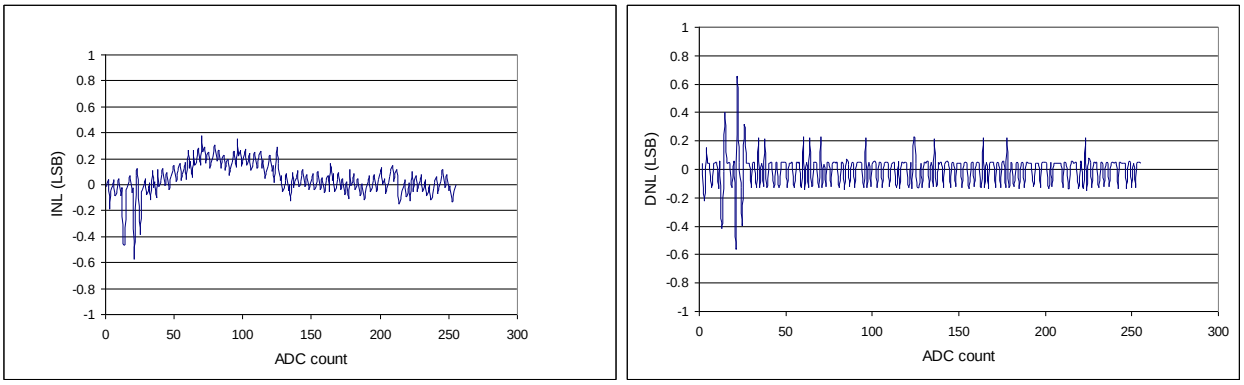


Figure 8-13: INL and DNL for Auxiliary ADC



8.7 Aux. DAC Testing

Figure 8-14 shows the output voltage plot for the auxiliary DACs. Figure 8-15 shows the integral and differential non linearity for both DACs. For both of these measurements the output of the DAC is loaded with a 500Ω load.

Figure 8-14: DAC0 and DAC1 Output Voltage versus Count

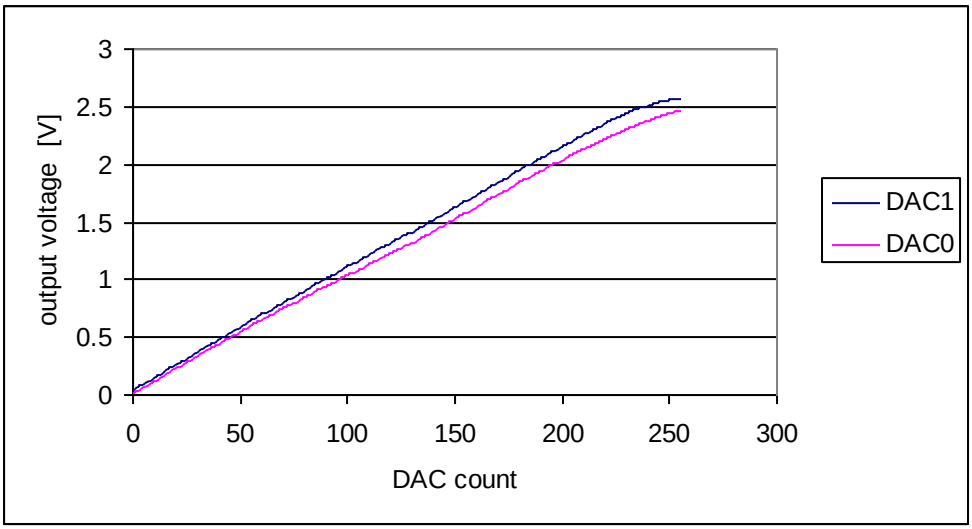
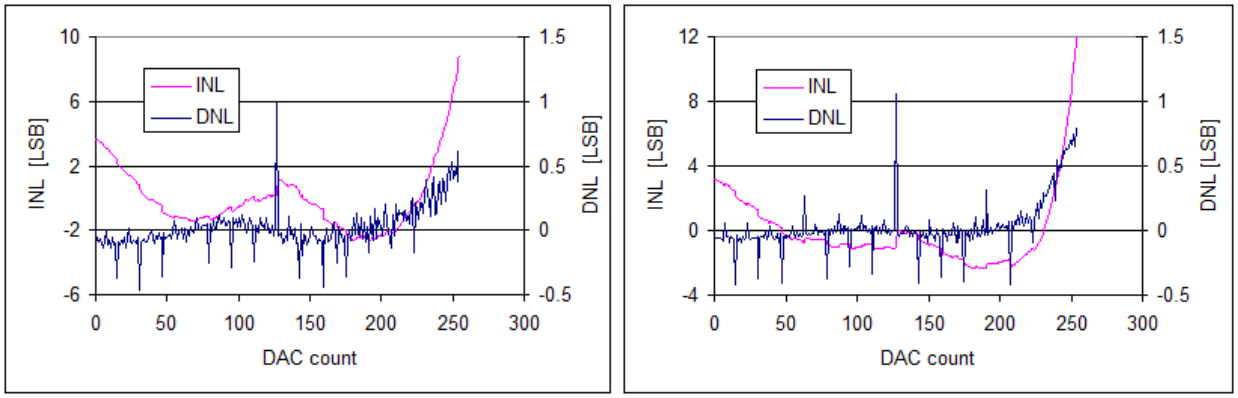


Figure 8-15: INL and DNL for DAC0(left) and DAC1(right)



9 Package Information

The Indy R2000 reader chip RFID Radio chip is packaged in a 64 pin, 9 mm x 9 mm x 0.85 mm, 0.50 mm pitch, quad flat no-lead (QFN) package. This product has a moisture sensitivity level of 3. Parts are delivered in “dry baked” trays. Parts from broken trays (open trays) or samples must be baked for 24hrs at 125C before soldering. Figure 8-16 illustrates the top view of the Indy R2000 reader chip package, and Figure 8-17 provides the dimensions for the package.

Figure 8-16: Indy R2000 Reader Chip Package Top View

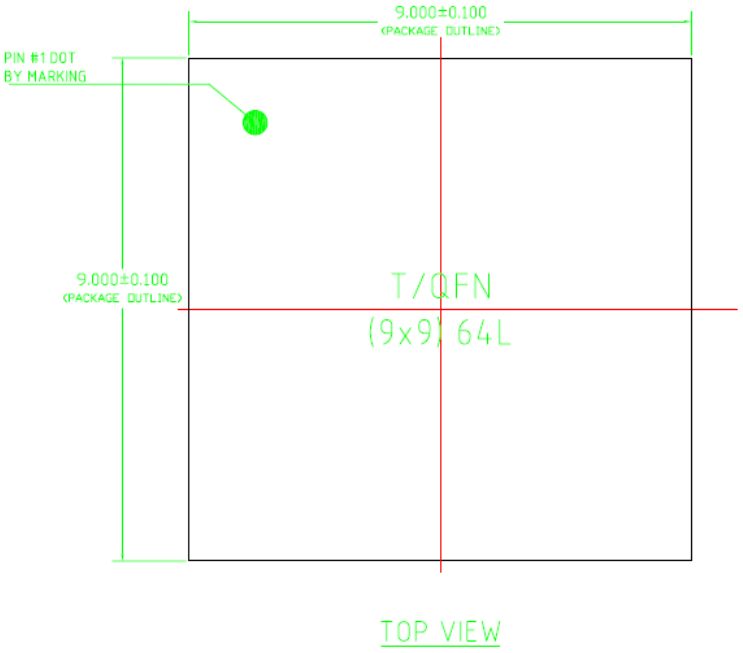
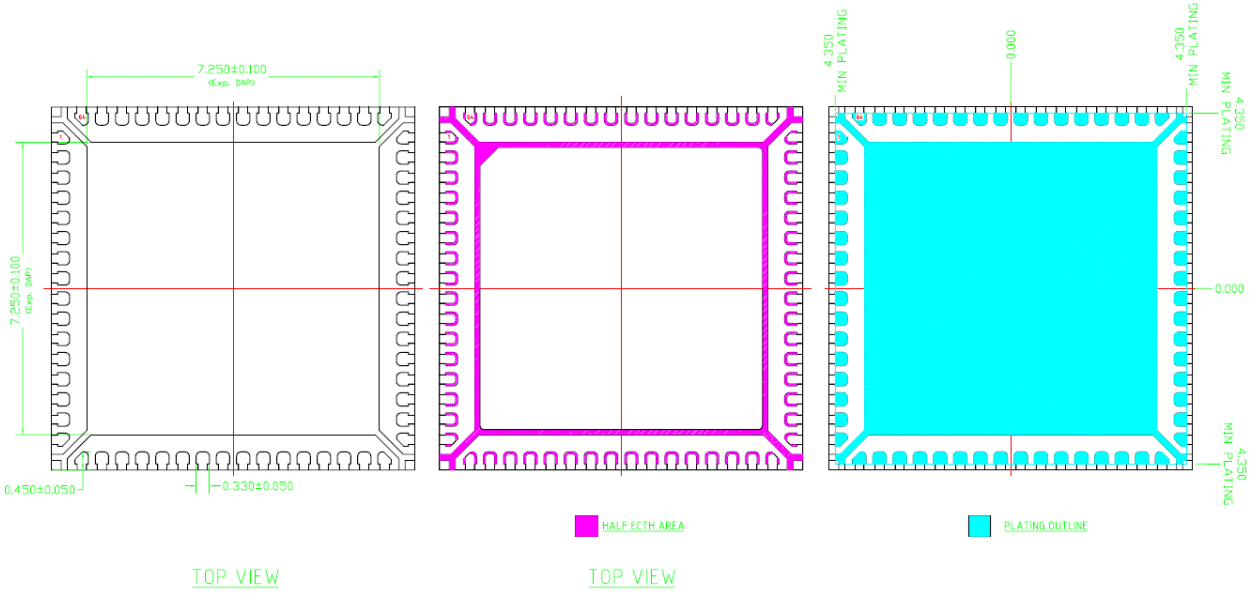


Figure 8-17: Indy R2000 Reader Chip Package Dimensions



10 Document Change Log

Table 10-1: Document Change Log

Version	Date	Description
1.0-1.4		Initial versions
2.0	7/30/2015	Formatting updated Diagrams updated RSSI register description updated Typos fixed

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