2023 EE5250 VLSI Design Homework 3

Due date:2023/11/30

**Set temperature = 25 degrees for TT corner during simulation.*
**The following should be included in your report: (a) picture of the schematic, (b) picture of the waveform with cursor values, (c) your comment*

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1. Run an inverter buffer (out = $\bar{in}$) with output loading 75pF with VDD = 1V, as shown in Fig 1. (The size of the first inverter has been assigned.) (the rising time and falling time of input is 0.01ns & input frequency = 5MHz).
   [Run with .18um technology and 14nm technology]

   (a) Please find the unit inverter, calculate the g and p and use the parameter to calculate the optimum ρ with the simulation result and your normalization condition. (10%) (Hint: use the skewed gate in Chapter 5)
   (b) Please design the size and stage of the inverter chain to reach tpdf and tpdr < 1ns. (tpdf and tpdr definition: Fig 2.) (10%)

   Connect the output of the inverter buffer back to the input to form the oscillation loop:
   (c) Calculate the oscillation frequency based on the simulated parameters. (5%)
   (d) Simulate the oscillation frequency. (10%)
   (e) What is the difference between (c) and (d), and comment on it. (10%)
   (f) Change the output loading to 120pF, fix the stage of the inverter chain, and compare the simulated oscillation frequency between the different output loading. (15%)

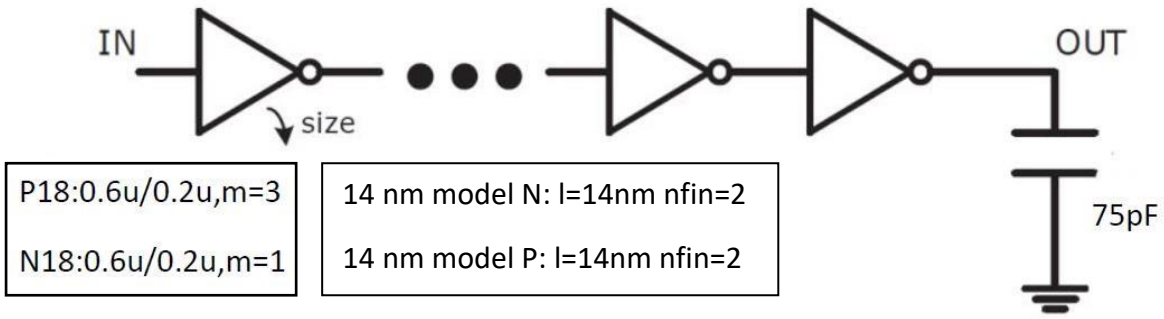

Fig.1

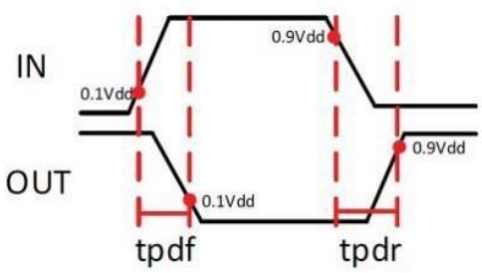

Fig. 2

2. Please design a 3-to-8 decoder with output loading 300fF at each output node (as shown in Fig. 2) and try to add an inverter buffer to **minimize the delay from input to output of the decoder**. VDD = 1.8V, and the size of the first inverter has been assigned. (the rising time and falling time of input A[0], $\bar{A}$ [0] is 0.01ns & input frequency = 20MHz, the rising time and falling time of input A[1], $\bar{A}$ [1] is 0.01ns & input frequency = 40MHz, the rising time and falling time of input A[2], $\bar{A}$ [2] is 0.01ns & input frequency = 80MHz) (60%)
[You only need to run with .18um technology]

   (a) Describe how you design the inverter buffer and the other device size in detail. (10%)
   (b) Finish the layout(whole circuit, from "A" to "Out"), DRC, and LVS. Paste the photo of the layout, DRC result, and LVS result in your report. Please mark the length and width on the layout and calculate the area(um^2). (15%)
   (c) Run the post-layout simulation and compare it with the pre-sim. (10%)

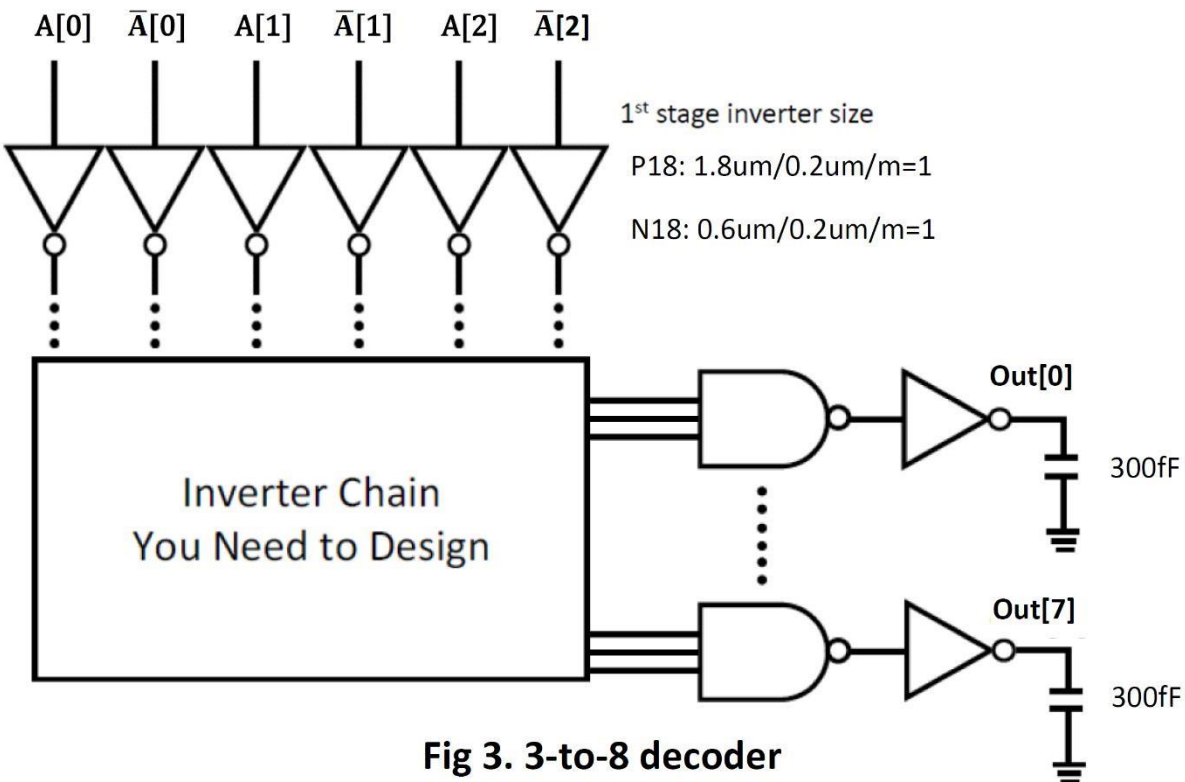

Fig 3. 3-to-8 decoder

➢Please submit homework in PDF format and turn it in on the eeclass system. You can finish this homework on handwriting paper and scan it into PDF format.

By CCHsieh