2023 EE5250 VLSI Final Project

Demo date:2024/1/18
Report submission date:2024/1/19

A Multi-Modulus Frequency Divider

I. Introduction

Dual modulus prescaler is an essential block in PLL (phase-locked loop) design. Take 8/9 dual modulus design for example. The block diagram and timing diagram are shown in Fig. 1. The ÷2/3 block is controlled by the control qualifier, where the control qualifier is the combinational logic controlled by the outputs (A, B, OUT) of each block. The ÷ 2/3 block enters into ÷3 mode as CON=1 which results in the OUT with divided 9 (=8+1) cycles. In contrast, it enters into ÷2 mode as CON=0 which results in OUT with divided 8 (=8+0) cycles.

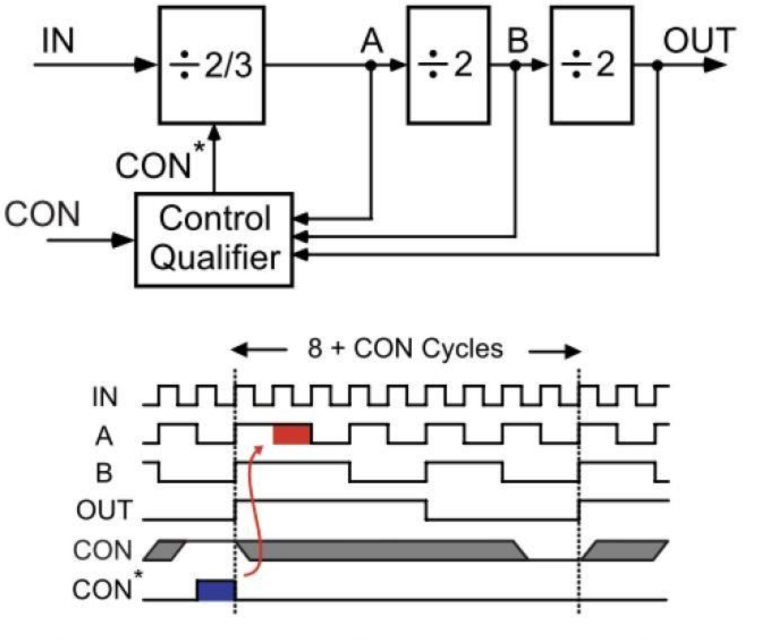

Fig. 1. The example and timing diagram of 8/9 dual modulus design.

II. Design Topic

Follow the same concept, please design a multi-modulus frequency divider with total **4 modes operation** $(\div 32/33/34/35)$, which is controlled by the signal CON_0, CON_1.The divided equation can be expressed as $(\mathbf{32+CON_0\times 2^0, CON_1\times 2^1})$, where the divided cycles is decided by $CON_{0\text{-}1}$.

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In this final project, the detail circuit implementation is "**free for design**." However, the number of I/O pin **is restricted to 1 input clock (CLK_{IN}), 2 control signals (CON_{0-1}) and 1 output clock (CLK_{OUT})** (see Fig. 2.) Your design should be verified from pre-sim to post-sim.

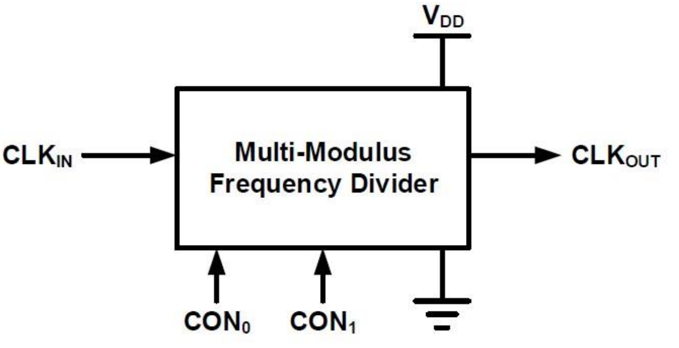

Fig. 2. The I/O description of the targeted design

III. Design Constraints

Power Supply

1. VDD = 1.8V (fixed)

Input

1. CLK_{IN}: the input clock with frequency defined by yourself
2. $CON_{0\text{-}1}$: digital control signals to choose modulo

Output

CLK_{OUT}: the output clock with frequency divided

Simulation Conditions for HSPICE

1. .option accurate = 1 runlvl = 5
2. transient simulation time resolution: (1/1000)*(1/fmax), fmax is the maximum frequency of CLK_{IN}.
3. Corner specification
   - TT：25 ℃
   - FF：-40 ℃
   - SS：125 ℃
   - SF：25 ℃
   - FS：25 ℃

Layout

1. Aspect ratio of full circuit block: 1 < (long side/short side) < 2

2. The total area is not limited

IV. Report

Block Diagram

1. Draw top view of your system design and explain why you choose this architecture and how your design operated.
2. Draw sub-block in gate level and transistor level hierarchical and explain why you use them.

Layout

1. Print-screen the whole design (with size & area) and sub-blocks.
2. DRC summary with no error (excluding the optional rules).
3. LVS report.

Simulation Results

1. Pre-sim results & post-sim results, need to compare and explain the difference between them.
2. Waveforms (cursor is needed) and tables (filled with measured data) for all modulus modes.

V. Demo

1. The demo session will be held at EECS-R407 on 2024/01/18, to be debated (follow the notice on eeclass)
2. Explain to TAs about why you choose this architecture and how your design operating.
3. Show DRC/LVS/PEX and then the pre-sim and post-sim for **4-different results**.
4. The best specification is required to be showed at demo day, the grading of your specification depends on the demo results. The data in your report should be matched to the results of demo day.

VI. Grading

Demo (70%, no show, no points)

1. Layout (10%)
    a. Completeness (5%)
    b. Aspect ratio (5%)
2. DRC (10%): No points if there are some errors.
3. LVS (10%): No points if there are some errors.
4. Waveforms: Check the functionality with all corners.

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a. Pre-sim (10%)

b. Post-sim (10%)

5. Specification table with all corners

a. Pre-sim (10%)

b. Post-sim (10%)

6. Power

7. fmax: Maximum frequency of CLK_{IN}

Report (30%)

1. Block diagram (5%)
2. Layout (5%)
3. Simulation Results (5%)
4. Spec table and your comments (15%)

< Pre-sim >

Corner	fmax	Power_div16	Power_div17	Power_div18	Power_div19
TT					
SS					
FF					
SF					
FS					

< Post-sim >

Corner	fmax	Power_div16	Power_div17	Power_div18	Power_div19	Area	FoM
TT							
SS							
FF							
SF							
FS							

Competition for Bonus

1. f_{max} of CLK_{IN} @ TT post-sim (4% for #1, 3% for #2, 2% for #3, 1 % for #4~10)
2. Area (4% for #1, 3% for #2, 2% for #3, 1 % for #4~10)
3. FoM = $\frac{f_{max}}{Power \times Area}$ (unit: GHz/(W*um2)) @ TT post-sim

(4% for #1, 3% for #2, 2% for #3, 1 % for #4~10)

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