超大型積體電路設計

VLSI Design

Homework I

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1. Run simulation to answer the following question. (40%)

(a) Please design a INVERTER schematic with $(W/L)n$ = 1μm/0.18μm while $(W/L)p$ is your design. Design the transfer curve according to Fig. 1 with $VDD = 1V$ and transition point $VM = 0.5VDD$. ($Vout = 0.5VDD@Vin = 0.5VDD$) in 3 process corner. (TT, SS, FF) Please print out both input and output waveforms in each condition.

Corner	PMOS size (W/L)
TT	5.4u/180.0n
SS	4.4u/180.0n
FF	5.4u/180.0n

Table 1 180nm size

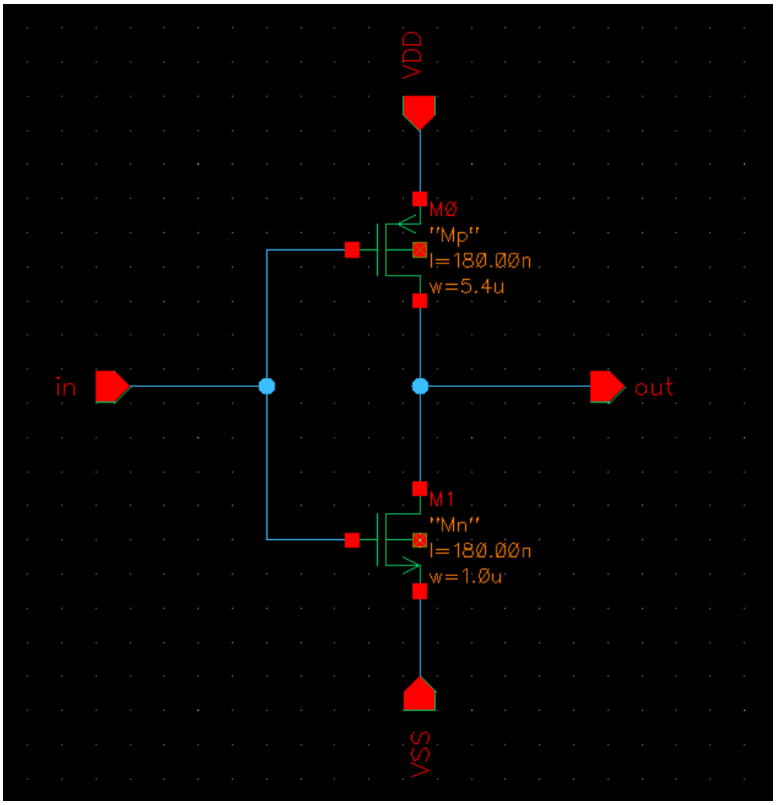

Figure 1 180nm Inverter schematic

I. TT

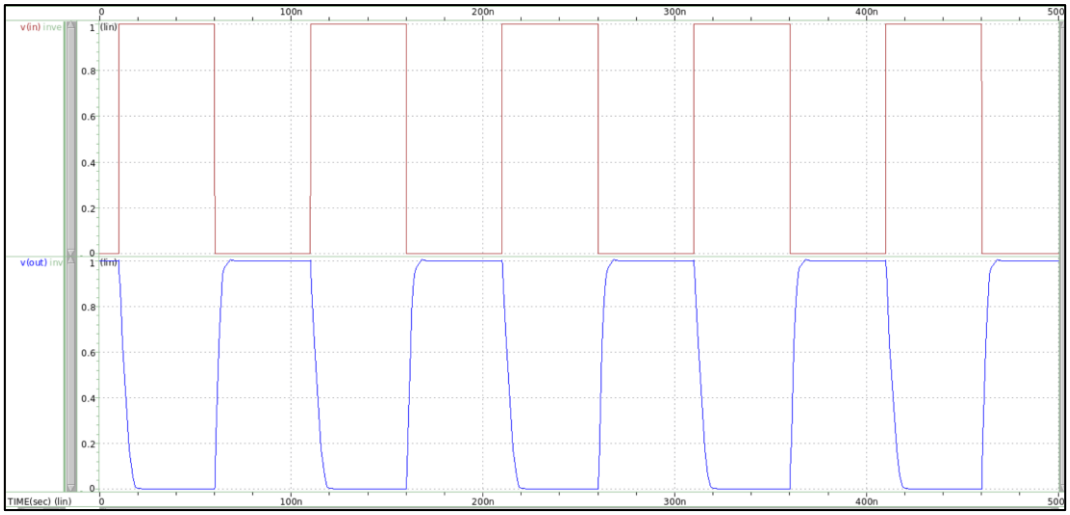

Figure 2 TT inverter pulse waveform (add 1pF capacitance)

Vin =500mV
Vout=504mV

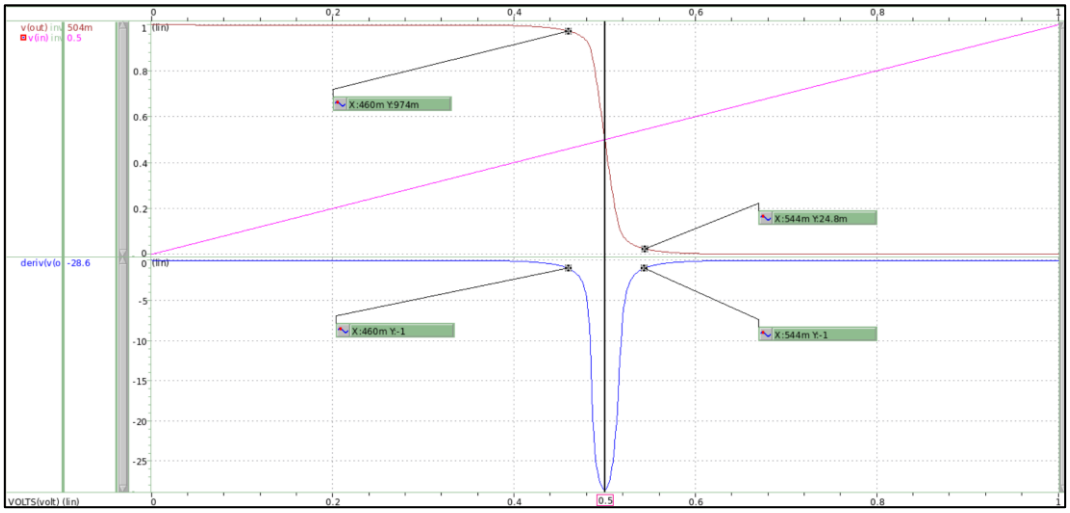

Figure 3 TT inverter VTC

II. SS

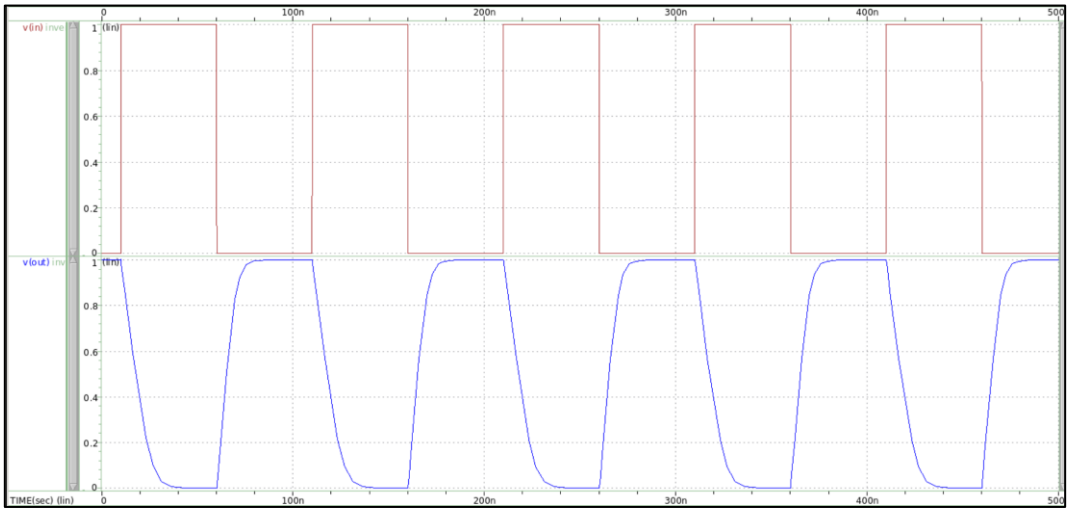

Figure 4 SS inverter pulse waveform (add 1pF capacitance)

Vin =500mV
Vout=496mV

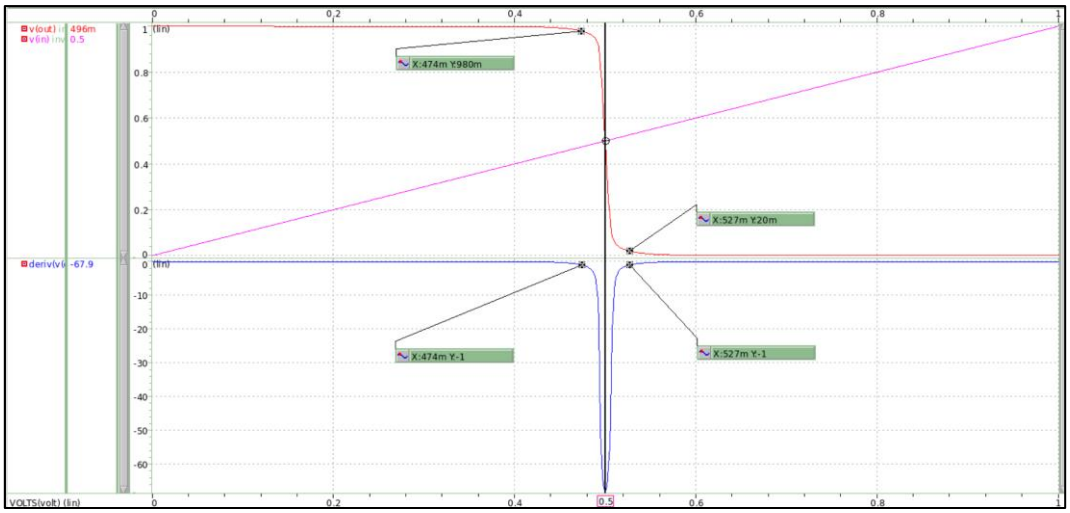

Figure 5 SS inverter VTC

III. FF

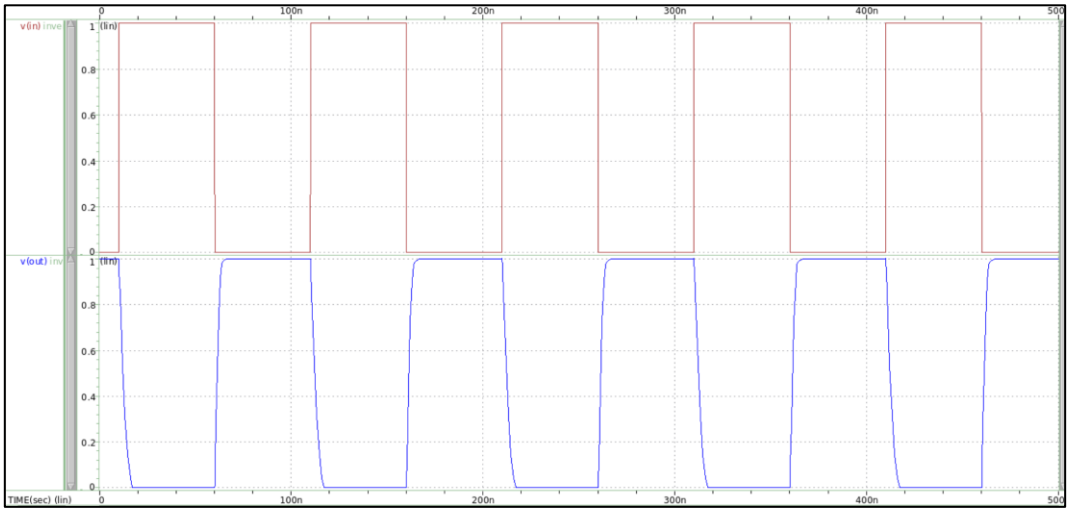

Figure 6 FF inverter pulse waveform (add 1pF capacitance)

Vin =496mV
Vout=504mV

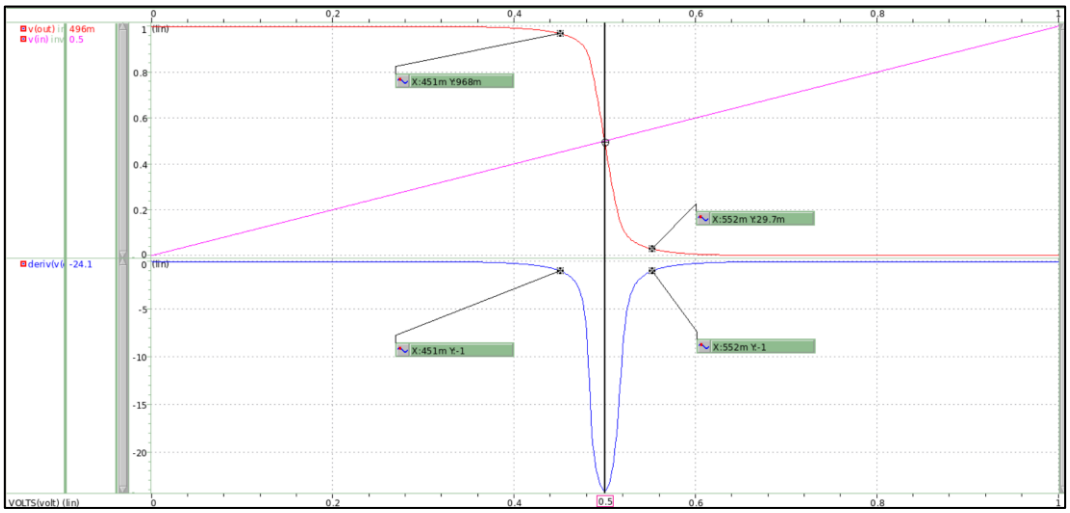

Figure 7 FF inverter VTC

(b) Comment on the different PMOS size in each corner.

TT : Black
SS : Blue
FF : Red

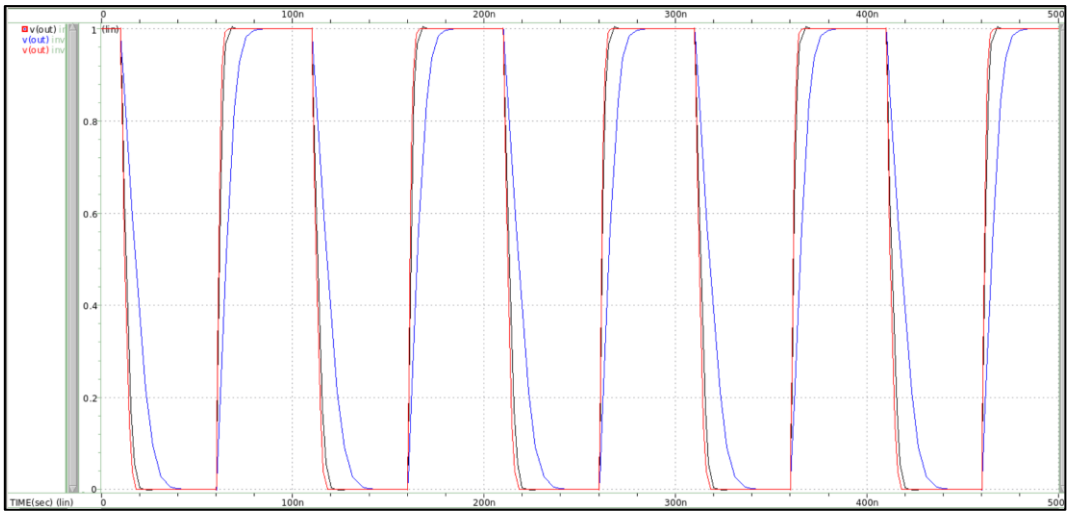

Figure 8 Compare pulse waveform (add 1pF capacitance)

TT : Black
SS : Blue
FF : Red

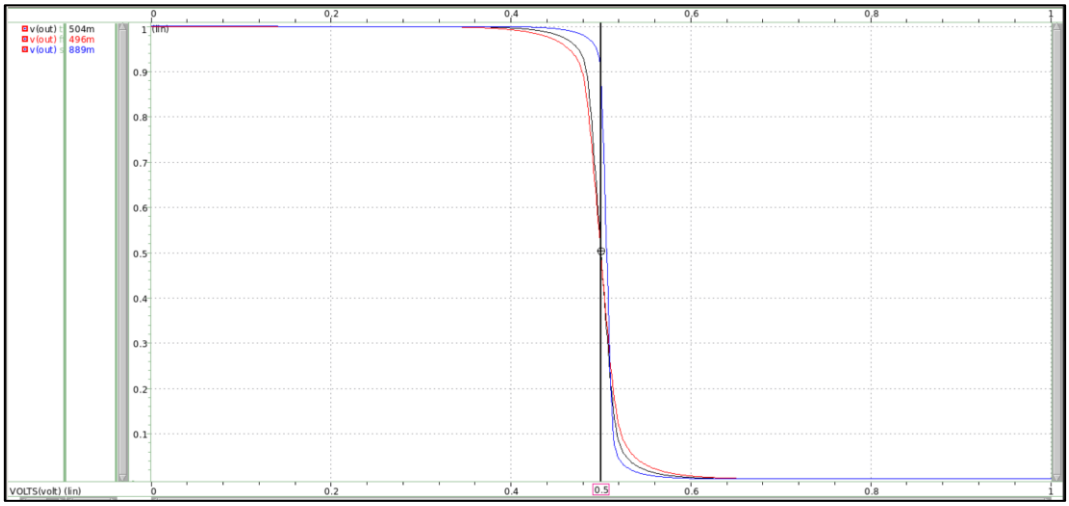

Figure 9 Compare VTC(Before modify pmos size)

TT : Black
SS : Blue
FF : Red

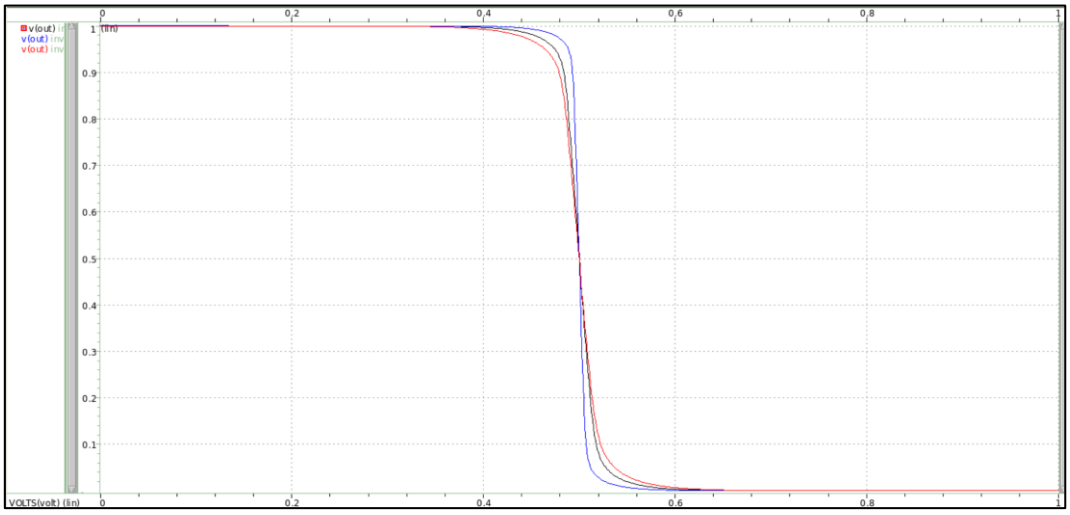

Figure 10 Compare VTC(After modify pmos size)

TT,SS,FF 為 NMOS 與 PMOS 的切換速率，由 Figure 8 可知 TT 的 waveform 會界在兩者之間，SS 電壓上升較慢，FF 則較快，在 SS 時模擬元件在低電壓高溫時速度下降的現象，如果使用和 TT 相同的 PMOS size 結果顯示如下圖 Figure11，vout 的曲線往右平移了，這表示 PMOS 的電流太大，所以要將 PMOS 的 size 調小，才能符合題目需要的 Vm=0.5Vdd，而 FF 在模擬的結果顯示在與 TT 相同的 PMOS size 下，結果是相近的。

Vin =500V
Vout=889mV

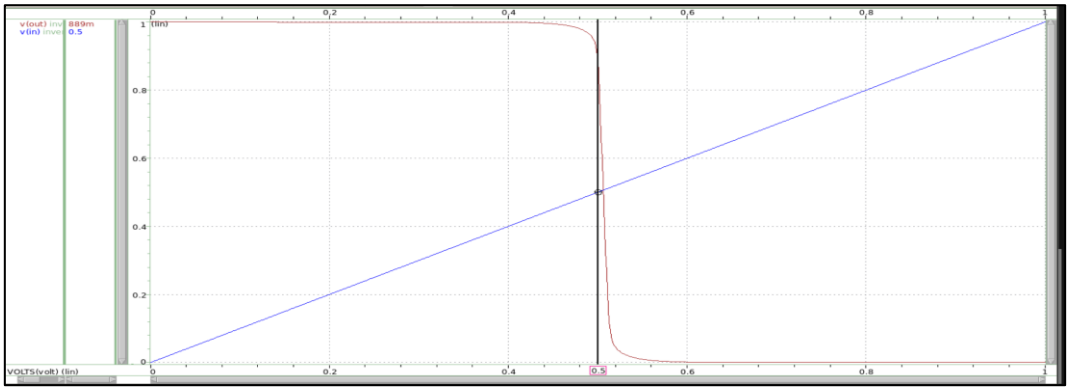

Figure 11 180nm Inverter SS_corner_VTC(Pmos size 4.4u/180.0n)

2. Run simulation to answer the following question. (40%)

(a) Please design a INVERTER schematic with length=14nm while nfinn and nfinp are your design. Design the transfer curve according to Fig. 1 with $VDD = 0.8V$ and transition point $VM = 0.5VDD$. ($Vout = 0.5VDD@Vin = 0.5VDD$) in 3 process corner. (TT, SS, FF) Please print out both input and output waveforms in each condition.

Corner	$nfin_n$	$nfin_p$
TT	2	2
SS	6	5
FF	2	2

Table 2 14nm size

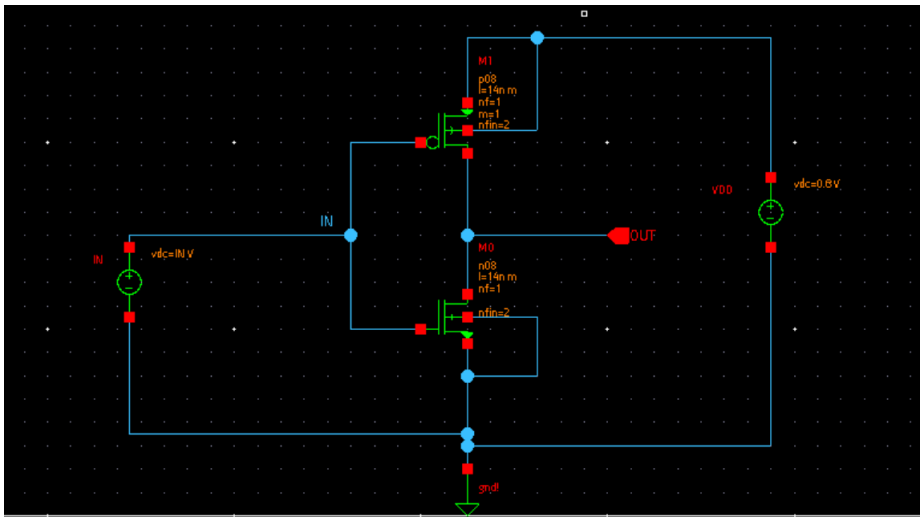

Figure 12 14nm Inverter schematic

I. TT

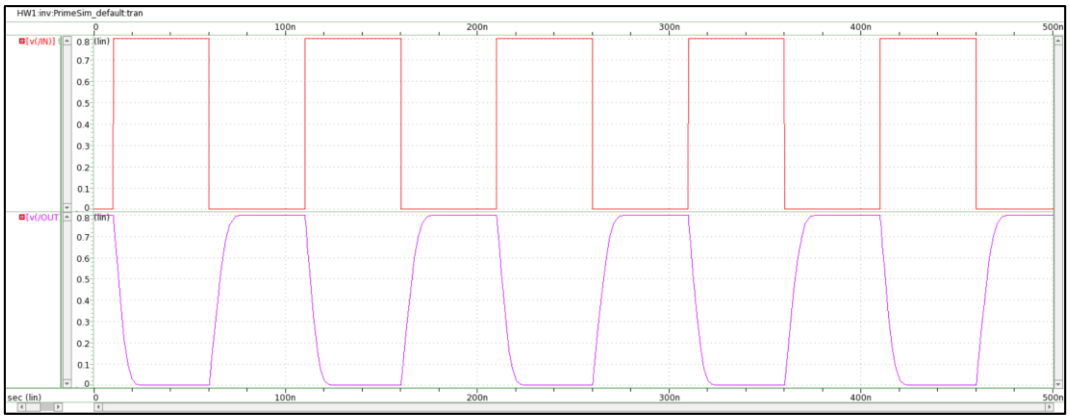

Figure 13 TT inverter pulse waveform (add 1pF capacitance)

Vin =400mV
Vout=425mV

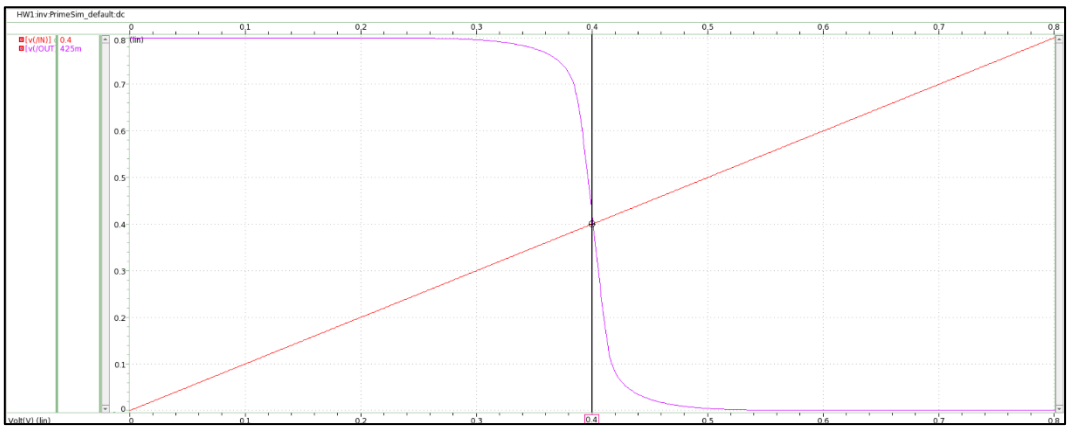

Figure 14 TT inverter VTC

II. SS

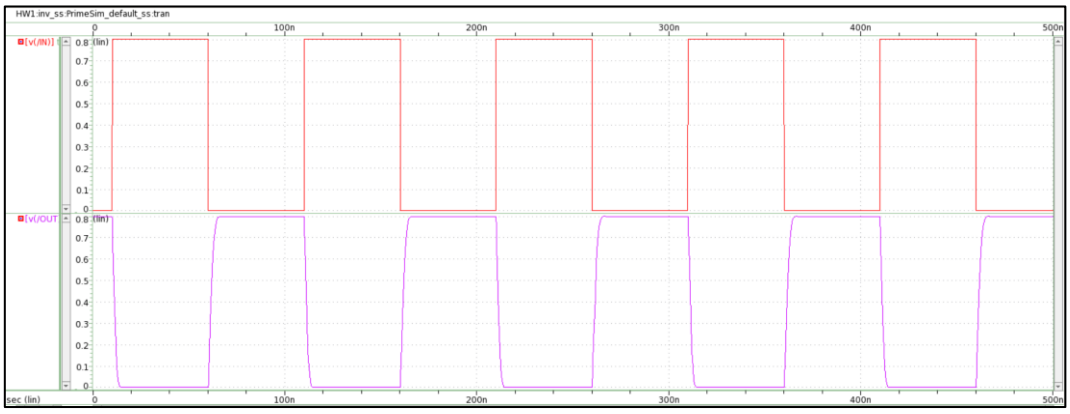

Figure 15 SS inverter pulse waveform (add 1pF capacitance)

Vin =400mV
Vout=407mV

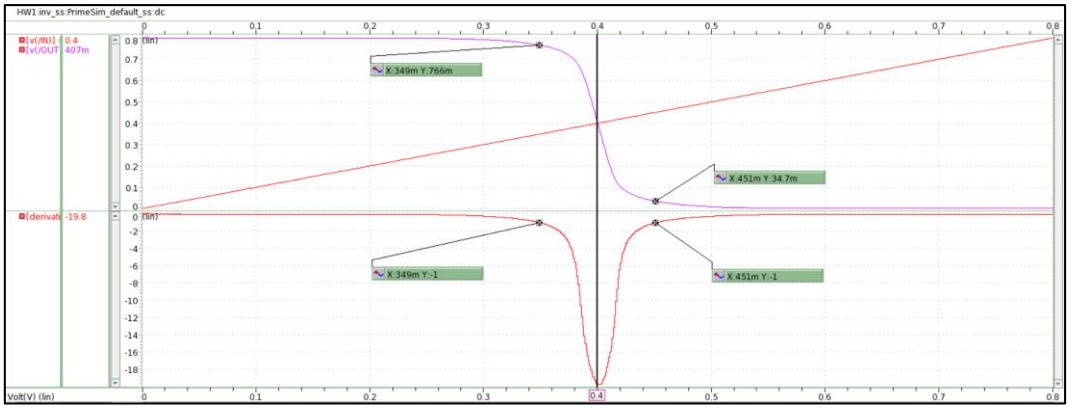

Figure 16 SS inverter VTC

III. FF

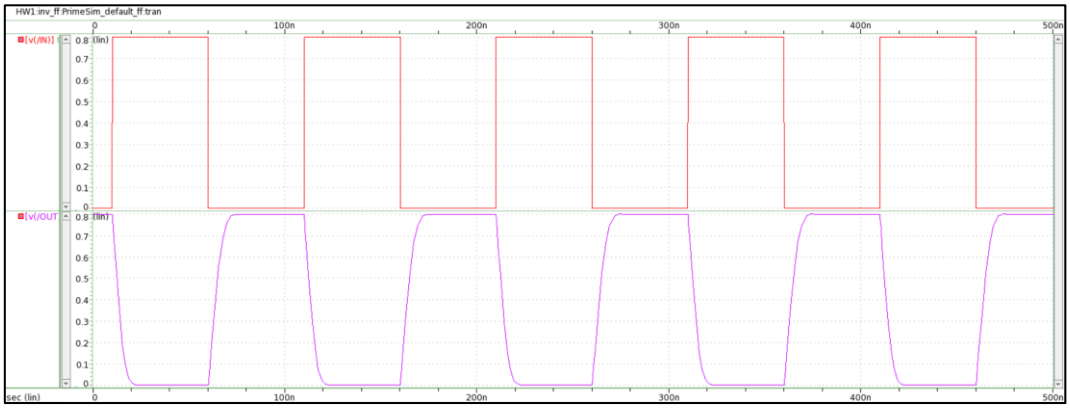

Figure 17 FF inverter pulse waveform (add 1pF capacitance)

Vin =400mV
Vout=414mV

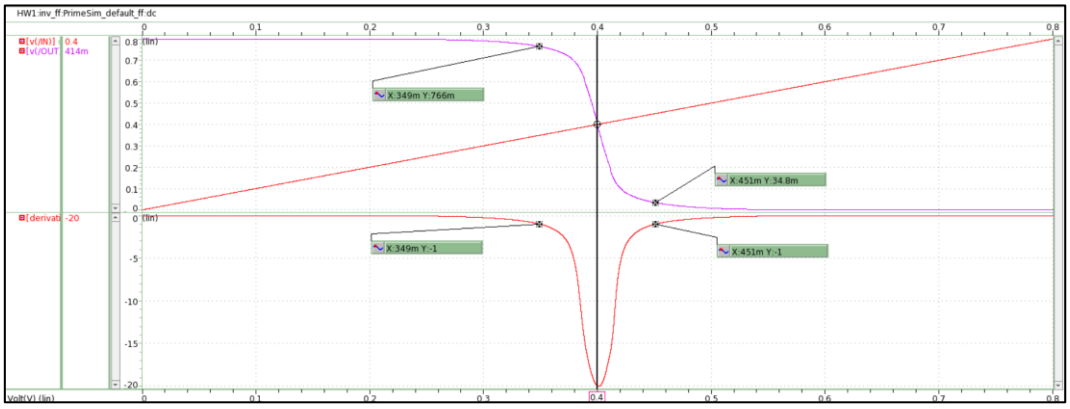

Figure 18 SS inverter VTC

(b) Comment on your design in each corner.

TT : Black
SS : Blue
FF : Red

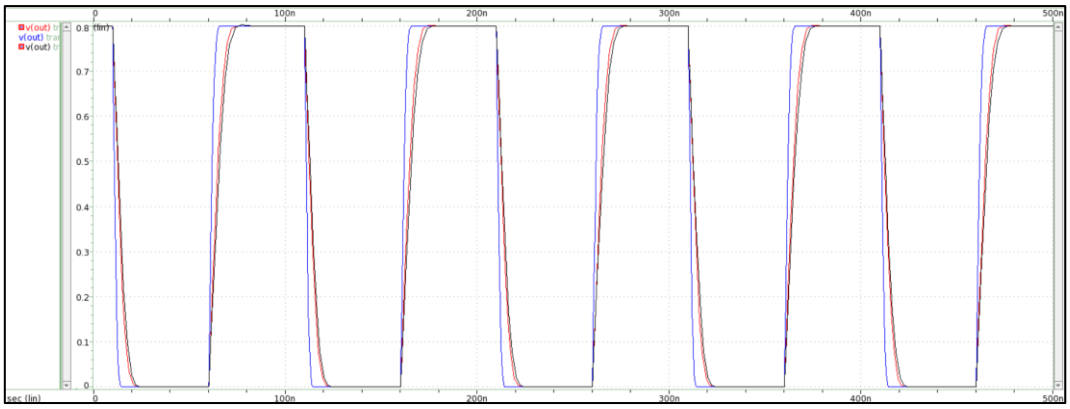

Figure 19 Compare pulse waveform (add 1pF capacitance)

TT : Black
SS : Blue
FF : Red

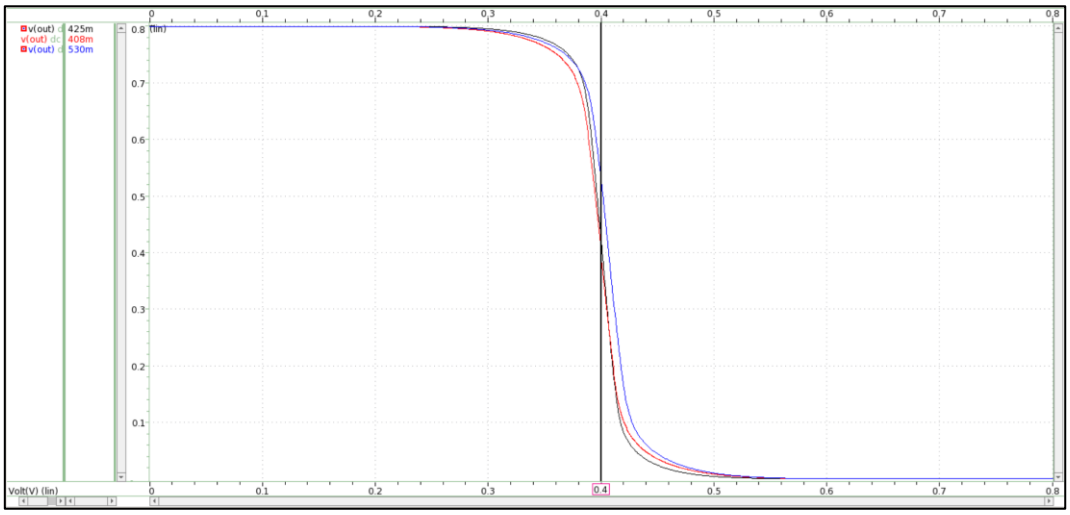

Figure 20 Compare VTC(Before modify pmos size)

TT : Black
SS : Blue
FF : Red

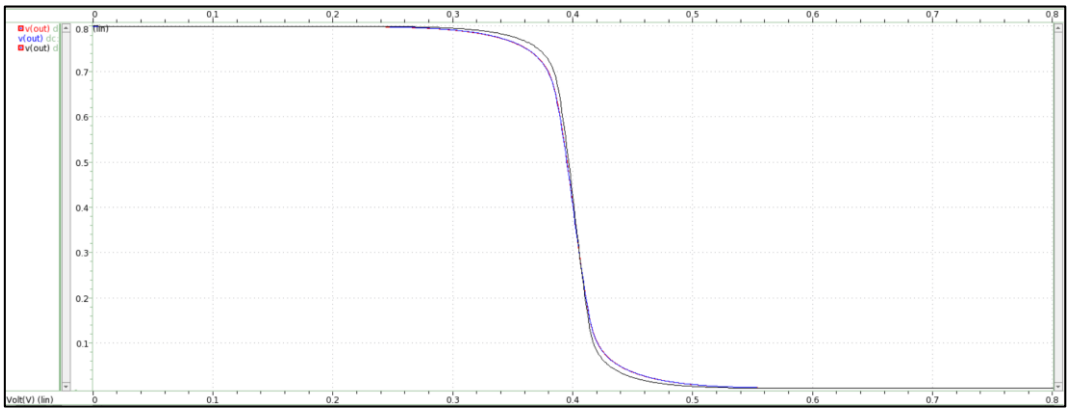

Figure 21 Compare VTC(After modify pmos size)

由 Figure20 可知 TT 和 FF 的 VM 值是接近的，但因為 FF 開關速度較快，溫度低，電流較小，所以 slope 較小，在 nmos 導通時的曲率較小，相反的 SS 開關速度較慢，溫度高，電流較大，所以 slope 較小。

3. Compare the result of two different process. (20%)

因使用 14nm 的製程可調整的是 fin 的數量，所以在調整 Vm 時會較難將數值調整到接近的值，從 Figure 8 和 Figure 18 的比較可以發現在 180nm 時，inverter 在 FF corner 可以達到較佳的輸出波型，而 14nm 的則相反，在 SS corner 的輸出波型較較還原輸入，由此推測，較大的製程下，元件需要在高電壓、低溫運作，而製成縮小後變成在低電壓、高溫時有較佳的效能。

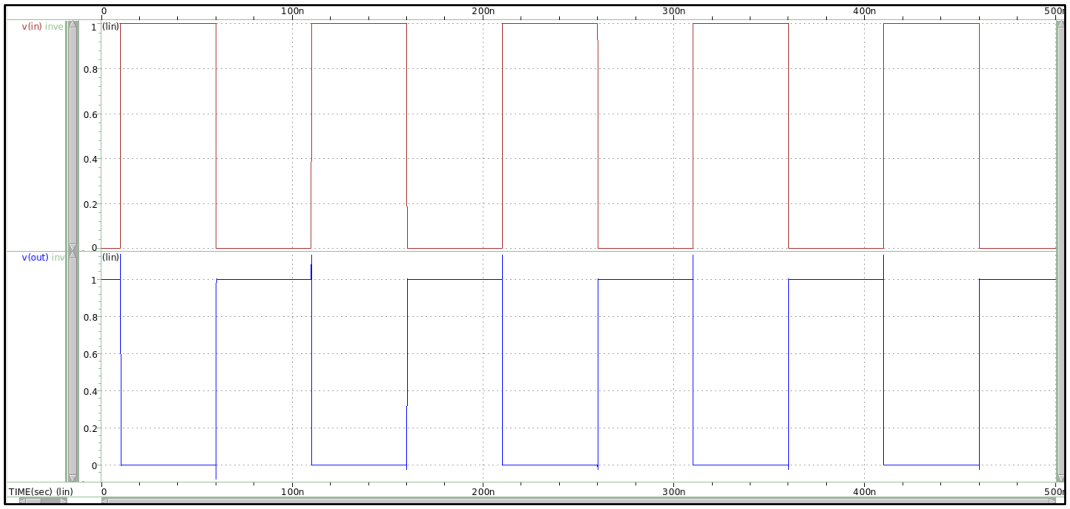

Figure 22 No capacitance 180nm Inverter

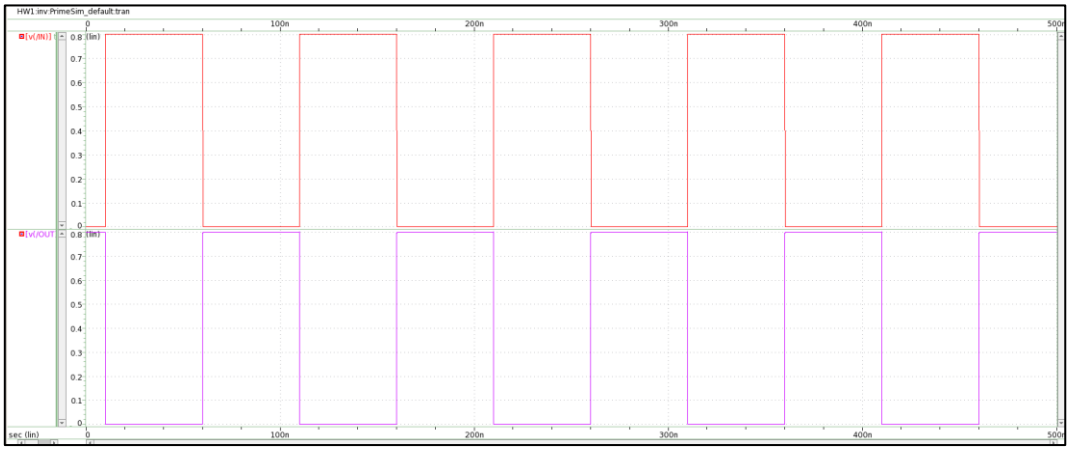

Figure 23 No capacitance 14nm Inverter

Figure21 是將 inverter 的輸出電容拿掉的情況，可以發現在上升下降時會有突波產生，原因可能是因為 t_{pHL} 和 t_{pLH} 的時間不足所造成的，或是在沒有電容的情況下，變成 mos 內部的小電容在反相時的電壓造成的突波，mos 中影響通道的電容可以可以分成 Cox 和 Cj，在導通時兩者串連形成。

Figure 24 與 180nm 不同的是，在沒加入電容時 14nm 沒有在反相時有突波的現象，我推測可能是製程下降，使 Cox 或是 Cj 下降，使電容的效應較不明顯。