2023 EE5250 VLSI Design Homework 2

Due date:2023/11/09

1. Please use the combination of CMOS to sketch the **transistor-level schematic** and **stick diagram** of the following compound gate function from those inputs A, B, C and D. (20%)

   (a) Y = A·B·C+D
   (b) Y = (A+B)·(C+D)
   (c) Y = A·C+B·C'
   (d) Y = A⊕B⊕C, ⊕ stands for XOR gate

   <Notice>
   You can try to simplify the function first. Please use different color or pattern to represent different layers, and to mark or use legend to explain which color representing which layer.

   <Grading Guideline>
   10% for each question
   - 4% for transistor-level schematic
   - 5% for stick diagram
   - 1% for your comments.

2. Based on problem 1(a),1(b), **please finish DRC and LVS verification**. You must attach the pictures on your report which contain layout, DRC result and LVS result. (20%)

   <Notice>
   $(W/L)_P$=3u/0.18u
   $(W/L)_N$=1u/0.18u V_{DD}=1.8V

   <Grading Guideline>
   - 8% for layout schematic (4% for each)
   - 8% for DRC correct results (4% for each)
   - 8% for LVS correct results (4% for each)
   - 16% If meet minimum DRC rules (8% for each)
   - 10% Explain what DRC rules do you learn, please list them.
     - Examples:
       What's the minimum distance between metal and metal?
       What's the minimum distance required for poly to exceed active region?

3. Run simulation to answer the following question.
   Using the two transfer curve you simulated under 180nm and 14nm process respectively in HW1, calculate the value of V_{IL},V_{IH}, V_{OL},V_{OH} and NM_H and NM_L in 3 process corners (TT, SS, FF). Please comment on the differences. (30%)

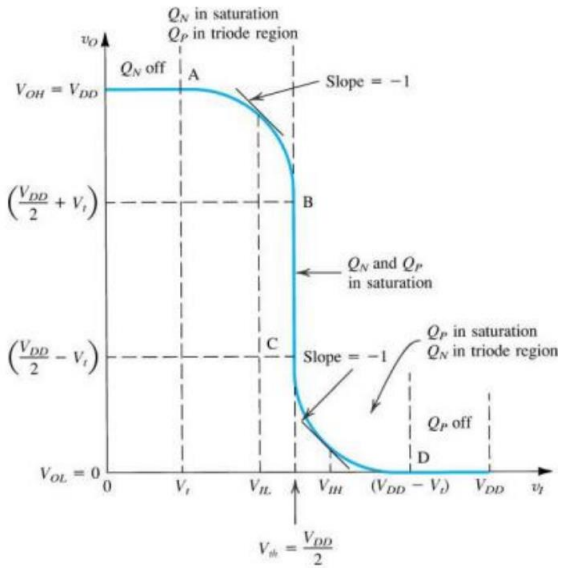

Figure 1

4. Run simulation to answer the following question, use V_{DD} = 1V. (30%)
   (a) Please design two 2-input NAND gate. One design with (W/L)n = 3μm/0.2μm and (W/L)p = your design, the other design with L=14nm, $nfin_n$ and $nfin_p$ = your design. Connect the two input together to run the transfer curve, the transition point should be Vout = 0.5V_{DD}@Vin = 0.5V_{DD} (Only in TT corner). (15%)
   (b) Using the 2-input NAND designed in (a) with V_{DD} = 1V.
   Input signal (A or B) = 0V - 1V @ 2MHz with rising time / falling time =0.1ns and a loading capacitor Cload = 1.5pF at output.

	Case 1			Case 2		
Input A	CLK			1V		
Input B	1V			CLK		
Corner	TT	SS	FF	TT	SS	FF
t_{pHL}						
t_{pLH}						
t_r						
t_f						

Table. 1

Change one input from 0V to 1V at a time and fix another one (See Table. 1).
Run HSPICE transient simulation of 2 cases at 5 corners and find the following values. Please comment on the differences. (15%)
t_{pHL} (from input to falling output crossing 0.5V_{DD})
t_{pLH} (from input to rising output crossing 0.5V_{DD})
t_r (from output crossing 0.2V_{DD} to 0.8V_{DD})
t_f (from output crossing 0.8V_{DD} to 0.2V_{DD})

➢ Please submit homework in PDF format and turn in it on eeclass system. You can finish this homework in handwriting paper and scan it into PDF format.

By CCHsieh