2023 EE5250 VLSI Design Homework 1

Due date:2023/10/19

∗ The following should be included in your report:
(a) picture of schematic
(b) 0.18um/14nm HSPICE netlist & simulation file (in form of attached file, no waveform file)
(c) picture of waveform with cursor values
(d) your comment

1. Run simulation to answer the following question. (40%)
(a) Please design a INVERTER schematic with $(W/L)n$ = 1μm/0.18μm while $(W/L)p$ is your design. Design the transfer curve according to Fig. 1 with $V_{DD} = 1V$ and transition point $V_M = 0.5V_{DD}$. ($V_{out} = 0.5V_{DD}@V_{in} = 0.5V_{DD}$) in 3 process corner. (TT, SS, FF)
Please print out both input and output waveforms in each condition.
(b) Comment on the different PMOS size in each corner.

corner	PMOS size (W/L)
TT	
SS	
FF	

2. Run simulation to answer the following question. (40%)
(a) Please design a INVERTER schematic with length=14nm while $nfin_n$ and $nfin_p$ are your design. Design the transfer curve according to Fig. 1 with $V_{DD} = 0.8V$ and transition point $V_M = 0.5V_{DD}$. ($V_{out} = 0.5V_{DD}@V_{in} = 0.5V_{DD}$) in 3 process corner. (TT, SS, FF)
Please print out both input and output waveforms in each condition.
(b) Comment on your design in each corner.

corner	$nfin_n$	$nfin_p$
TT		
SS		
FF		

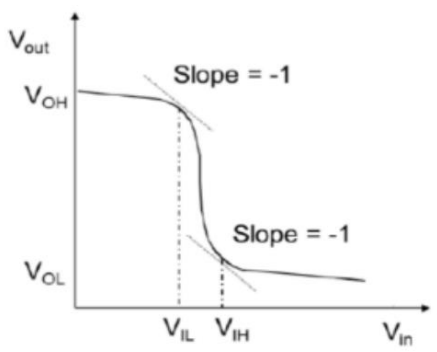

Fig. 1

3. Compare the result of two different process. (20%)

By CCHsieh