

超大型積體電路設計

VLSI Design

Homework III



國立清華大學

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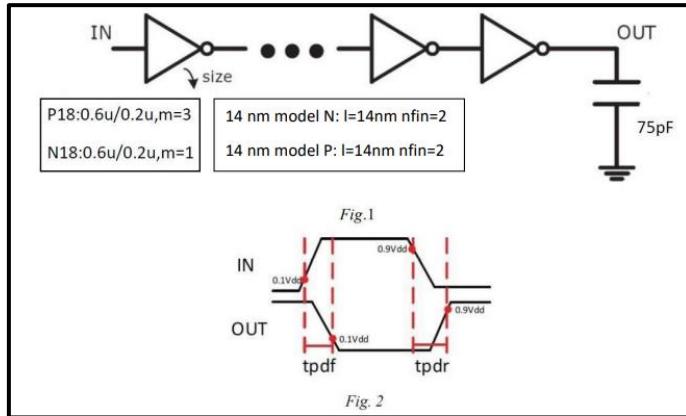
授課老師：謝志成

## Content:

1. Run an inverter buffer ( $\text{out} = \text{in}^{\text{---}}$ ) with output loading 75pF with VDD = 1V, as shown in Fig 1. (The size of the first inverter has been assigned.) (the rising time and falling time of input is 0.01ns & input frequency = 5MHz). ..... 2
  - (a) Please find the unit inverter, calculate the g and p and use the parameter to calculate the optimum  $\rho$  with the simulation result and your normalization condition. (10%) (Hint: use the skewed gate in Chapter 5)..... 2
  - (b) Please design the size and stage of the inverter chain to reach tpdf and tpdr < 1ns. (tpdf and tpdr definition: Fig 2.) (10%)..... 6
  - (c) Calculate the oscillation frequency based on the simulated parameters. (5%)..... 12
  - (d) Simulate the oscillation frequency. (10%) ..... 12
  - (e) What is the difference between (c) and (d), and comment on it. (10%)..... 13
  - (f) Change the output loading to 120pF, fix the stage of the inverter chain, and compare the simulated oscillation frequency between the different output loading. (15%) ..... 14
2. Please design a 3-to-8 decoder with output loading 300fF at each output node (as shown in Fig. 2) and try to add an inverter buffer to minimize the delay from input to output of the decoder. VDD = 1.8V, and the size of the first inverter has been assigne. (the rising time and falling time of input  $A[0]$ ,  $A^{\text{---}}[0]$  is 0.01ns & input frequency = 20MHz, the rising time and falling time of input  $A[1]$ ,  $A^{\text{---}}[1]$  is 0.01ns & input frequency = 40MHz, the rising time and falling time of input  $A[2]$ ,  $A^{\text{---}}[2]$  is 0.01ns & input frequency = 80MHz) (60%) ..... 18
  - (a) Describe how you design the inverter buffer and the other device size in detail. (10%) 18
  - (b) Finish the layout (whole circuit, from “A” to “Out”), DRC, and LVS. Paste the photo of the layout, DRC result, and LVS result in your report. Please mark the length and width on the layout and calculate the area( $\mu\text{m}^2$ ). (15%) ..... 23
  - (c) Run the post-layout simulation and compare it with the pre-sim. (10%) ..... 24

1. Run an inverter buffer ( $\text{out} = \text{in}^-$ ) with output loading  $75\text{pF}$  with  $\text{VDD} = 1\text{V}$ , as shown in Fig 1. (The size of the first inverter has been assigned.) (the rising time and falling time of input is  $0.01\text{ns}$  & input frequency =  $5\text{MHz}$ ).

[Run with  $.18\mu\text{m}$  technology and  $14\text{nm}$  technology]



- (a) Please find the unit inverter, calculate the  $g$  and  $p$  and use the parameter to calculate the optimum  $\rho$  with the simulation result and your normalization condition. (10%) (Hint: use the skewed gate in Chapter 5)

**180nm:**

$\text{VDD} = 1.8\text{V}$ :

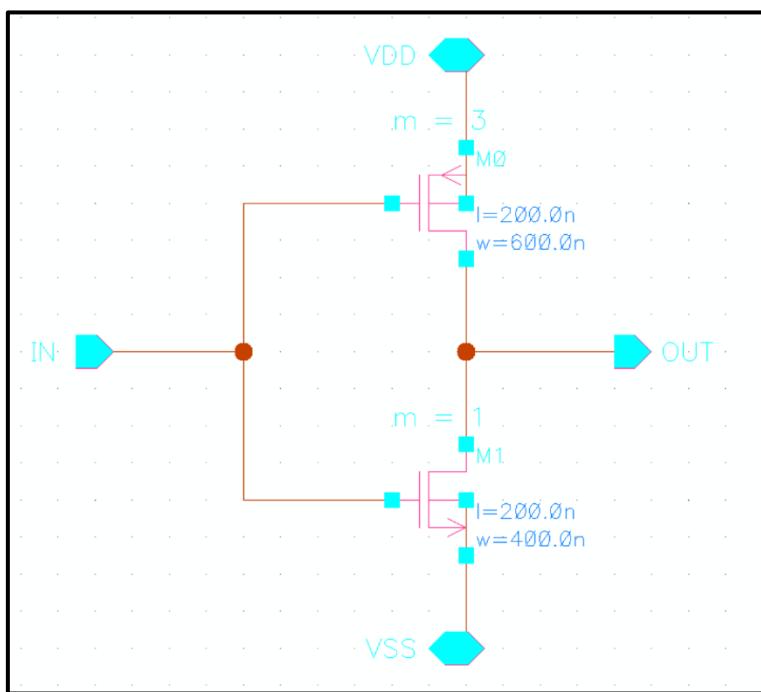


Figure 1 Unit inverter schematic

	$W(L=0.2\mu)$	M
PMOS	$0.6\mu$	1
NMOS	$0.4\mu$	3

Table 1 Unit inverter size

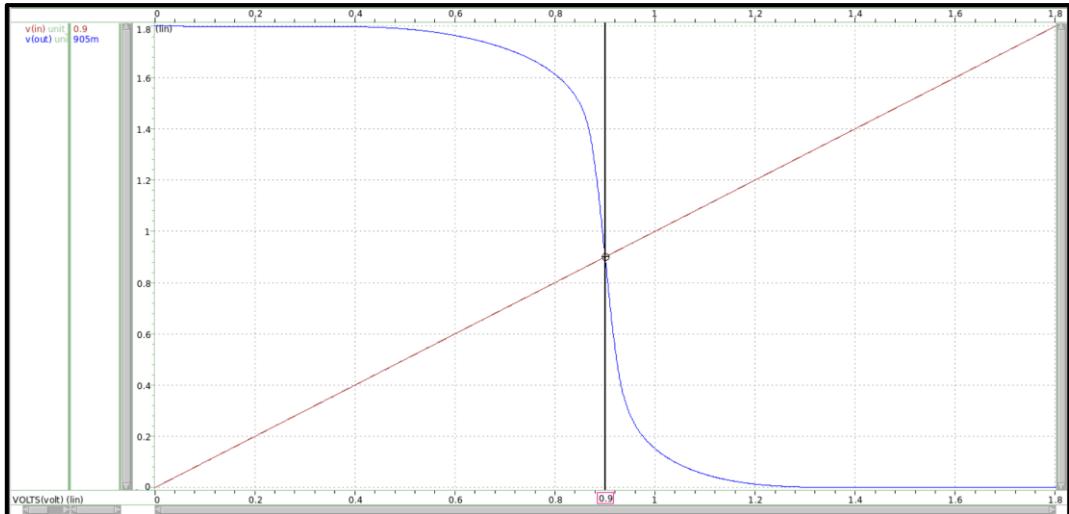


Figure 2 Unit inverter VTC

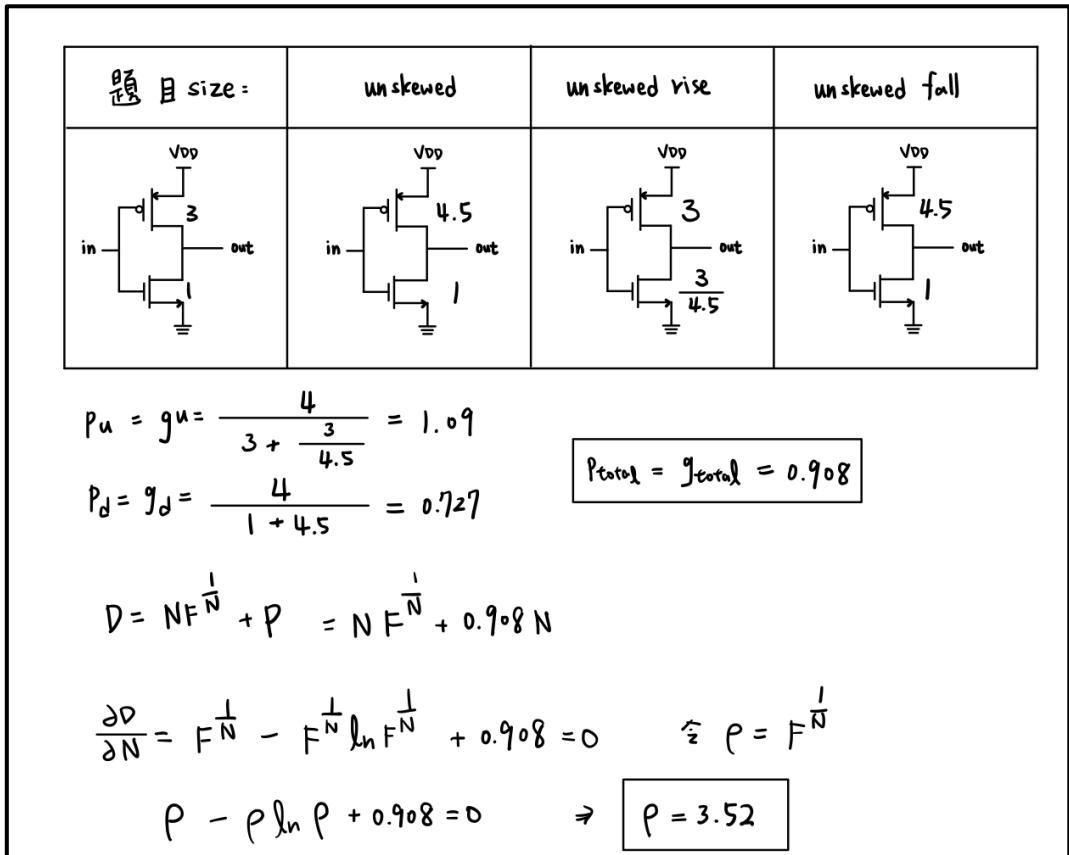


Figure 3 Calculate p & g &  $\rho$

$g = 0.908$	$p = 0.908$	$\rho = 3.52$
-------------	-------------	---------------

Table 2 p & g &  $\rho$  value

下方附上題目原本要求的  $VDD=1V$  時的計算與模擬結果，可以發現在  $VDD=1V$  時的  $g, h, \rho$  都相較於  $VDD=1V$  小。

VDD = 1V:

	W(L=0.2u)	M
PMOS	2.13u	1
NMOS	0.6u	3

Table 3 Unit inverter size

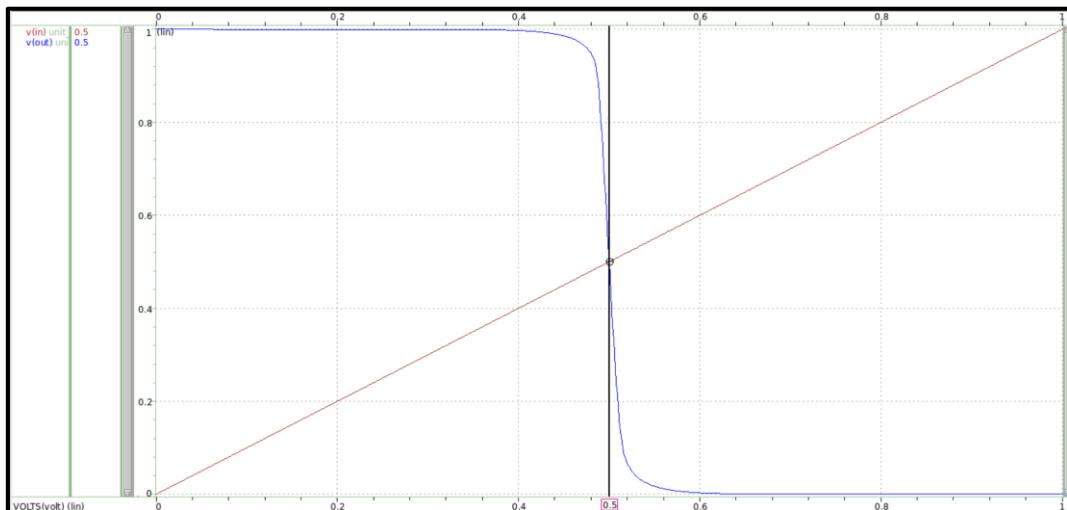


Figure 4 Unit inverter VTC

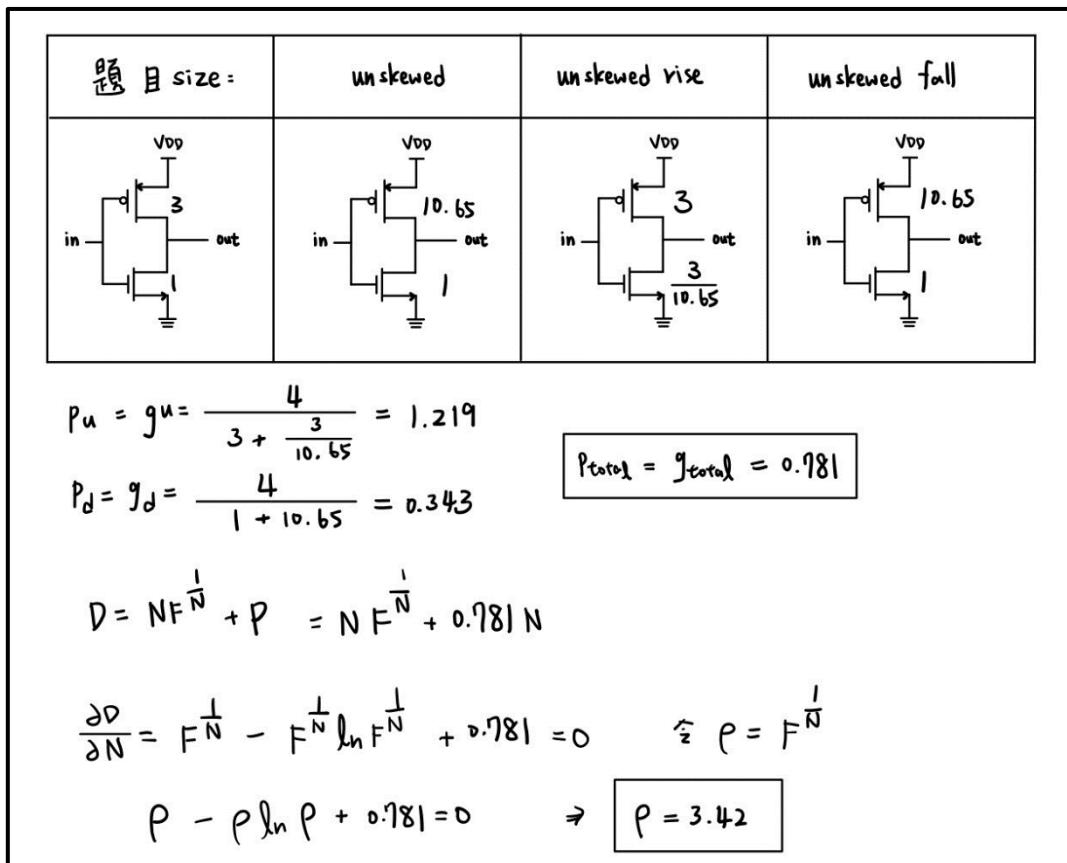


Figure 5 Calculate p & g &  $\rho$

$g = 0.781$	$p = 0.781$	$\rho = 3.42$
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Table 4 p & g &  $\rho$  value

14nm:

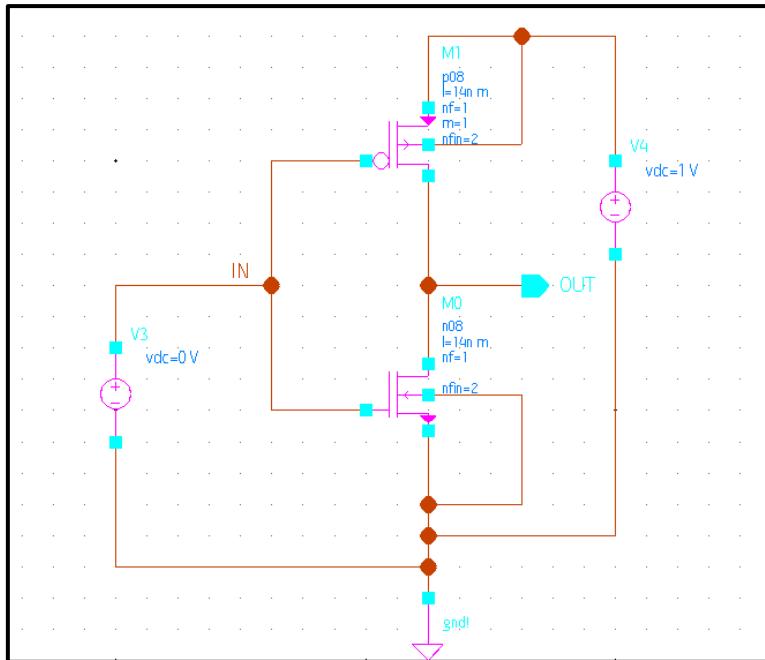


Figure 6 Unit inverter schematic

nfinp	2
nfinn	2

Table 5 Unit inverter size

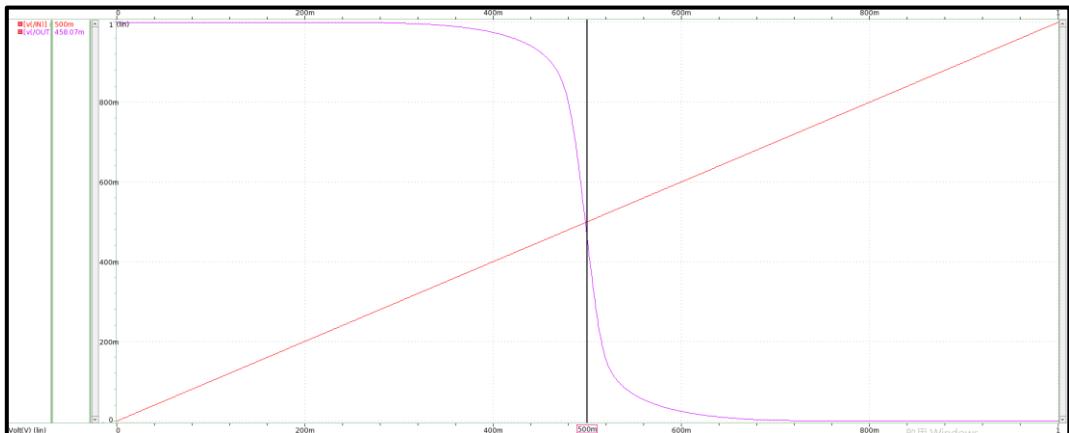


Figure 7 Unit inverter VTC

$$g = 1, \rho = 1, D = NF^{\frac{1}{N}} + P = NF^{\frac{1}{N}} + N$$

$$\frac{\partial D}{\partial N} = F^{\frac{1}{N}} - F^{\frac{1}{N}} \ln F^{\frac{1}{N}} + 1 = 0, \therefore \rho = F^{\frac{1}{N}} \Rightarrow \rho - \rho \ln \rho + 1 = 0 \Rightarrow \rho = 3.59$$

Figure 8 Calculate  $\rho$

$g = 1$	$p = 1$	$\rho = 3.59$
---------	---------	---------------

Table 6 p & g &  $\rho$  value

- (b) Please design the size and stage of the inverter chain to reach tpdf and tpdr < 1ns.  
 (tpdf and tpdr definition: Fig 2.) (10%)

**180nm:**

VDD = 1.8V:

$$\left\{ \begin{array}{l} F = G_B H = (0.908)^N \times 1 \times \frac{75 \times 10^{-12}}{4.6961 \times 10^{15}} = 15970.7 \times (0.908)^N \\ P = F^{\frac{1}{N}} = [15970.7 \times (0.908)^N]^{\frac{1}{N}} = 3.52 \\ (15970.7)^{\frac{1}{N}} = 3.876 \quad \frac{1}{N} \log 15970.7 = \log 3.876 \Rightarrow N = 7.144 \Rightarrow \text{取 } N = 7 \end{array} \right.$$

Figure 9 Calculate the inverter chain stage

maximum nodal capacitance=	9.170E-11	on node	0:vss					
nodal capacitance table								
node	=	cap	node	=	cap	node	=	cap
+0:in	=	4.6961f	0:out	=	89.5228p	0:vdd	=	36.1608p
+0:vss	=	91.7007p	1:net33	=	22.2847f	1:net37	=	79.4092f
+1:net41	=	356.5099f	1:net45	=	1.2498p	1:net49	=	5.6559p
+1:net53	=	19.8406p						

Figure 10 Cin value when Vi = 0.5VDD

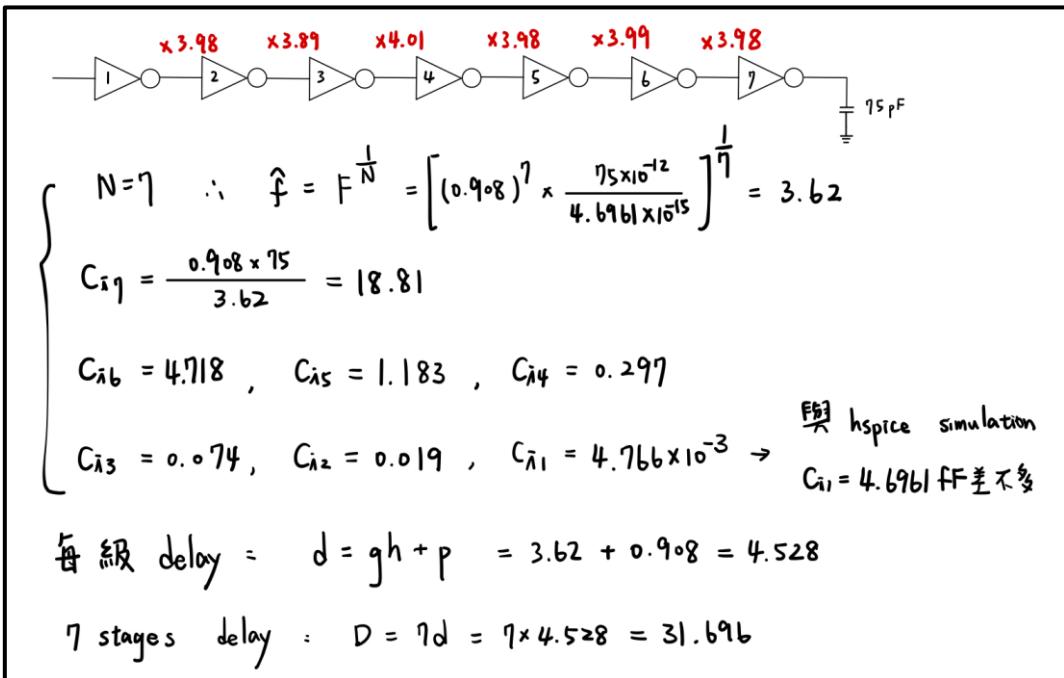


Figure 11 Calculate every state size & path delay

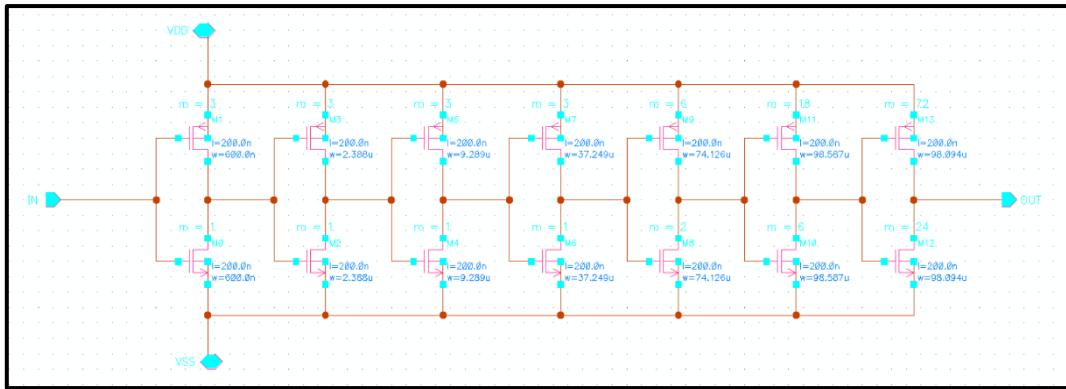


Figure 12 Inverter chain schematic

PMOS	W (L = 0.2u)	m
1st stage	0.6u	3
2nd stage	2.52u	3
3rd stage	10.256u	3
4th stage	43.383u	3
5th stage	91.105u	6
6th stage	95.66u	24
7th stage	97.4u	99

Table 7 PMOS size

NMOS	W (L = 0.2u)	m
1st stage	0.6u	1
2nd stage	2.52u	1
3rd stage	10.256u	1
4th stage	43.383u	1
5th stage	91.105u	2
6th stage	95.66u	8
7th stage	97.4u	33

Table 8 NMOS size

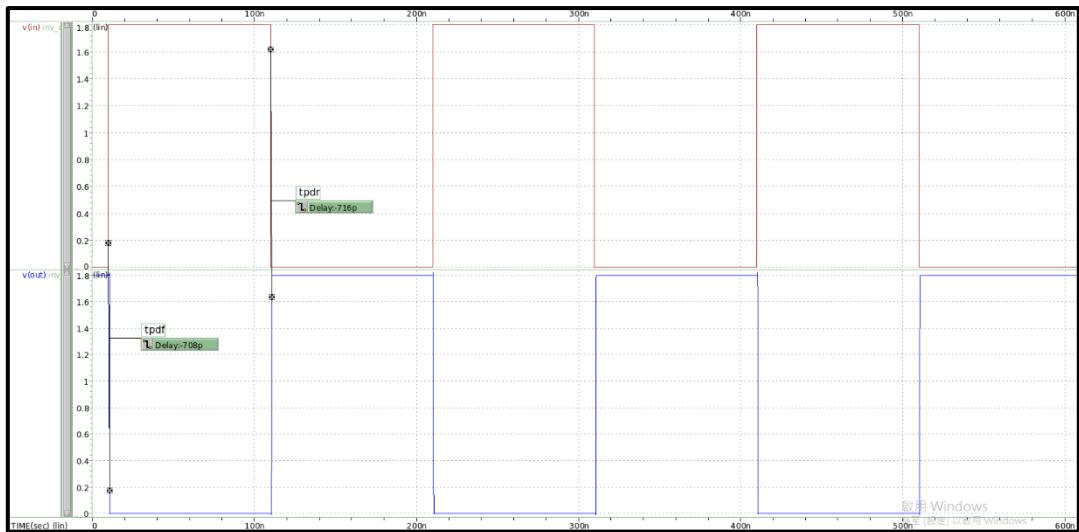


Figure 13 Delay waveform

$tpdr = 716\text{ps}$	$tpdf = 708\text{ps}$
$tpd = \frac{tpdr+tpdf}{2} = 712\text{ps}$	

Table 9 Propagation delay

下方同樣附上題目原本要求的 VDD=1V 時的計算與模擬結果，可以發現在 VDD=1V 時，同樣是取 7 級 inverter，但 VDD=1V 的 propagation delay 會大於 1ns，在 1V 的情形下無法將 delay 縮減到 1ns 以下，所以下面的 oscillation loop 就不再繼續模擬。

VDD = 1V:

$$\begin{cases} F = G B H = (0.781)^N \times 1 \times \frac{75 \times 10^{-12}}{3.2559 \times 10^{-15}} = 23035.11 \times (0.781)^N \\ \rho = F^{\frac{1}{N}} = [23035.11 \times (0.781)^N]^{\frac{1}{N}} = 3.42 \\ (23035.11)^{\frac{1}{N}} = 4.379 \quad \frac{1}{N} \log 23035.11 = \log 4.379 \Rightarrow N = 6.802 \Rightarrow \text{取 } N = 7 \end{cases}$$

Figure 14 Calculate the inverter chain stage

maximum nodal capacitance= 9.554E-11		on node	0:out		
nodal capacitance table					
node	= cap	node	= cap	node	= cap
+0:in	= 3.2559f	0:out	= 95.5368p	0:vdd	= 49.2276p
+0:vss	= 22.5013p	1:ci_2	= 23.6710f	1:ci_3	= 86.1979f
+1:ci_4	= 414.3061f	1:ci_5	= 1.5073p	1:ci_6	= 7.3045p
+1:ci_7	= 26.5839p				

Figure 15 Cin value when Vi = 0.5VDD

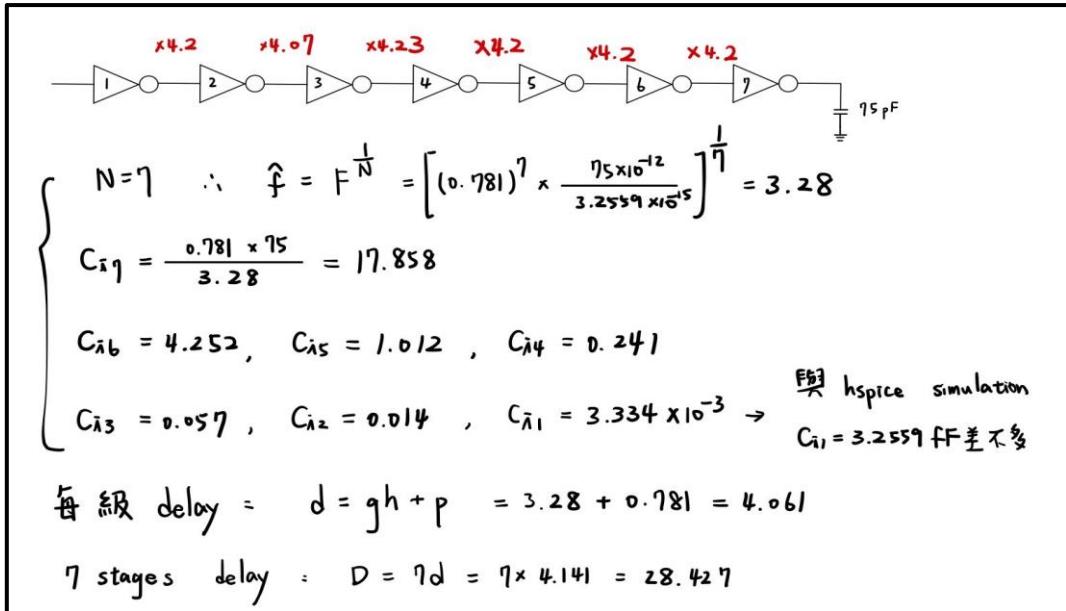


Figure 16 Calculate every state size & path delay

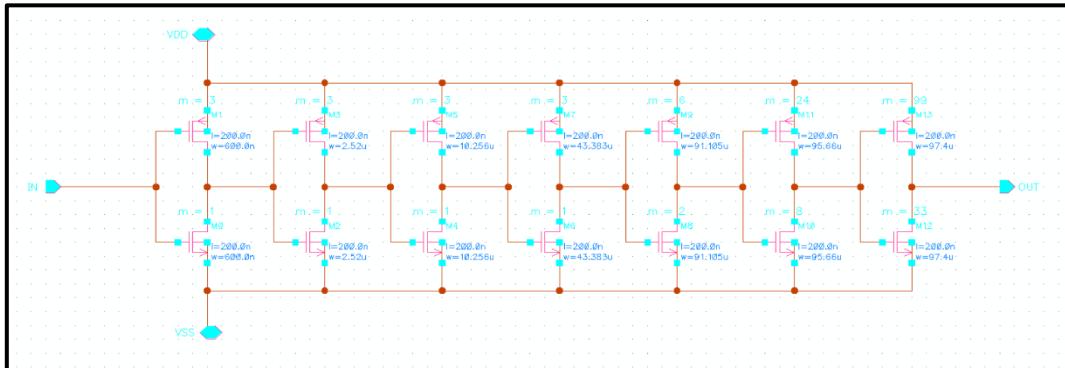


Figure 17 Inverter chain schematic

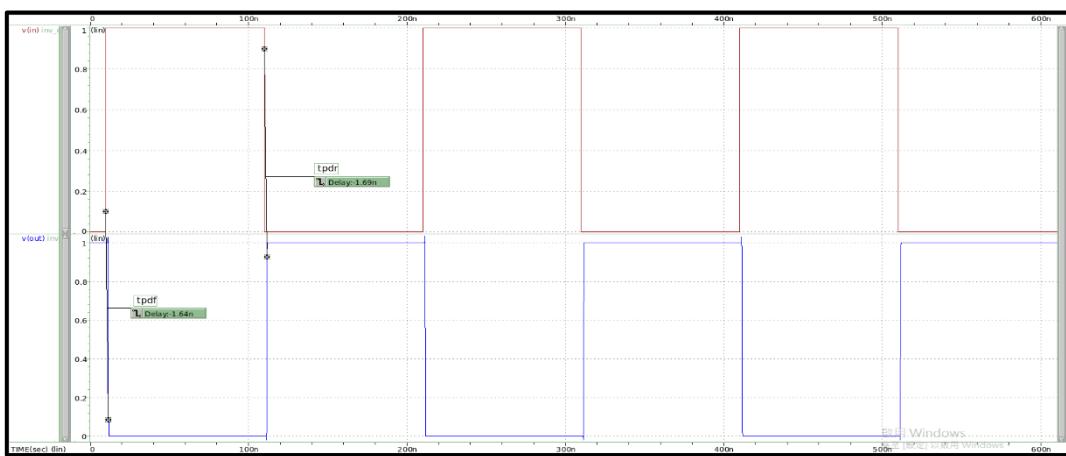


Figure 18 Delay waveform

$\text{tpdr} = 1.69\text{ns}$	$\text{tpdf} = 1.64\text{ns}$
$\text{tpd} = \frac{\text{tpdr}+\text{tpdf}}{2} = 1.665\text{ns}$	

Table 10 Propagation delay

14nm:

$$F = G \cdot B \cdot H = 1 \times 1 \times \frac{75 \times 10^{-12}}{0.1525 \times 10^{-15}} = 491803$$

$$\rho = F^{\frac{1}{N}} = 3.59 \quad \Rightarrow \quad (491803)^{\frac{1}{N}} = 3.59$$

$$N = \frac{\log(491803)}{\log(3.59)} = 10.25 \quad \Rightarrow \text{取 } N = 11$$

Figure 19 Calculate the inverter chain stage

```
* PrimeSim SPICE U-2023.03.SPI1 (Compiled on May 19 2023 at 16:51:02 (US-Pacific)) build id: 8211726
* Copyright(c) 2003-2023 Synopsys, Inc.
* Generated at Sat Dec 2 13:57:25 2023
* Host: 192.168.1.104, Username: m111063517
* Input File: /home/m111063517/simulation/HW3(inv_chain_75.schematic/history_1/simulation/PrimeSim_default/PrimeSimSPICE/nominal/netlist/primesim.spi
* Title: "Generated for: PrimeSim"
* temperature = 25.0000
* time = 0.0000
*.option captab=1
* capacitance table
out 78.1977 pF
net76 10.0017 pF
net58 3.2155 pF
net65 1.1113 pF
net46 0.3825 fF
net37 122.4783 fF
net44 39.7785 fF
net48 13.7563 fF
net27 4.4280 fF
net20 1.5287 fF
net13 0.4913 fF
net1 5.2500 pF
in 0.1525 fF
```

Cin = 0.1525fF

Figure 20 Cin value when Vi = 0.5VDD

$$\hat{f} = N^{\frac{1}{F}} = (491803)^{\frac{1}{11}} = 3.29, \text{ 每級相差3.29倍。但 nfin 只能整數，故取 3 倍}$$

$$C_{in\_11} = \frac{1 \times 75 \text{ pF}}{3.29} = 22.996 \text{ pF}, \quad C_{in\_10} = \frac{1 \times 22.996 \text{ pF}}{3.29} = 6.929 \text{ pF}$$

$$C_{in\_9} = \frac{1 \times 6.929 \text{ pF}}{3.29} = 2.106 \text{ pF}, \quad C_{in\_8} = \frac{1 \times 2.106 \text{ pF}}{3.29} = 0.64 \text{ pF}$$

$$C_{in\_7} = \frac{1 \times 0.64 \text{ pF}}{3.29} = 0.195 \text{ pF}, \quad C_{in\_6} = \frac{1 \times 0.195 \text{ fF}}{3.29} = 59.271 \text{ fF}$$

$$C_{in\_5} = \frac{1 \times 59.271 \text{ fF}}{3.29} = 18.016 \text{ fF}, \quad C_{in\_4} = \frac{1 \times 18.016 \text{ fF}}{3.29} = 5.476 \text{ fF}$$

$$C_{in\_3} = \frac{1 \times 5.476 \text{ fF}}{3.29} = 1.664 \text{ fF}, \quad C_{in\_2} = \frac{1 \times 1.664 \text{ fF}}{3.29} = 0.506 \text{ fF}$$

$$C_{in} = \frac{1 \times 0.506 \text{ fF}}{3.29} = 0.154 \text{ fF} \quad \text{與 simulation } C_{in} = 0.1525 \text{ fF 相近}$$

每級 delay = d = gh + p = 3.29 + 1 = 4.29

11 stages delay = D = 11 d = 47.19

Figure 21 Calculate every state size & path delay

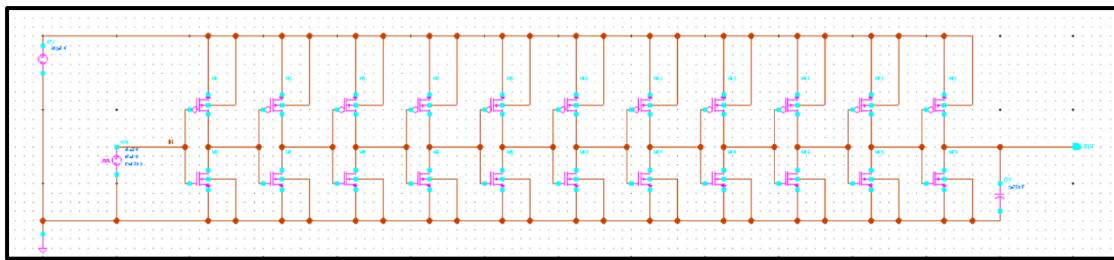


Figure 22 Inverter chain schematic

PMOS & NMOS	$nfinp = nfinn (L = 14nm)$	Number of fingers
1st stage	2	1
2nd stage	6	1
3rd stage	18	1
4th stage	54	1
5th stage	162	1
6th stage	81	6
7th stage	81	18
8th stage	81	54
9th stage	81	162
10th stage	243	162
11th stage	243	486

Table 11 Size

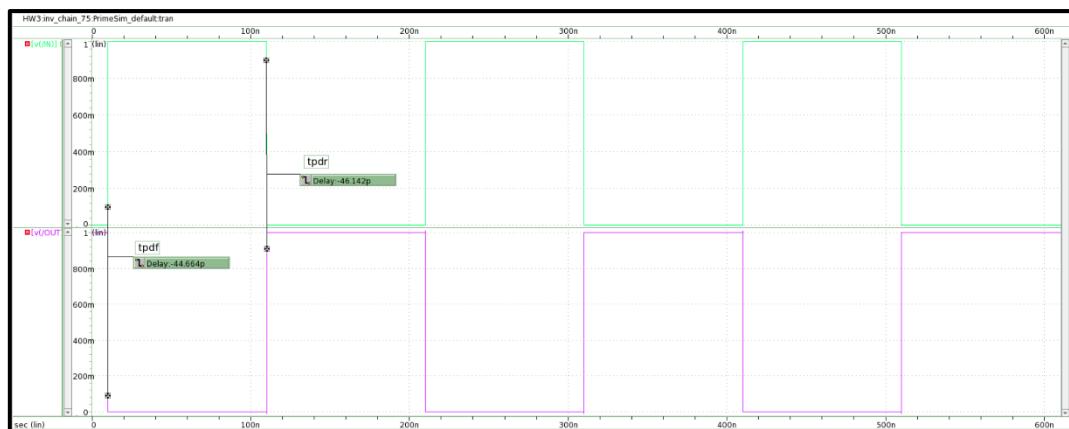


Figure 23 Delay waveform

$tpdr = 46.142\text{ps}$	$tpdf = 44.664\text{ps}$
$tpd = \frac{tpdr+tpdf}{2} = 45.403\text{ps}$	

Table 12 Propagation delay

(c) Calculate the oscillation frequency based on the simulated parameters. (5%)

**180nm:**

$$f_{osc} = \frac{1}{2Nd} = \frac{1}{2 * 712p} = 702.25MHz$$

**14nm:**

$$f_{osc} = \frac{1}{2Nd} = \frac{1}{2 * 45.403p} = 11.012GHz$$

(d) Simulate the oscillation frequency. (10%)

**180nm:**

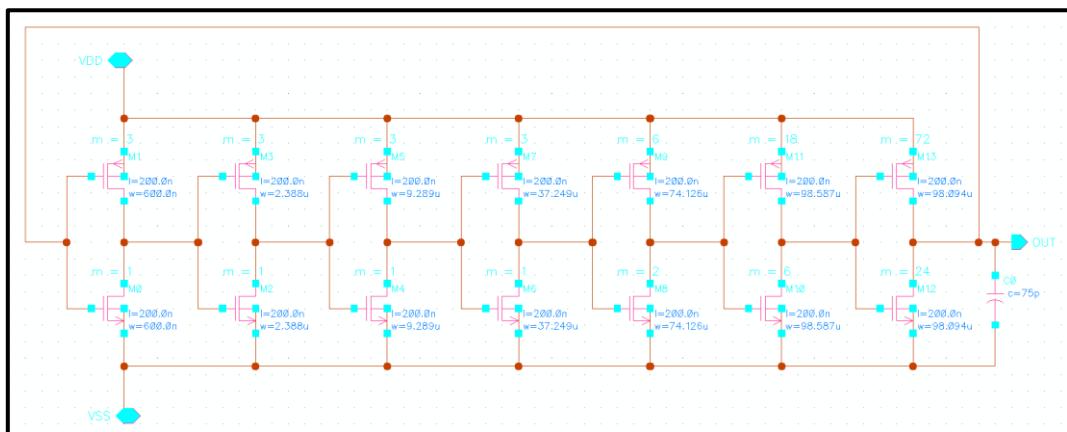


Figure 24 Oscillator schematic(75pF)

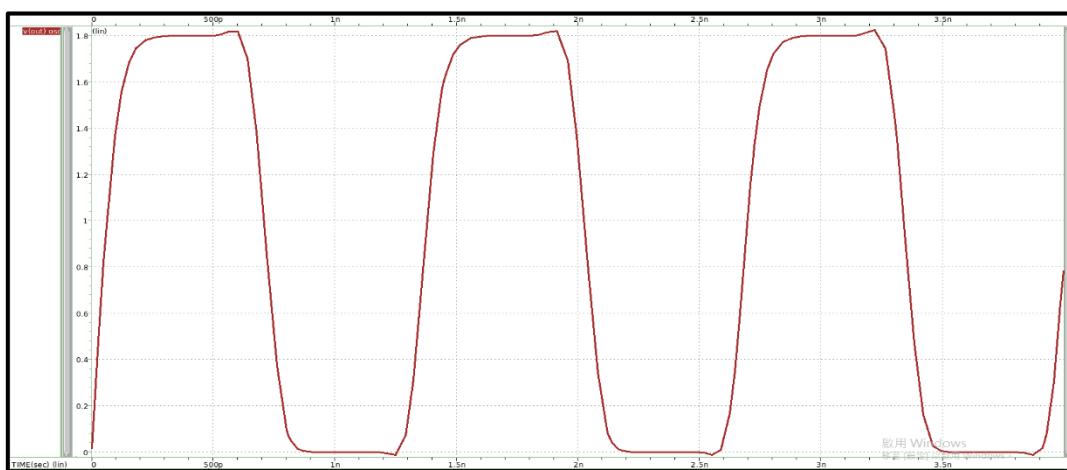


Figure 25 Oscillator waveform(75pF)

```
***** transient analysis tnom= 25.000 temp= 25.000 *****
period= 1.3183n targ= 1.3810n trig= 62.6726p
```

Figure 26 Oscillator period(75pF)

$$Frequency = \frac{1}{period} = 758.55MHz$$

**14nm:**

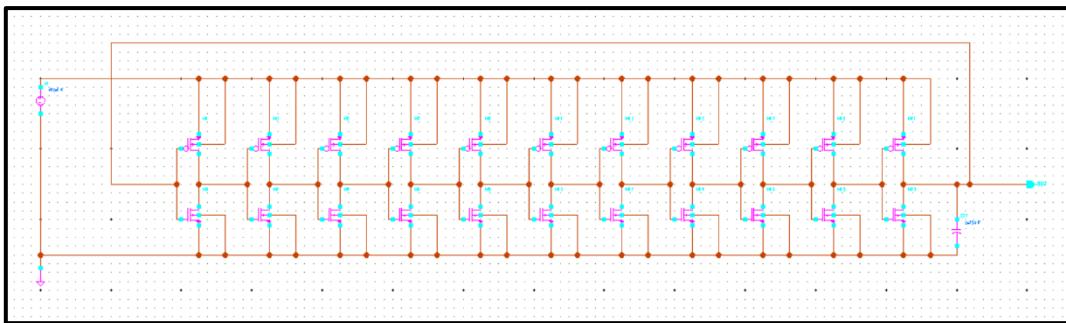


Figure 27 Oscillator schematic(75pF)

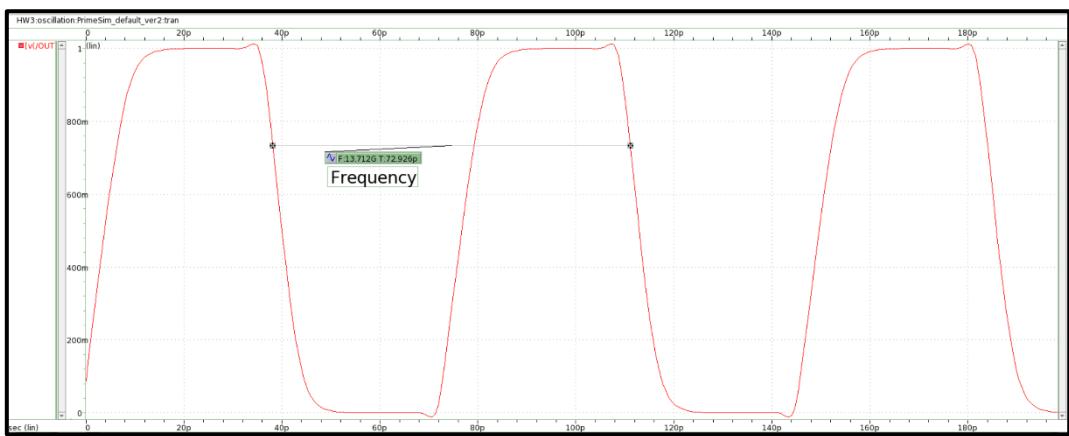


Figure 28 Oscillator waveform(75pF)

$$Frequency = 13.712 \text{ GHz}$$

(e) What is the difference between (c) and (d), and comment on it. (10%)

**180nm:**

計算的結果是  $f_{osc} = 702.25\text{MHz}$  而模擬的結果是  $f_{osc} = 758.55\text{MHz}$ ，從結果可以知道使用前兩小題結果計算的頻率較小，原因是因為(c)小題是用輸入 0.9VDD 到輸出 0.9VDD 的 propagation delay，所以 delay 時間較長，但(d)小題的模擬，是 0.5VDD 到 0.5VDD，delay 時間較短，故(c)小題的頻率會較(d)小題小。

**14nm:**

模擬結果與 180nm 的趨勢一樣，(c)小題計算的結果比(d)小題長，原因來自於定義不同。

- (f) Change the output loading to 120pF, fix the stage of the inverter chain, and compare the simulated oscillation frequency between the different output loading. (15%)

**180nm:**

$$\left\{ \begin{array}{l} F = GBH = (0.908)^N \times 1 \times \frac{120 \times 10^{-12}}{4.6961 \times 10^{-15}} = 25553.12 \times (0.908)^N \\ \rho = F^{\frac{1}{N}} = [25553.12 \times (0.908)^N]^{\frac{1}{N}} = 3.52 \\ (25553.12)^{\frac{1}{N}} = 3.876 \quad \frac{1}{N} \log 25553.12 = \log 3.876 \Rightarrow N = 7.491 \Rightarrow N = 7 \end{array} \right.$$

Figure 29 Calculate the inverter chain stage

$$\left\{ \begin{array}{l} N = 7 \quad \therefore \hat{f} = F^{\frac{1}{N}} = \left[ (0.908)^7 \times \frac{120 \times 10^{-12}}{4.6961 \times 10^{-15}} \right]^{\frac{1}{7}} = 3.87 \\ C_{i1} = \frac{0.908 \times 120}{3.87} = 28.16 \\ C_{i2} = 6.607, \quad C_{i3} = 1.55, \quad C_{i4} = 0.364 \\ C_{i5} = 0.085, \quad C_{i6} = 0.02, \quad C_{i7} = 4.693 \times 10^{-3} \xrightarrow{\text{hspice simulation}} C_{i1} = 4.6961 \text{ fF} \end{array} \right.$$

$$\text{每級 delay} = d = g + p = 3.87 + 0.908 = 4.778$$

$$7 \text{ stages delay} : D = 7d = 7 \times 4.778 = 33.446$$

Figure 30 Calculate every state size & path delay

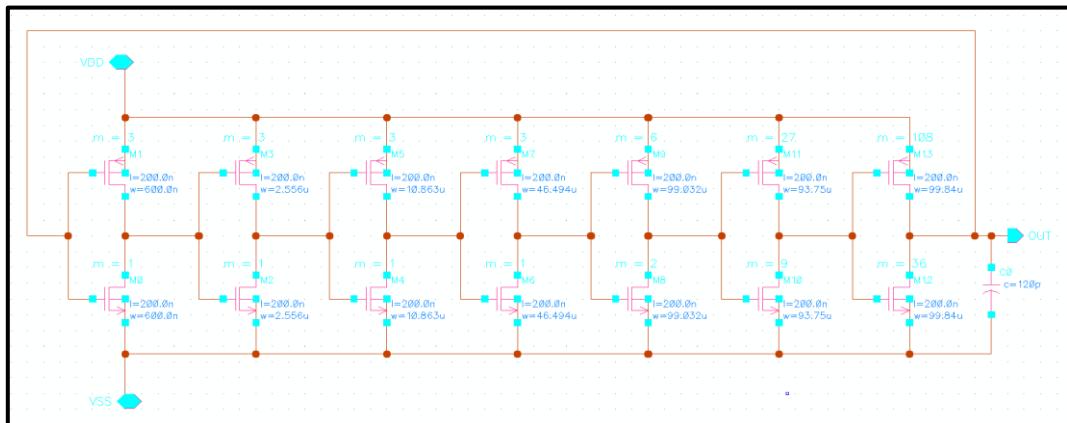


Figure 31 Oscillator schematic(120pF)

PMOS	W (L = 0.2u)	m
1st stage	0.6u	3
2nd stage	2.556u	3
3rd stage	10.863u	3
4th stage	46.494u	3
5th stage	99.032u	6
6th stage	93.75u	27
7th stage	99.84u	108

Table 13 PMOS size

NMOS	W (L = 0.2u)	m
1st stage	0.6u	1
2nd stage	2.556u	1
3rd stage	10.863u	1
4th stage	46.494u	1
5th stage	99.032u	2
6th stage	93.75u	9
7th stage	99.84u	36

Table 14 NMOS size



Figure 32 Oscillator waveform(120pF)

```
***** transient analysis tnom= 25.000 temp= 25.000 *****
period= 1.3931n targ= 1.4581n trig= 64.9490p
```

Figure 33 Oscillator period(120pF)

$$Frequency = \frac{1}{period} = 717.82MHz$$

Blue: 75pF  
Red: 120pF

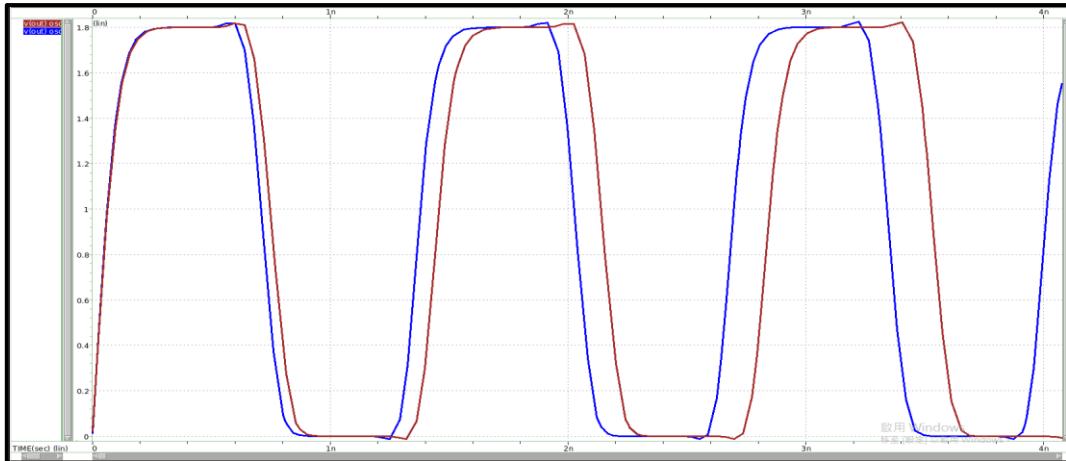


Figure 34 Compare with 75pF and 120pF Oscillator

Load capacitance 變大使  $F = GBH$  中的  $H$  變大，故 delay 也因此變大，與模擬相符。

14nm:

$$F = G_B H = 1 \times 1 \times \frac{120 \times 10^{-12}}{0.1525 \times 10^{-15}} = 786885$$

$$\rho = F^{\frac{1}{N}} = 3.59 \quad \Rightarrow \quad (786885)^{\frac{1}{N}} = 3.59$$

$$N = \frac{\log(1491803)}{\log(3.59)} = 10.62 \quad \Rightarrow \text{取 } N = 11$$

Figure 35 Calculate the inverter chain stage

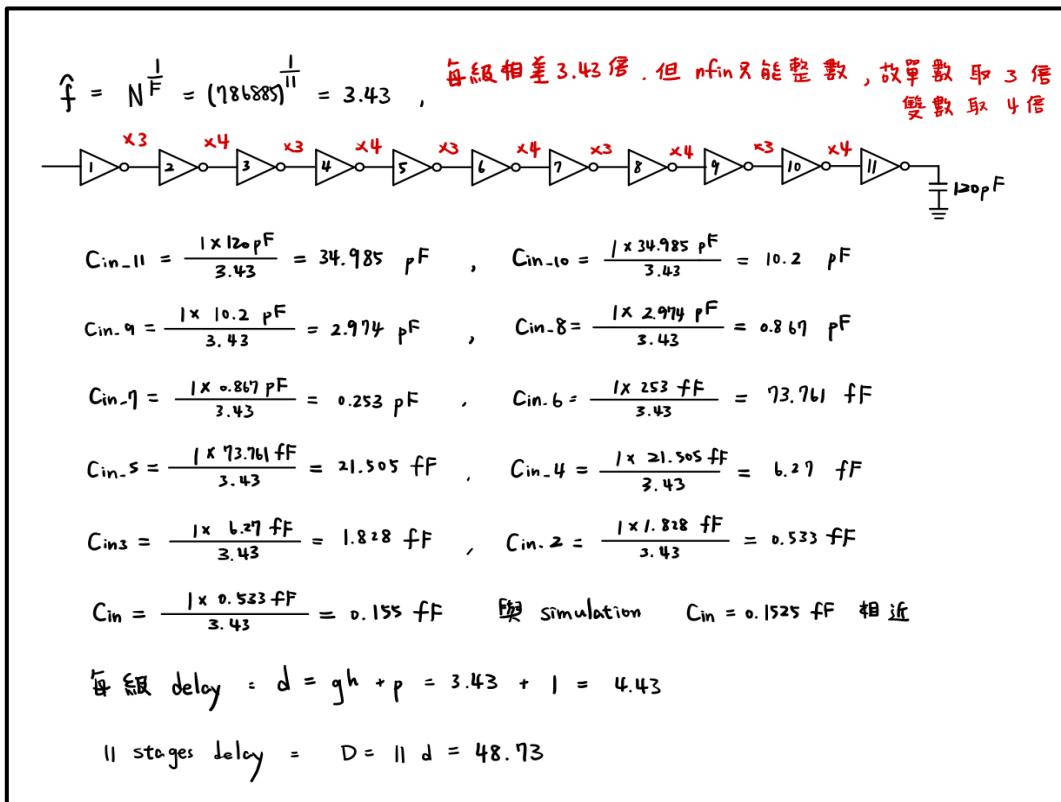


Figure 36 Calculate every state size & path delay

PMOS & NMOS	nfinp = nfinn (L = 14nm)	Number of fingers
1st stage	2	1
2nd stage	6	1
3rd stage	24	1
4th stage	72	1
5th stage	288	1
6th stage	108	8
7th stage	108	32
8th stage	108	96
9th stage	108	384
10th stage	324	384
11th stage	324	1536

Table 15 Size

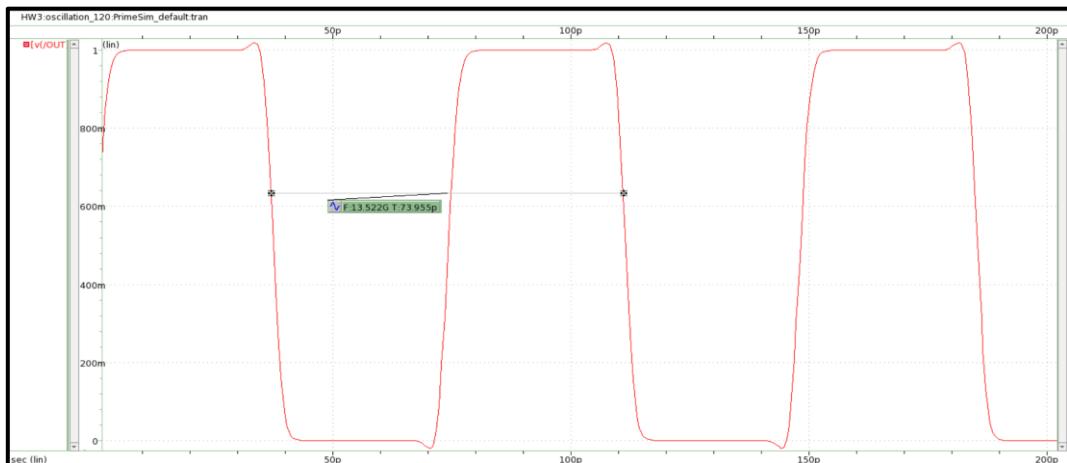


Figure 37 Oscillator waveform(120pF)

Frequency = 13.522GHz

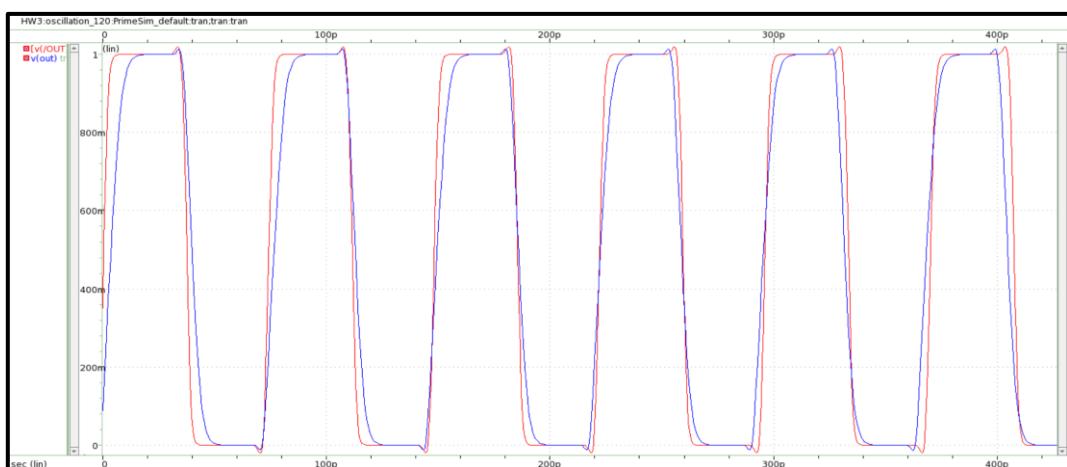
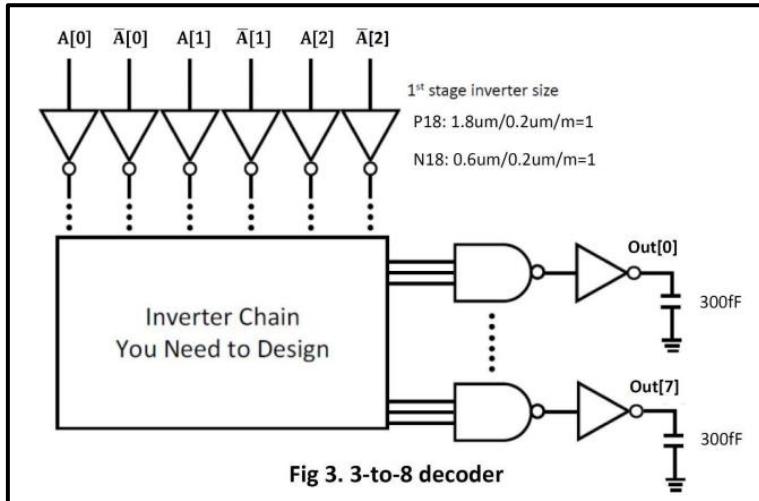


Figure 38 Compare with 75Pf and 120pF Oscillator

與 180nm 相同，因 Load capacitance 所以 delay 也因此變大，不同之處是在最一開始的 2 個波呈現相反的現象。

2. Please design a 3-to-8 decoder with output loading 300fF at each output node (as shown in Fig. 2) and try to add an inverter buffer to minimize the delay from input to output of the decoder. VDD = 1.8V, and the size of the first inverter has been assigned. (the rising time and falling time of input A[0],  $\bar{A}[0]$  is 0.01ns & input frequency = 20MHz, the rising time and falling time of input A[1],  $\bar{A}[1]$  is 0.01ns & input frequency = 40MHz, the rising time and falling time of input A[2],  $\bar{A}[2]$  is 0.01ns & input frequency = 80MHz) (60%)

[You only need to run with .18um technology]



- (a) Describe how you design the inverter buffer and the other device size in detail. (10%)
- 設計 Unit inverter size。
  - 使用 Unit inverter size 得到的 P/N ratio 計算 3-inputs-NAND 的 logic effort。
  - 計算第一顆 inverter 的 logic effort。
  - 算出整體的 path delay，再用 path delay 對 N 微分找出最佳 state。

以下詳細說明每步驟的計算過程。

Unit inverter 的 size 有兩組如下：

PMOS: 2.4u/200n, m=1; NMOS: 600n/200n, m=1

PMOS: 1.8u/200n, m=1; NMOS: 400n/200n, m=1

我選擇了第一組，原因是因為第二組在 layout 上會遇到無法 layout 的情形，因為在 diffusion 為 0.4 時長度不足以放下 contact。

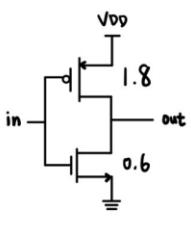
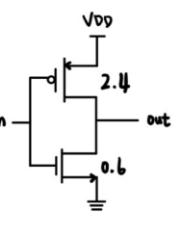
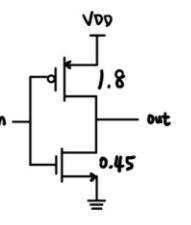
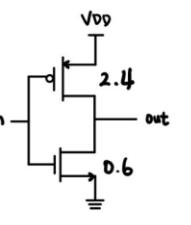
```

maximum nodal capacitance= 9.057E-15          on node 0:vdd
nodal capacitance table
node = cap   node = cap   node = cap
+0:in = 4.7010f 0:out = 3.0336f 0:vdd = 9.0567f
+0:vss = 3.5466f

```

Figure 39 Cin capacitance

推測與第一題相比因沒有使用並聯電容所電容較大。

題目 size:	Unit inverter	unskewed rise	unskewed fall
			

$$g_u = P_u = \frac{2.4}{1.8 + 0.45} = 1.07$$

$$g_d = P_d = \frac{2.4}{2.4 + 0.6} = 0.8$$

$$\Rightarrow g_{avg} = P_{avg} = 0.935$$

Figure 40 Calculate unit inverter

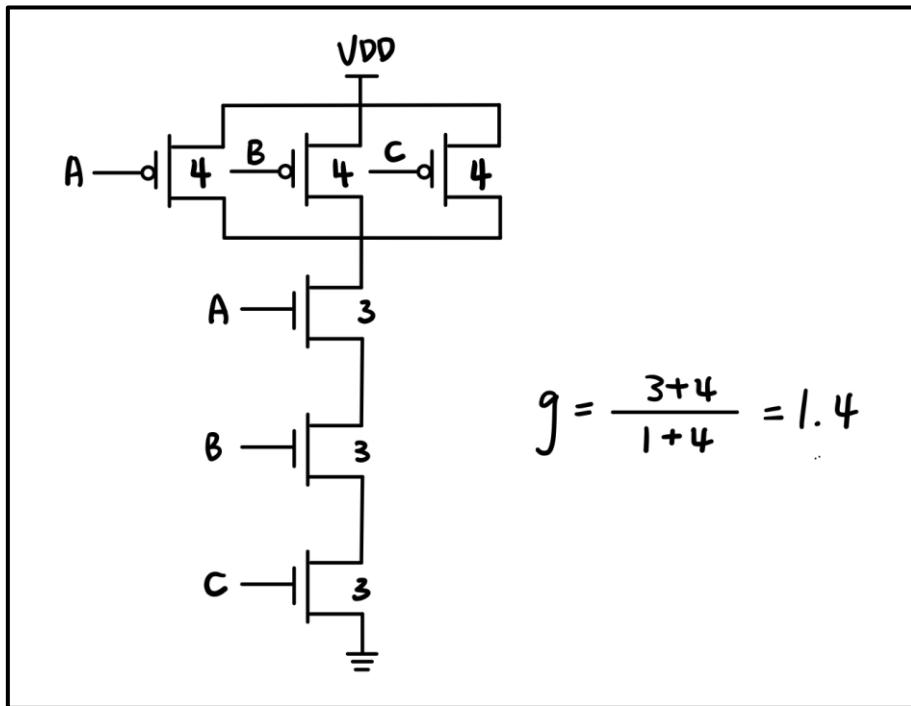


Figure 41 Calculate the 3 inputs NAND size

$$D = NF^{\frac{1}{N}} + P = NF^{\frac{1}{N}} + [0.935(N-2) + 3 + 1] = NF^{\frac{1}{N}} + 0.935N + 2.13$$

$$\frac{\partial D}{\partial N} = F^{\frac{1}{N}} - F^{\frac{1}{N}} \ln F^{\frac{1}{N}} + 0.935 = 0 \quad \therefore P = F^{\frac{1}{N}}$$

$$P - P \ln P + 0.935 = 0 \quad \Rightarrow \quad P = 3.54$$

$$N = n + 2$$

$$\begin{cases} F = GBH = (0.935)^n \times 1.4 \times 4 \times \frac{300 \times 10^{-15}}{4.7010 \times 10^{-15}} = 357.37 \times (0.935)^n \\ P = F^{\frac{1}{N}} = [357.37 \times (0.935)^n]^{\frac{1}{n+2}} = 3.52 \quad n=2.5 \quad \Rightarrow \text{取 } n=2 \end{cases}$$

Figure 42 Calculate buffer state

由此可知 inverter buffer 為 2 顆。

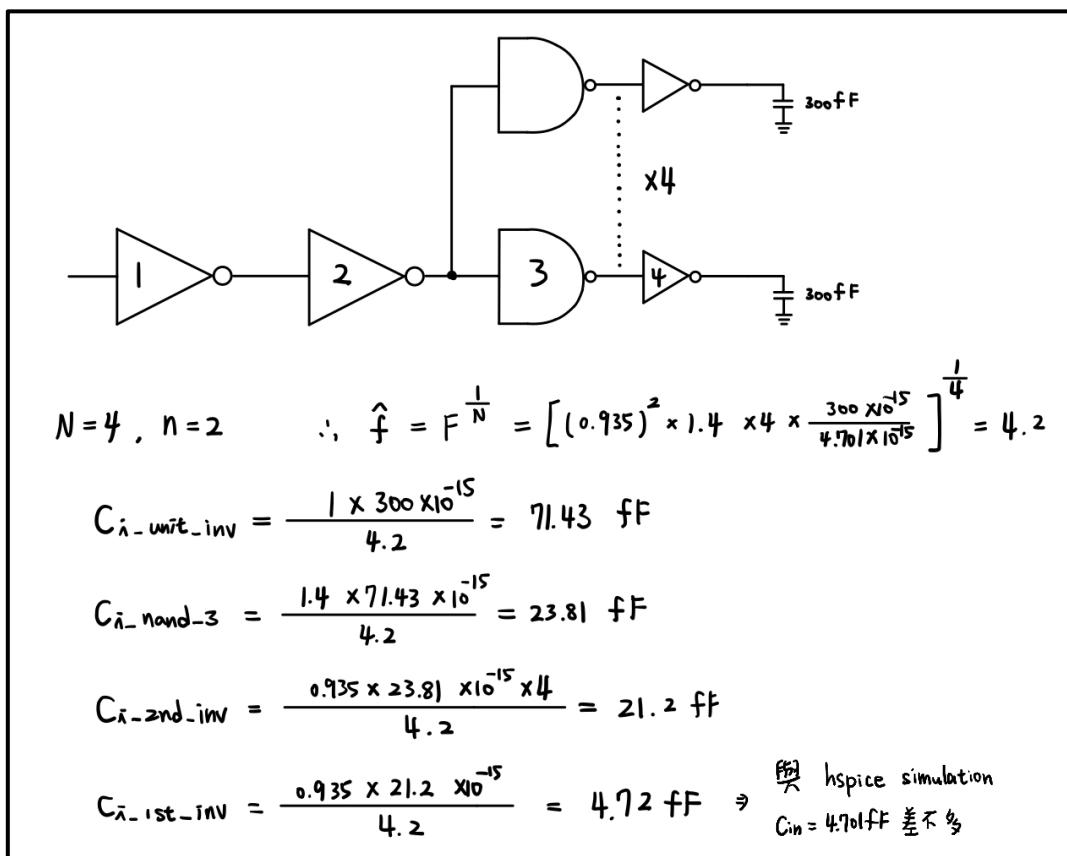


Figure 43 Calculate capacitance

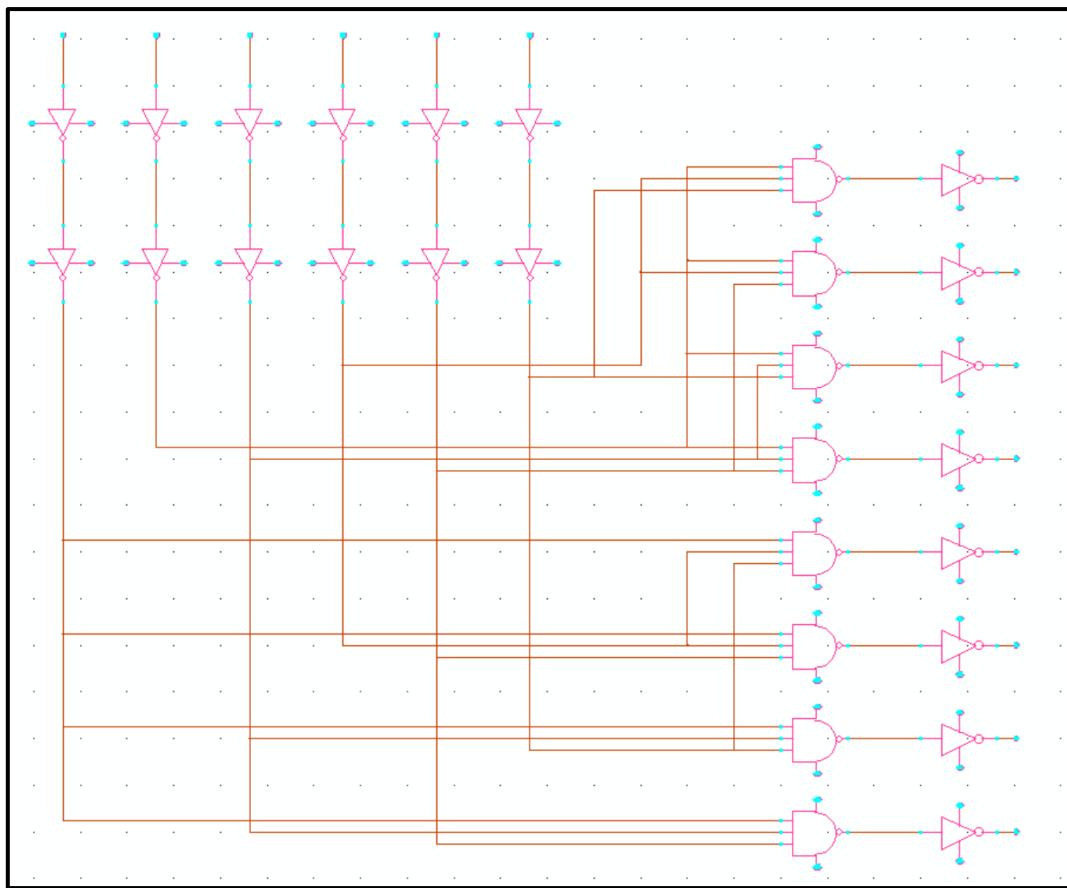


Figure 44 Decoder schematic

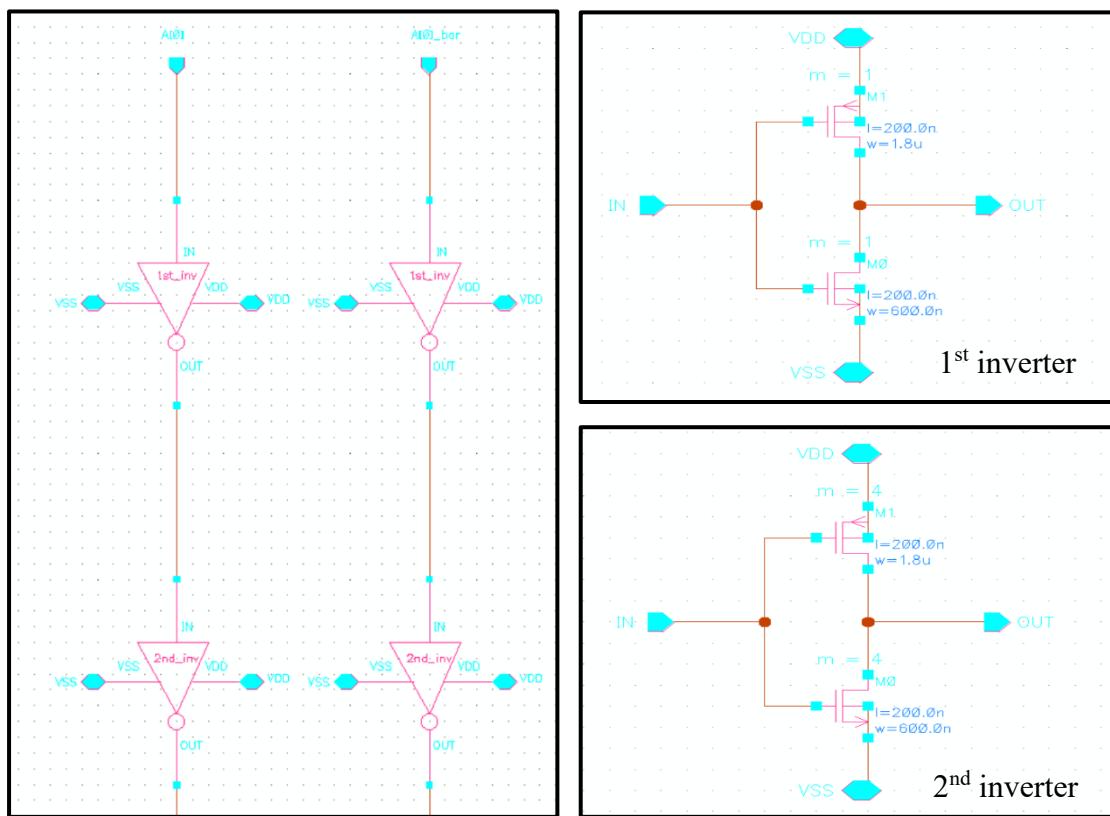


Figure 45 1<sup>st</sup> & 2<sup>nd</sup> inverter

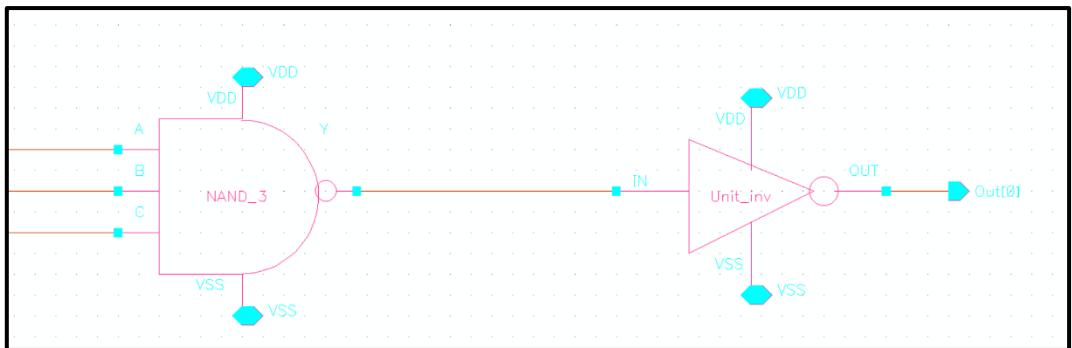
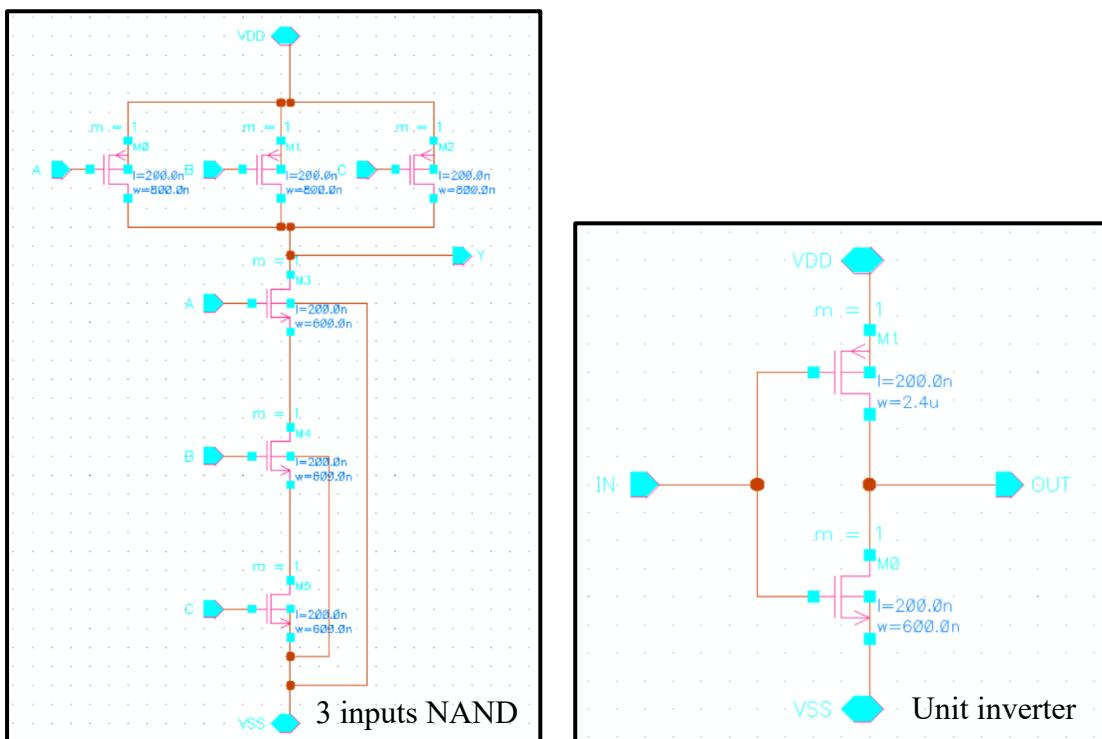


Figure 46 3 inputs NAND &unit inverter



	PMOS (W/L * m)	NMOS (W/L * m)
1 <sup>st</sup> inverter	1.8u/0.2u * 1	0.6/0.2u * 1
2 <sup>nd</sup> inverter	1.8u/0.2u * 4	0.6/0.2u * 4
3 inputs NAND	0.8u/0.2u * 1	0.6/0.2u * 1
Unit inverter	2.4u/0.2u * 1	0.6/0.2u * 1

Table 16 Each state size

- (b) Finish the layout (whole circuit, from “A” to “Out”), DRC, and LVS. Paste the photo of the layout, DRC result, and LVS result in your report. Please mark the length and width on the layout and calculate the area( $\mu\text{m}^2$ ). (15%)

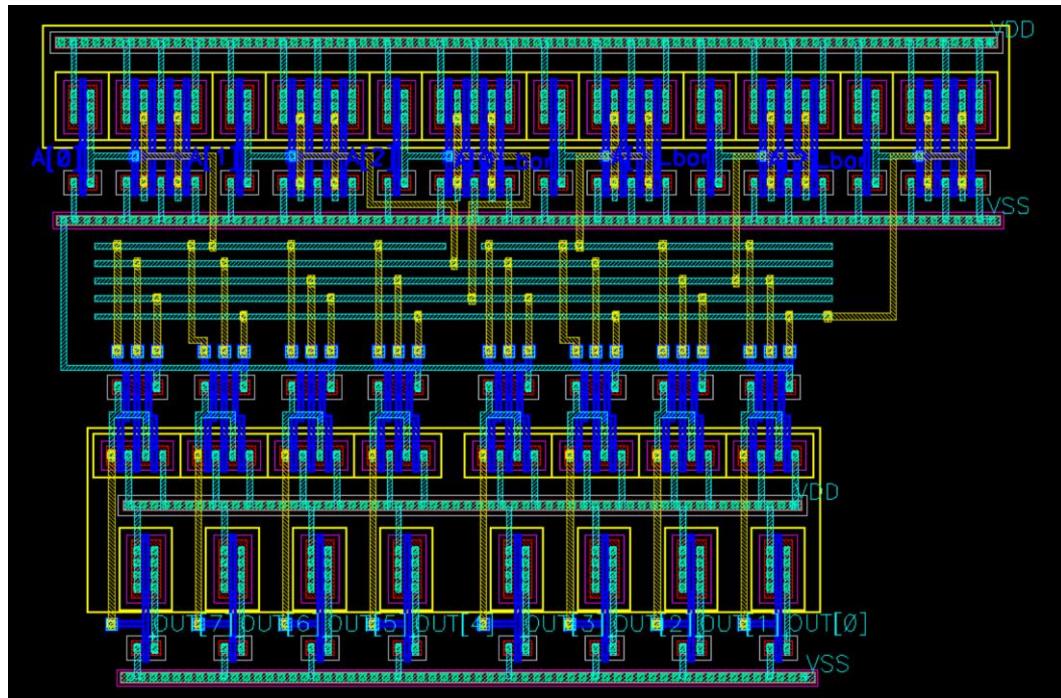
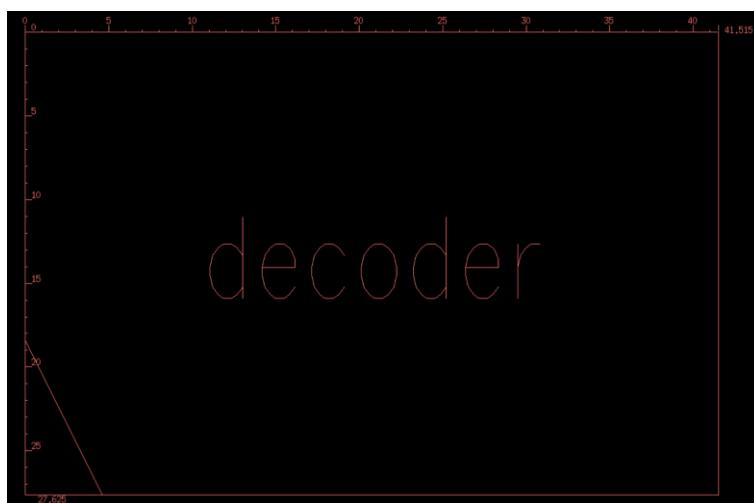


Figure 47 Layout



Length:27.625 $\mu\text{m}$   
Width:41.515 $\mu\text{m}$   
**Area = 1146.85 $\mu\text{m}^2$**

Figure 48 Area

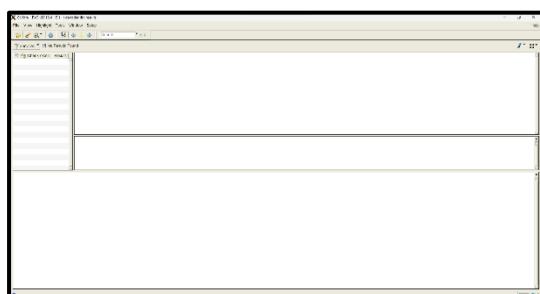


Figure 49 DRC

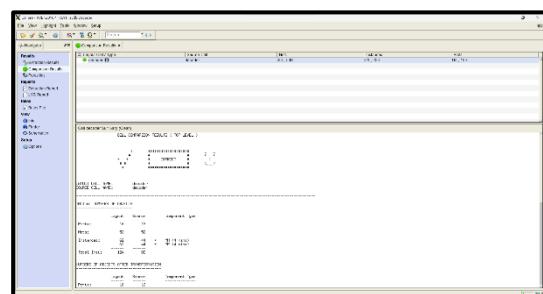


Figure 50 LVS

- (c) Run the post-layout simulation and compare it with the pre-sim. (10%)

波形由上到下分別為：

Input: VA [0]

Input: VA [0] \_bar

Input: VA [1]

Input: VA [1] \_bar

Input: VA [2]

Input: VA [2] \_bar

Output: OUT [0], OUT [1], OUT [2], OUT [3]

Output: OUT [4], OUT [5], OUT [6], OUT [7]

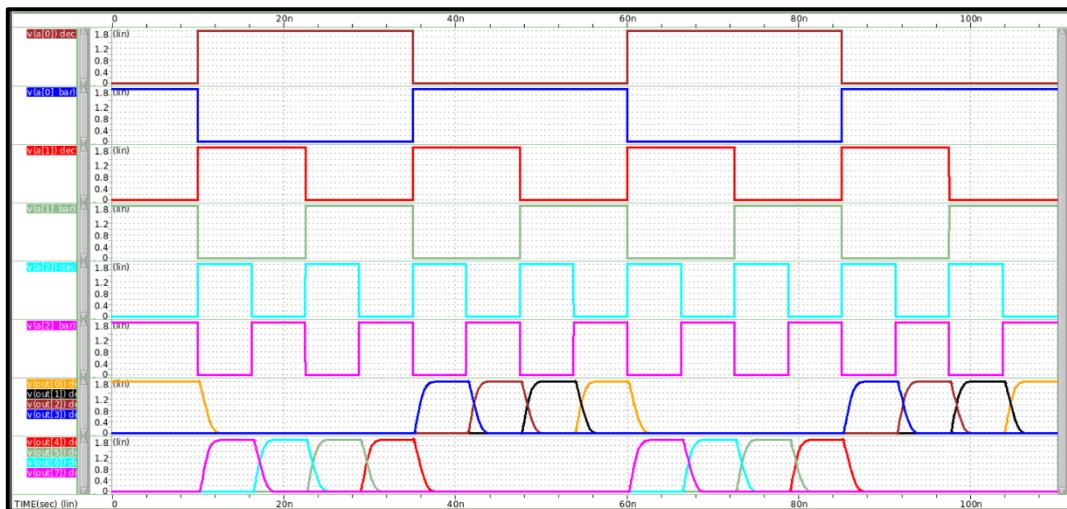


Figure 51 Pre-sim waveform

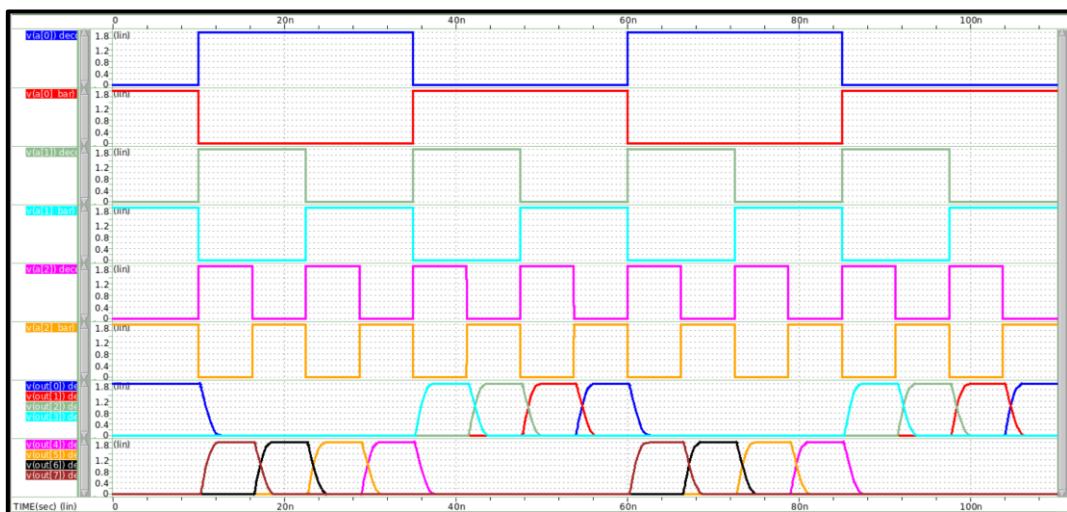


Figure 52 Post-sim waveform

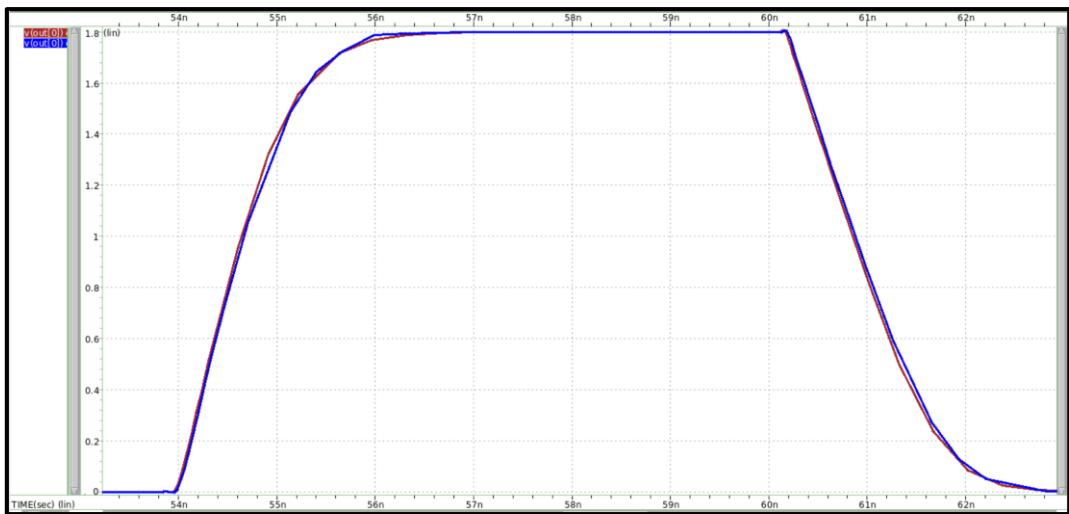


Figure 53 Compare pre-sim (brown) & post-sim (blue) in OUT [0]

Post-sim 後的波型可以發現 delay 稍微比 pre-sim 時來的大，原因我認為是，在 PEX 產生 netlist 時加入了很多寄生電容，使的整體電路的電容上升，delay 也因此上升。