

超大型積體電路設計

VLSI Design

Homework IV



國立清華大學

系所：電子所碩二

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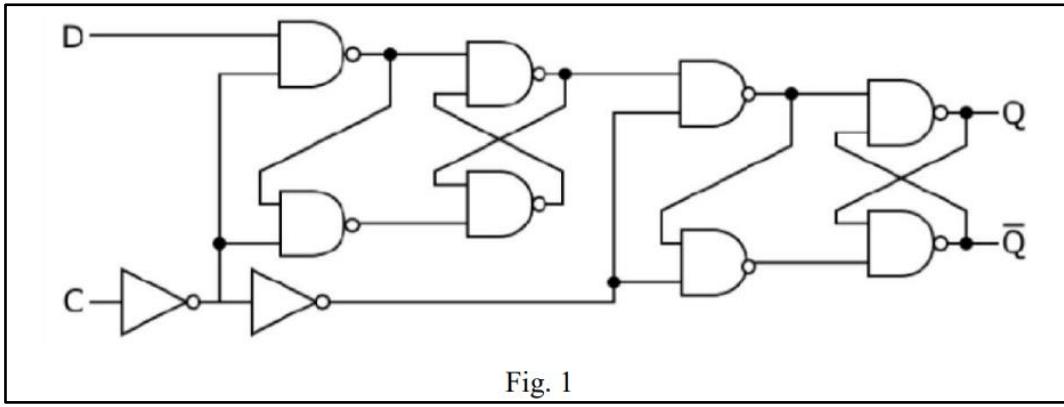
學號：111063517

授課老師：謝志成

Contents

1.	Consider a positive-edge-triggered D flip-flop as shown in Fig. 1	2
(a)	Simulate and find the setup time of this flip-flop including rising and falling input. Briefly explain what is the setup time and the way you find it. (7%)	5
(b)	Simulate and find the hold time of this flip-flop including rising and falling output. Briefly explain what is the hold time and the way you find it. (7%).....	9
(c)	Simulate the clock to Q delay for both rising and falling input transitions. (7%).....	13
(d)	Finish the layout, DRC, and LVS. Paste the photo of layout, DRC result and LVS result in your report. (8%)	15
(e)	Run the post-layout simulation (post-sim) and compare it with pre-layout simulation (pre-sim) in (a), (b), and (c). (21%).....	16
2.	Insert an inverter chain between 2 DFFs (shown in Fig.2) as a combinational logic to introduce a delay. (50%).....	20
(a)	Using the DFF you designed in previous question (15%).....	20
(b)	Using the DFF in Fig.3 and with the inverter size (W/L) n = 0.6um/0.2um and (W/L) p = 1.8um/0.2um, the transmission gate size (W/L) n = (W/L) p = 0.8um/0.2um. (15%)..	24
(c)	Use the previous results in question1 (setup time and hold time) to hand calculate the maximum and minimum delay failure condition in (a). As for (b), do the same hand calculation as (a). (10%).....	32
(d)	Please compare and comment the results of (a) and (b) with (c). (10%).....	33

1. Consider a positive-edge-triggered D flip-flop as shown in Fig. 1.



180nm:

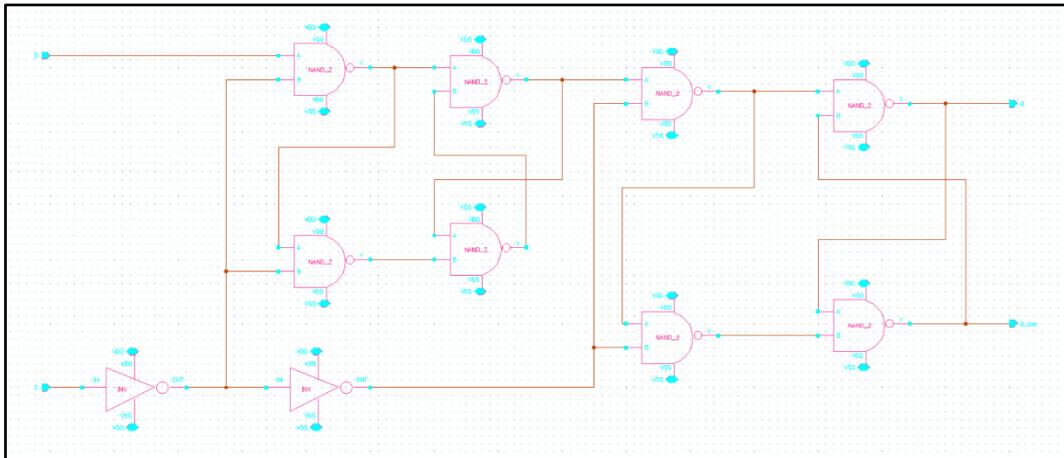


Figure 1 Schematic

Size	Inverter	2-inputs NAND
PMOS	1.8u/0.18u, m = 1	1.73u/0.18u, m = 1
NMOS	0.6u/0.18u, m = 1	1.2u/0.18u, m = 1

Table 1 Size

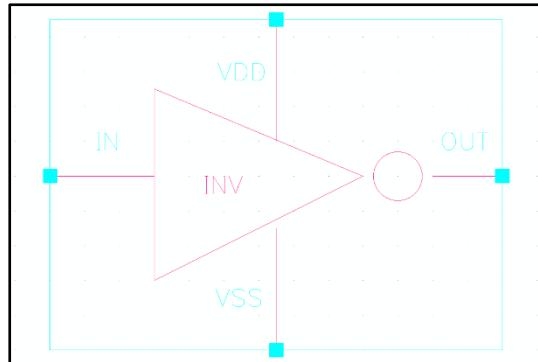


Figure 2 Inverter symbol

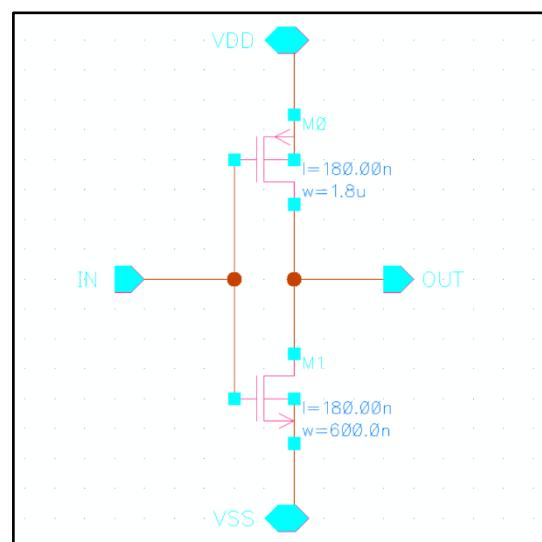


Figure 3 Inverter schematic

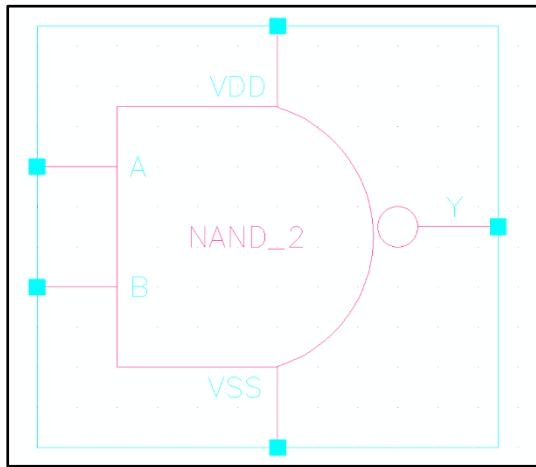


Figure 4 2-inputs NAND symbol

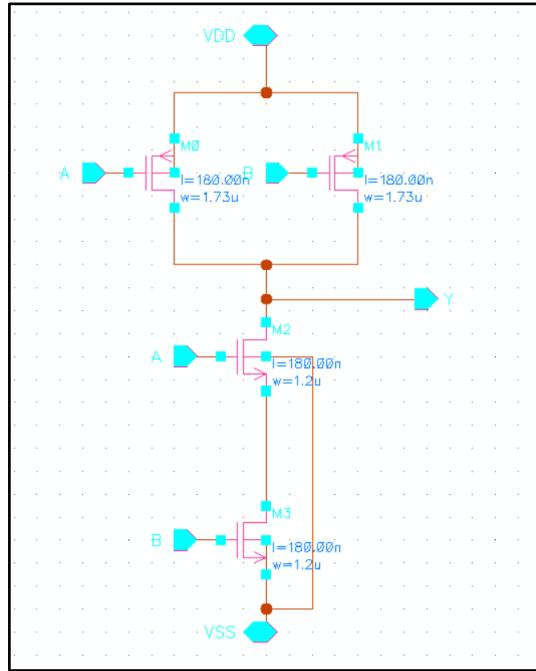


Figure 5 2-inputs NAND schematic

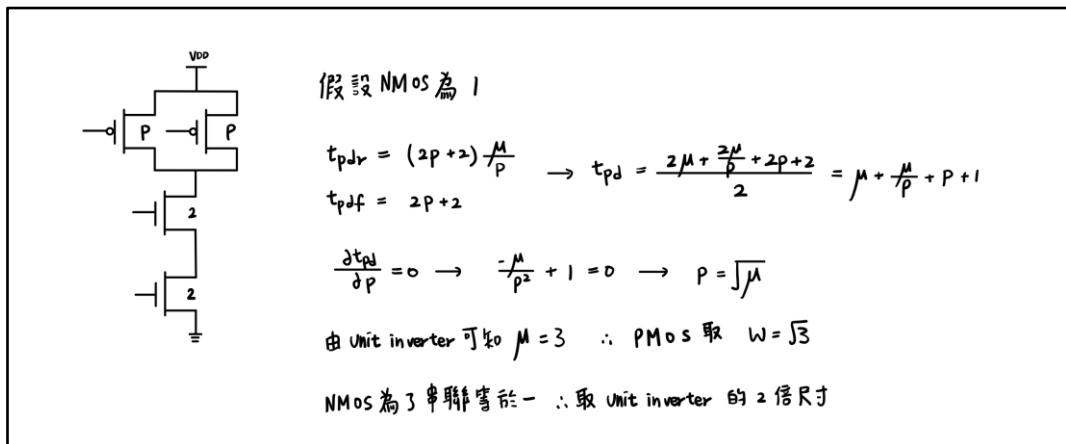


Figure 6 Calculate 2-inputs NAND size

14nm:

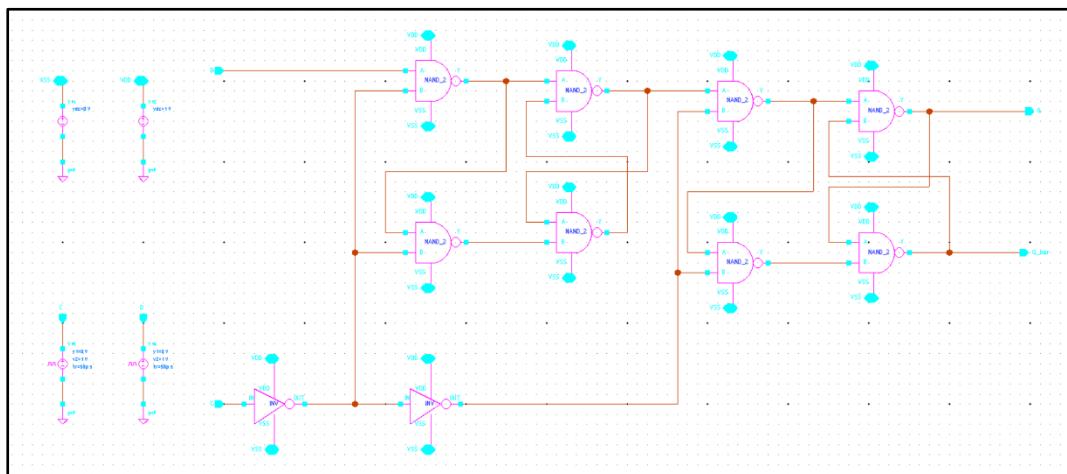


Figure 7 Schematic

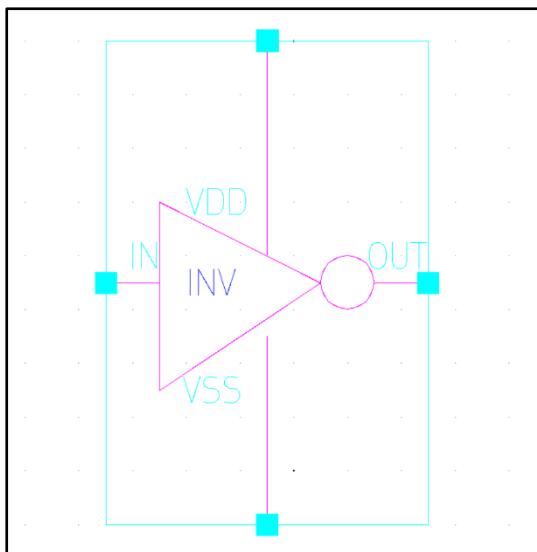


Figure 8 Inverter symbol

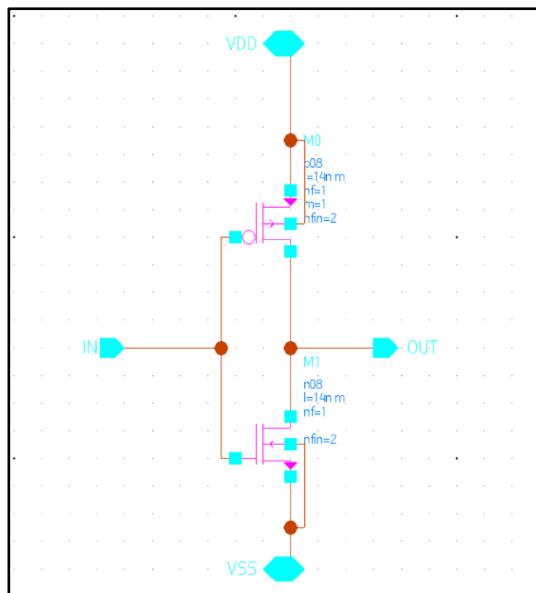


Figure 9 Inverter schematic

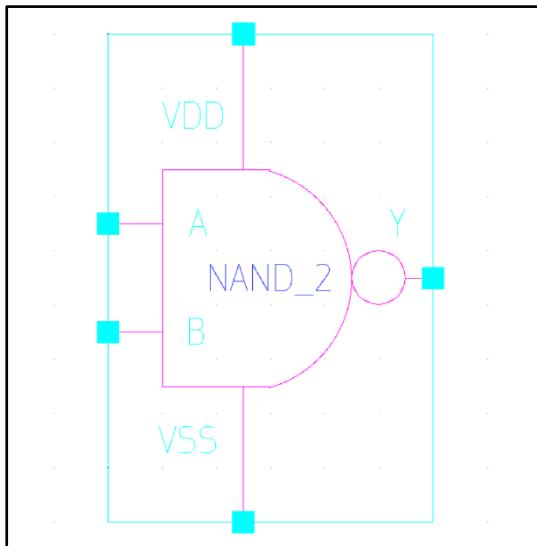


Figure 10 2-inputs NAND symbol

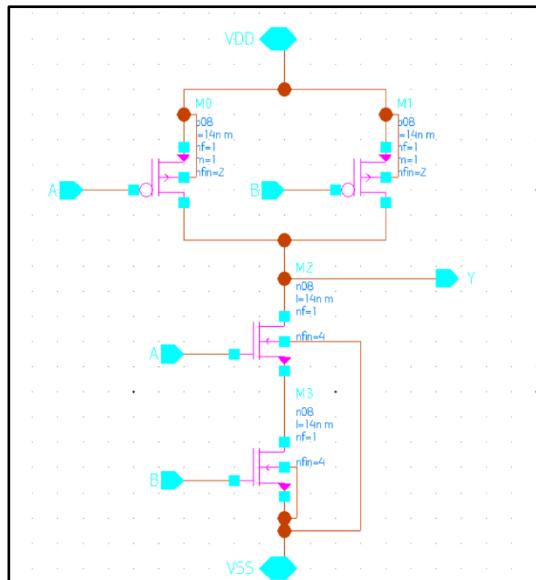


Figure 11 2-inputs NAND schematic

Size	Inverter	2-inputs NAND
PMOS (nfin)	2	2
NMOS (nfin)	2	4

Table 2 Size

- (a) Simulate and find the setup time of this flip-flop including rising and falling input. Briefly explain what is the setup time and the way you find it. (7%)

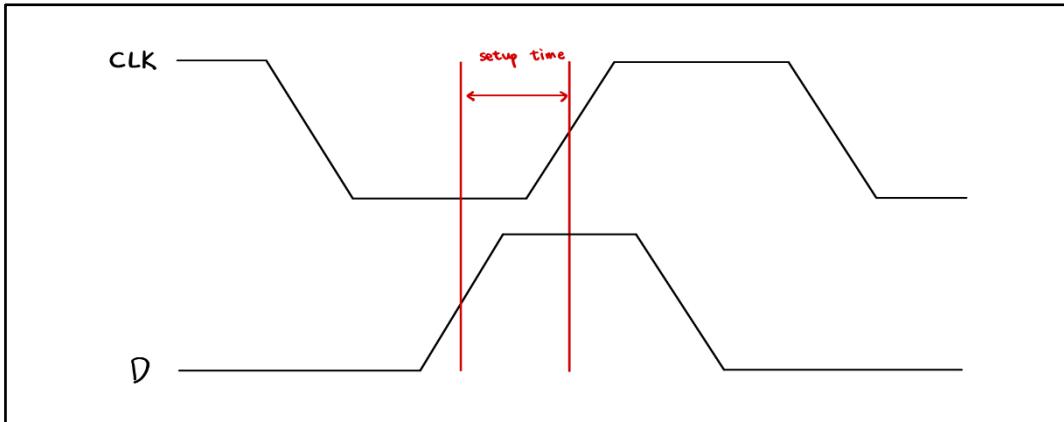


Figure 12 Setup time

Setup time 為 **CLK edge 前**，data 維持穩定的時間，以 data rising 為例，本題是 positive CLK，故 setup time 定義為 data 上升到 $0.5VDD$ 到 CLK 上升為 $0.5VDD$ 的時間，若 data 的頻率太快，週期太短，在 setup time 裡轉態的話，電路會因同時有兩個相反的輸入，導致 setup time violation，輸出無法正常拉起。

180nm:

The way to find setup time:

使用 sweep 的方法，將輸入的 data period 從 9.9ns 每次 0.001ns 的 step 掃描到 10.1ns ，找出 setup time 最小值的瞬間，Pwidth 設定 0.5period 確保 hold time 時間足夠。

由 Figure13 可知 data 在 period 為 9.996ns 為 rising setup time 的極限值， 9.967ns 時會發生 setup time violation。

由 Figure14 可知 data 在 period 為 9.925ns 為 falling setup time 的極限值， 9.926ns 時會發生 setup time violation。

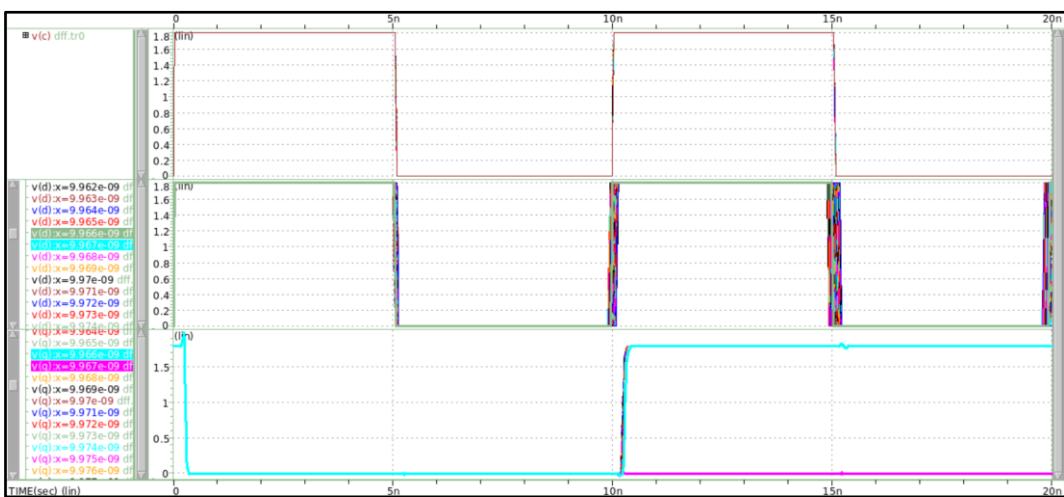


Figure 13 Rising input setup time

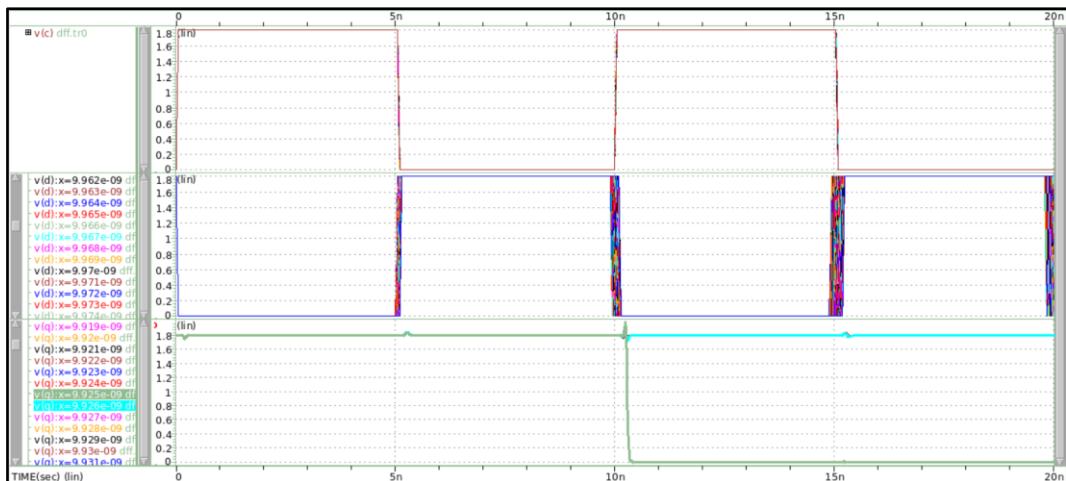


Figure 14 Falling input setup time

Result:

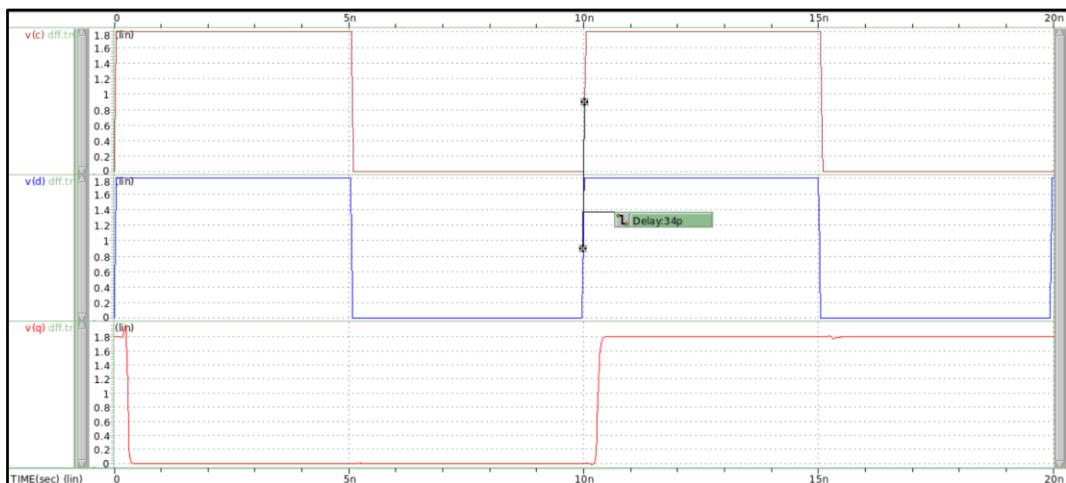


Figure 15 Rising input at 9.966ns period

由 Figure15 可知 data 在 period 為 9.996ns 時，rising setup time = 34ps。

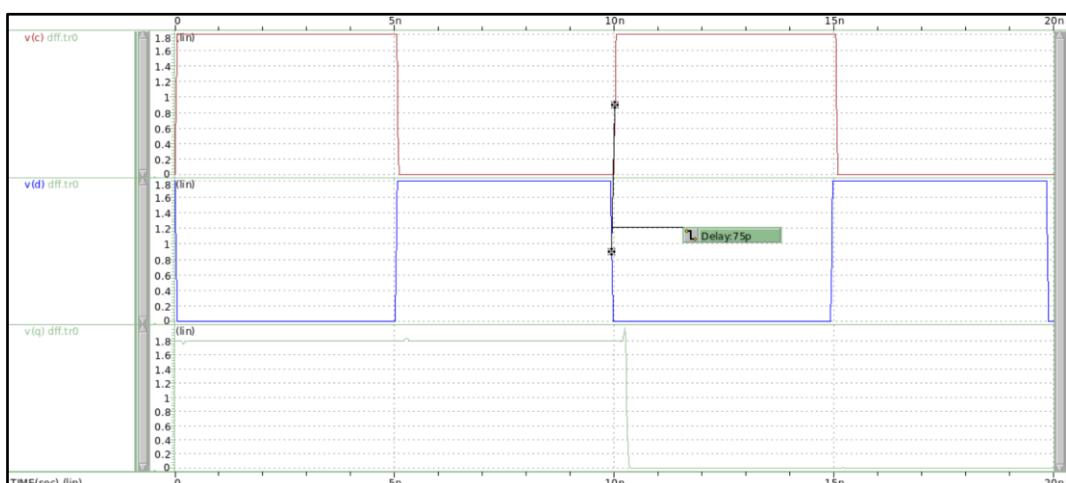


Figure 16 Falling input at 9.925ns period

由 Figure16 可知 data 在 period 為 9.925ns 時，falling setup time = 75ps。

14nm:

The way to find setup time:

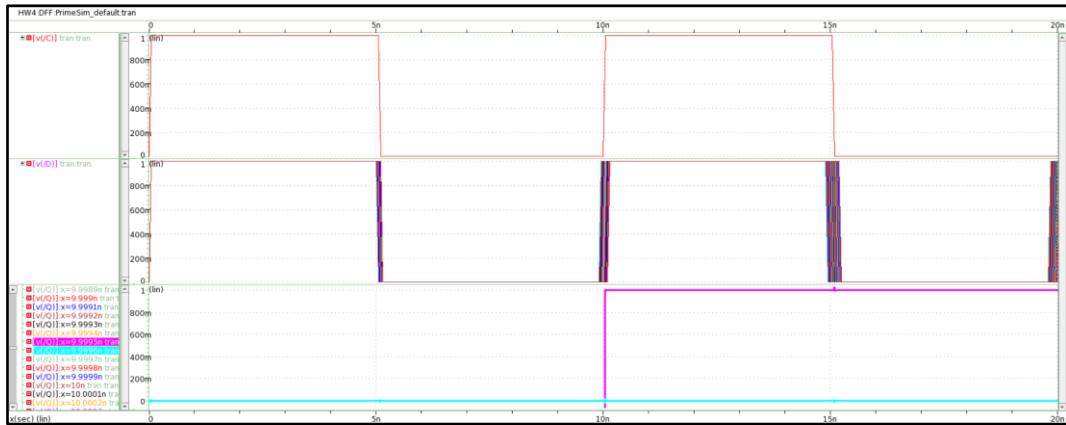


Figure 17 Find rising setup time

在 period 為 9.9995ns 時，有足夠的 setup time。

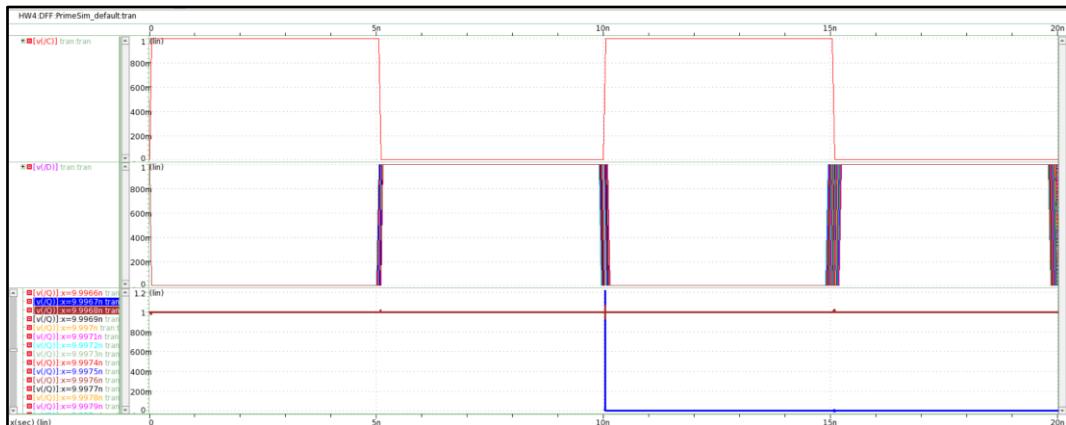


Figure 18 Find falling setup time

在 period 為 9.9967ns 時，有足夠的 setup time。

Result:

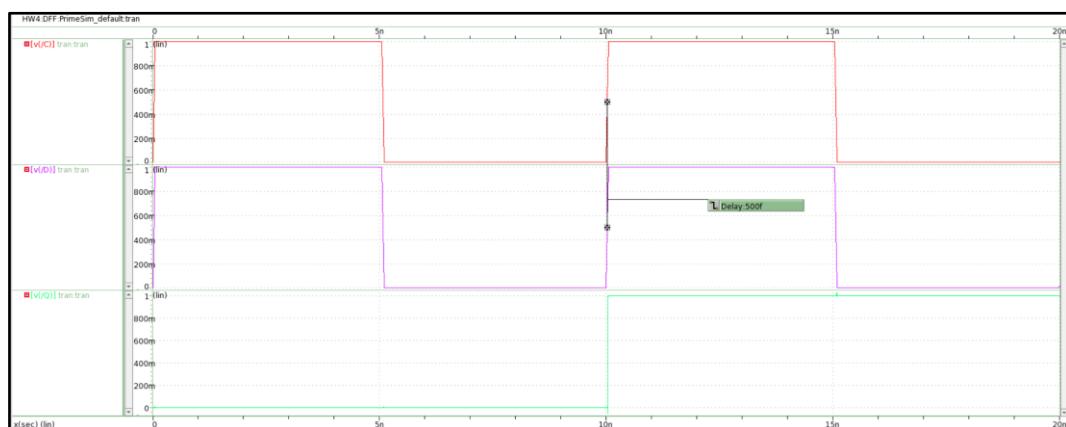


Figure 19 Rising input at 9.9995ns period

由 Figure19 可知 data 在 period 為 9.9995ns 時，rising setup time = 0.5ps

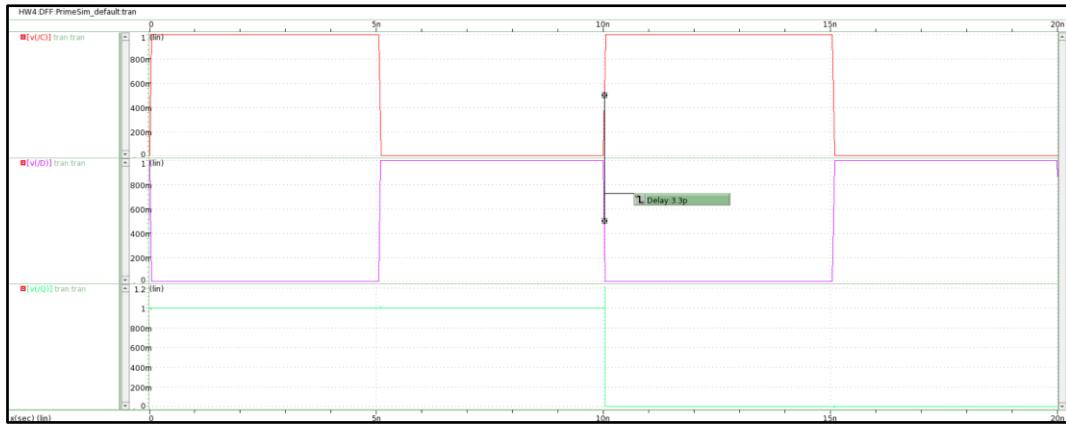


Figure 20 Falling input at 9.9968ns period

由 Figure20 可知 data 在 period 為 9.9968ns 時，falling setup time = 3.3ps

Setup time	Rising	Falling
180nm	34ps	75ps
14nm	0.5ps	3.3ps

Table 3 Compared setup time between 180nm & 14nm

從結果來看，因為製程的縮小，故電路的 setup time 也因此縮短了很多。

- (b) Simulate and find the hold time of this flip-flop including rising and falling output. Briefly explain what is the hold time and the way you find it. (7%)

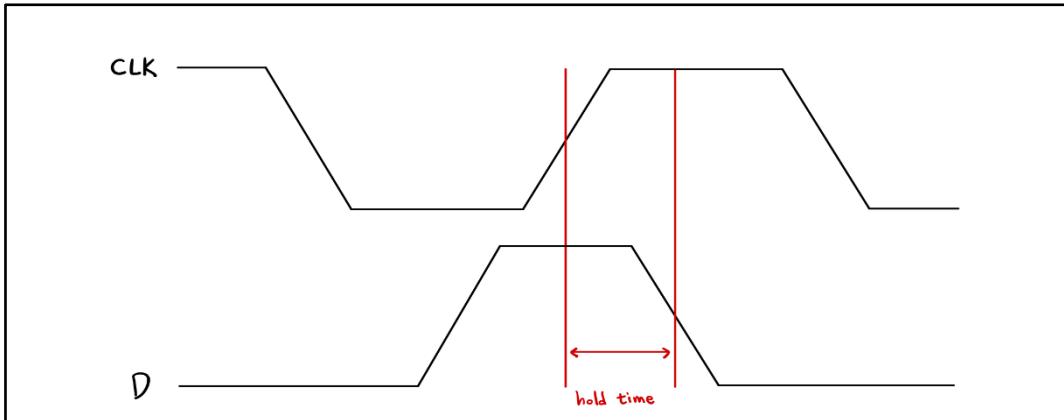


Figure 21 Hold time

Hold time 為 **CLK edge** 後，data 維持穩定的時間，以 data rising 為例，本題是 positive CLK，故 hold time 定義為 CLK 上升為 0.5VDD 的時間到 data 下降到 0.5VDD，若 data 的頻率太快，週期太短，在 hold time 裡轉態的話，電路會因同時有兩個相反的輸入，導致 hold time violation，輸出無法正常拉起。

180nm:

The way to find hold time:

使用 sweep 的方法，將輸入的 data period 固定在(a)小題的 setup time(代表時間是足夠的)，再將 period width 從 0.05ns 每次 0.001ns 的 step 掃描 1ns，找出 hold time 最小值的瞬間。

由 Figure22 可知 data 在 period 為 0.09ns 為 rising hold time 的極限值，0.089ns 時會發生 hold time violation。

由 Figure23 可知 data 在 period 為 0.057ns 為 falling hold time 的極限值，0.056ns 時會發生 hold time violation。

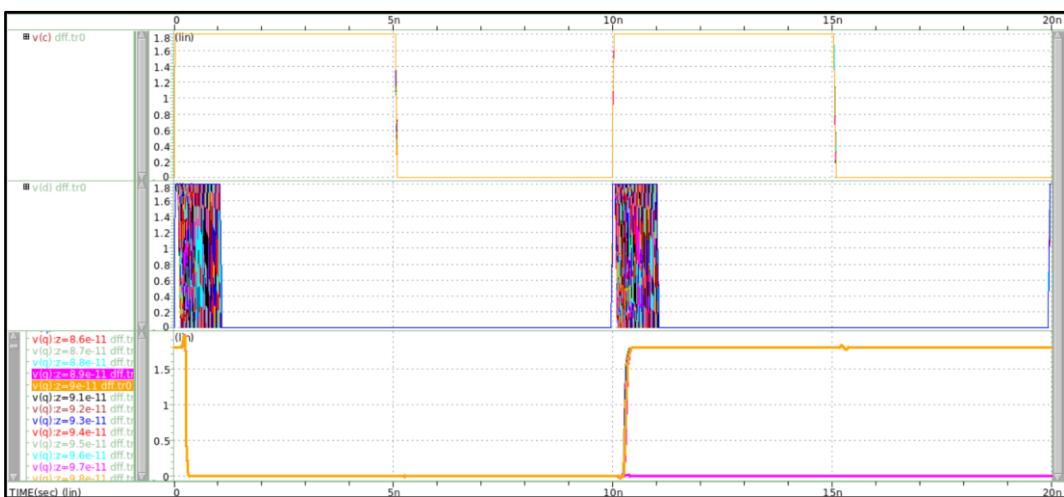


Figure 22 Rising input hold time

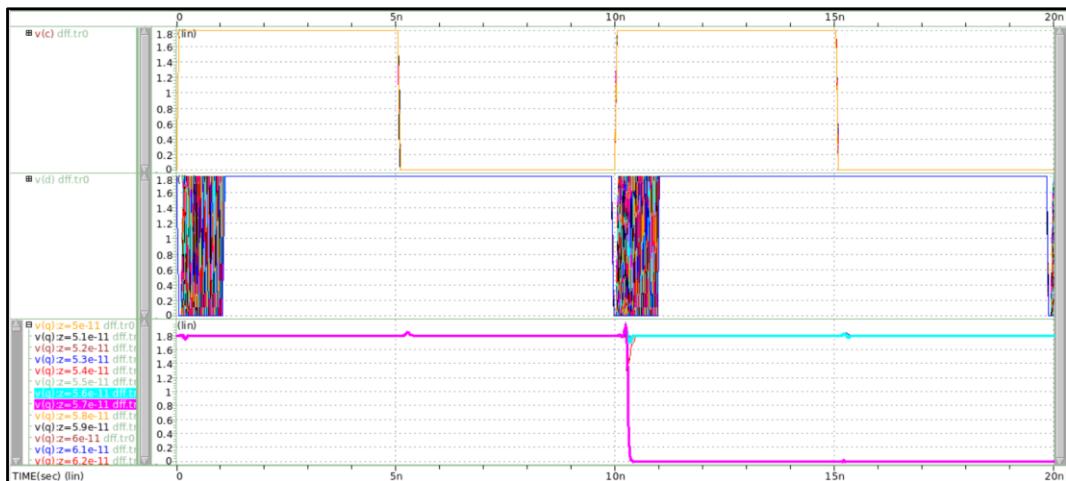


Figure 23 Falling input hold time

Result:

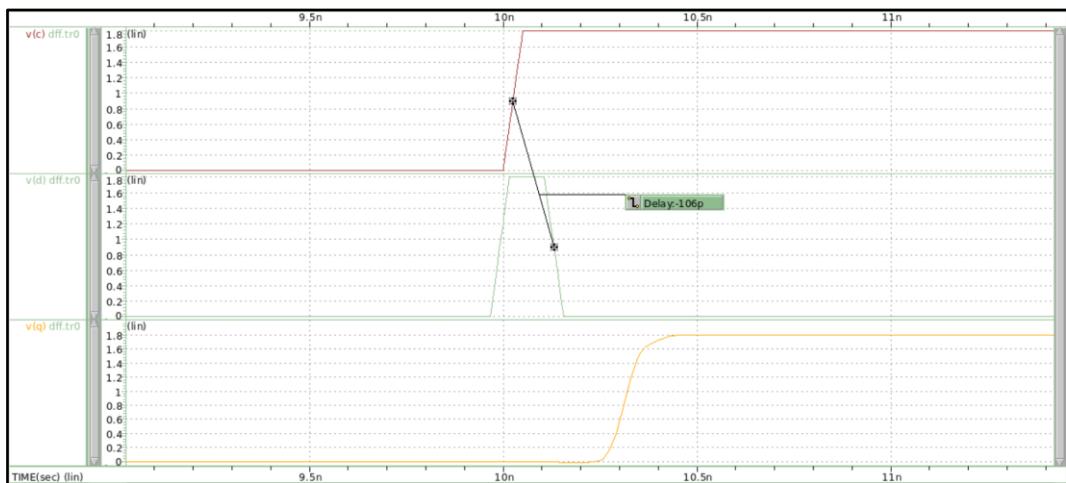


Figure 24 Rising input at 0.09ns period width

由 Figure24 可知 data 在 periodwidth 為 0.09ns 時，rising hold time = 106ps。

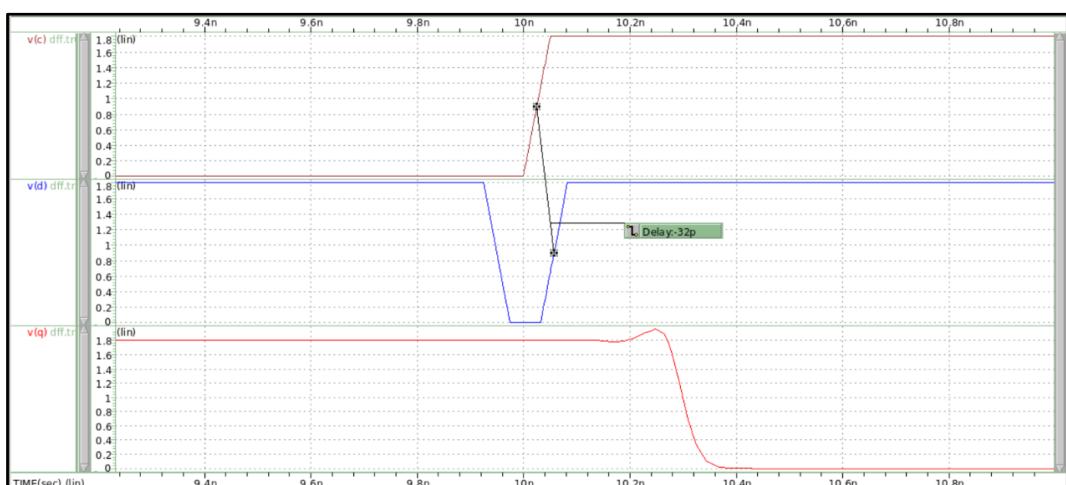


Figure 25 Falling input at 0.057ns period width

由 Figure25 可知 data 在 periodwidth 為 0.057ns 時，rising hold time = 32ps。

14nm:

The way to find hold time:

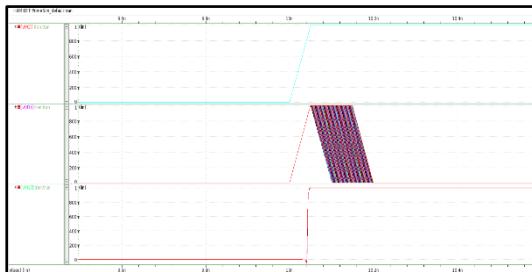


Figure 26 Rising with no delay



Figure 27 Falling with no delay

從 figure26 和 27 可以發現在 14nm 的 hold time 可能是負值，因為正常 sweep 掃描都不會出現 time violation 的週期，故下方的 hold time 我將 CLK 延遲了 1ns 來尋找 hold time。

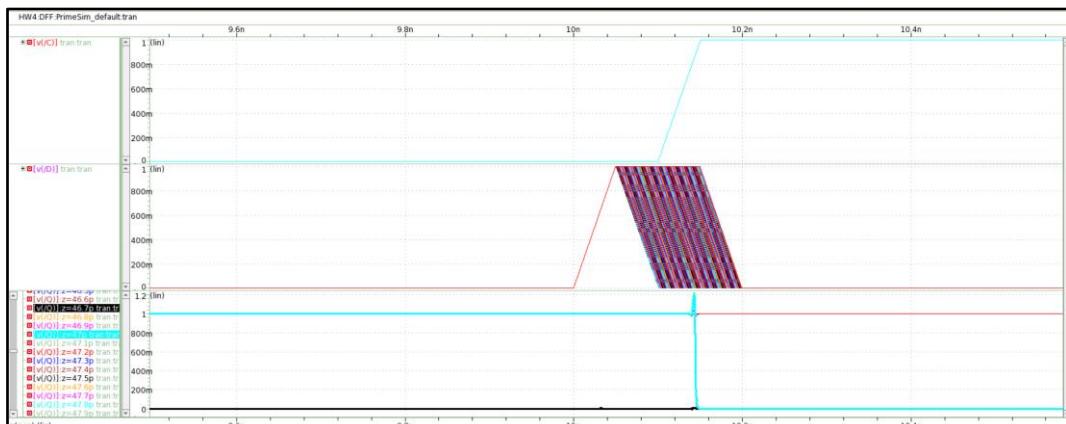


Figure 28 Find rising hold time

在 period width= 0.047ns 時，有足夠的 hold time。



Figure 29 Find falling hold time

在 period width= 0.052ns 時，有足夠的 hold time。

Result:

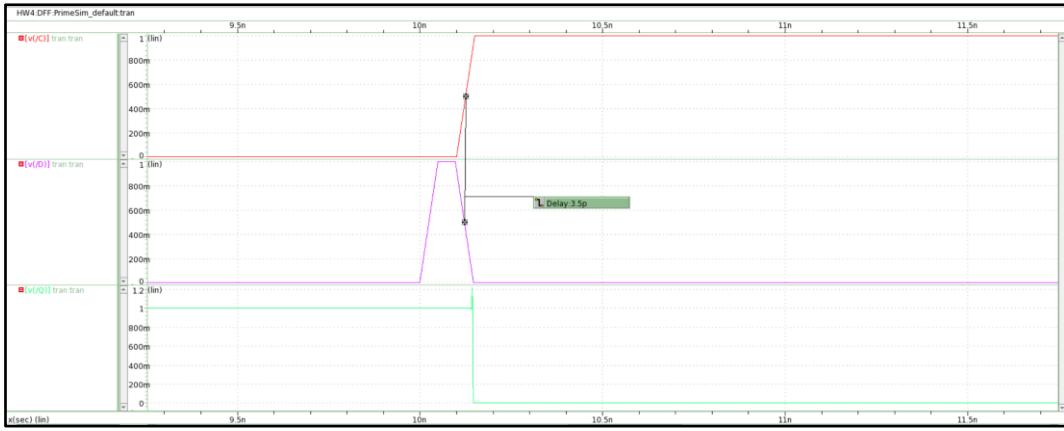


Figure 30 Rising input at 0.047ns period width

由 Figure30 可知 data 在 periodwidth 為 0.047ns 時，rising hold time = -3.5ps。

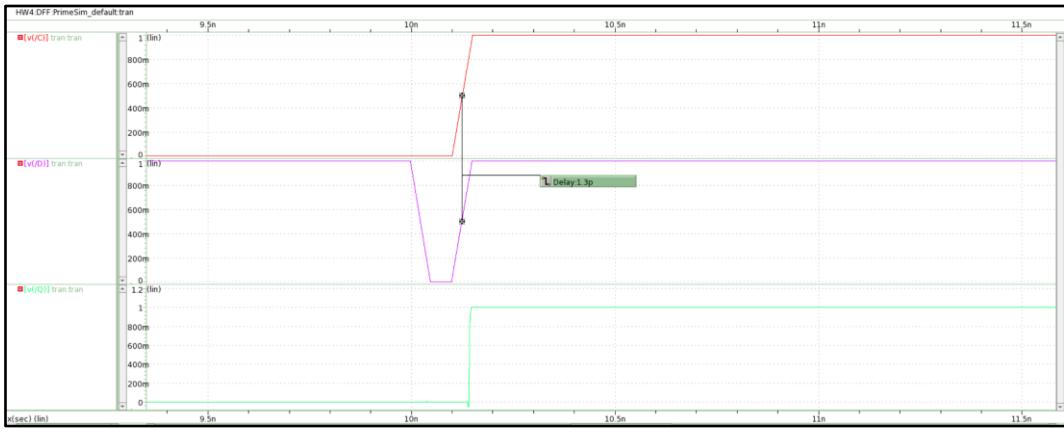


Figure 31 Falling input at 0.052ns period width

由 Figure31 可知 data 在 periodwidth 為 0.047ns 時，rising hold time = -1.3ps。

Setup time	Rising	Falling
180nm	106ps	32ps
14nm	-3.5ps	-1.3ps

Table 4 Compared hold time between 180nm & 14nm

從結果來看，因為製程的縮小，故電路的 hold time 也因此縮短了很多，甚至出現負值，hold time 出現負值代表輸入在 posedge 前就已經有改變，但在電路上還是辨識到改變前的訊號，也就是正確的訊號，造成這現象的原因可能是 CLK 的內部 delay。

(c) Simulate the clock to Q delay for both rising and falling input transitions. (7%)

180nm:

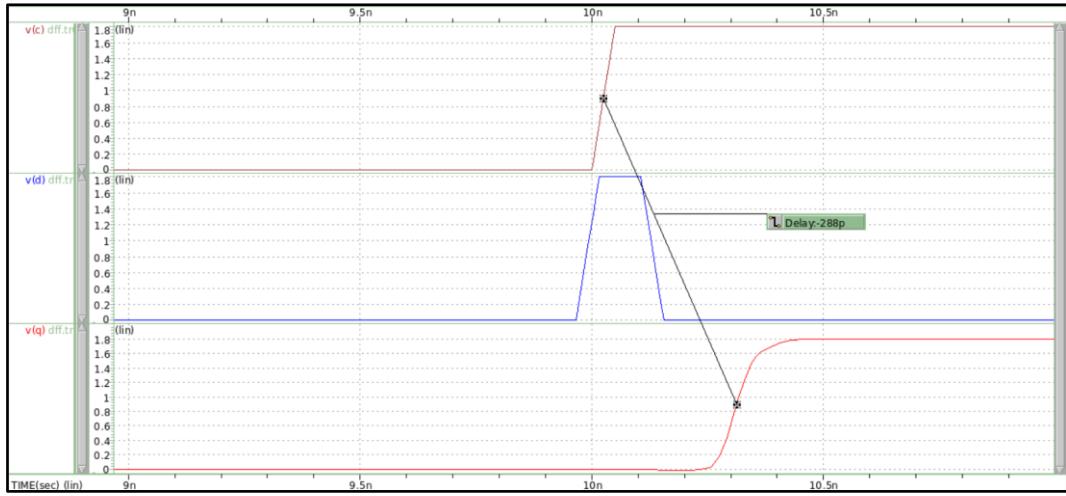


Figure 32 Rising input Tcq

Tcq for rising input = 288ps

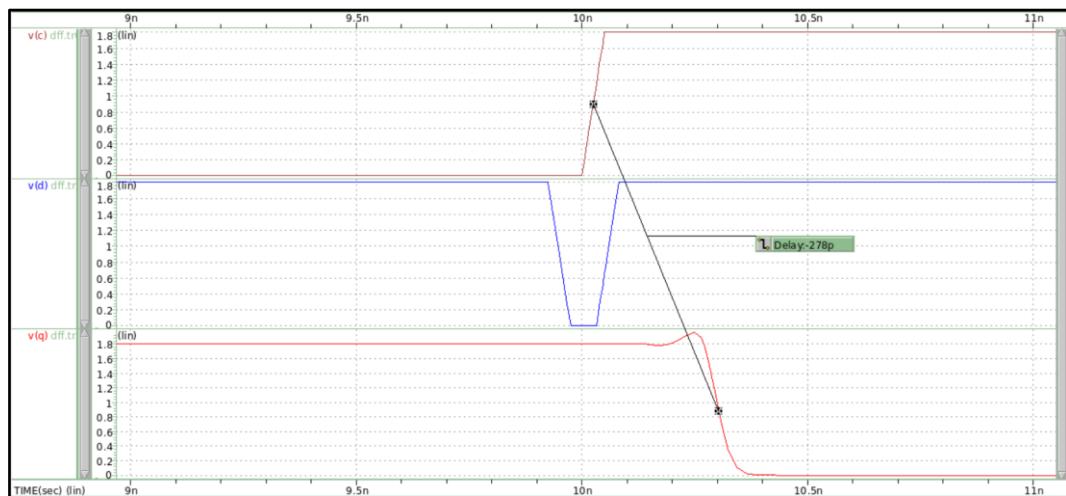


Figure 33 Falling input Tcq

Tcq for falling input = 278ps

14nm:

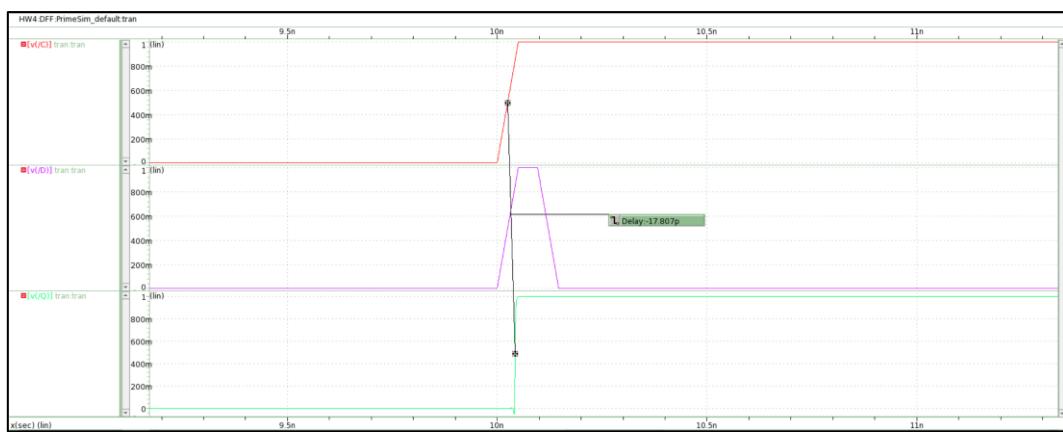


Figure 34 Rising input Tcq
Tcq for rising input = 17.807ps

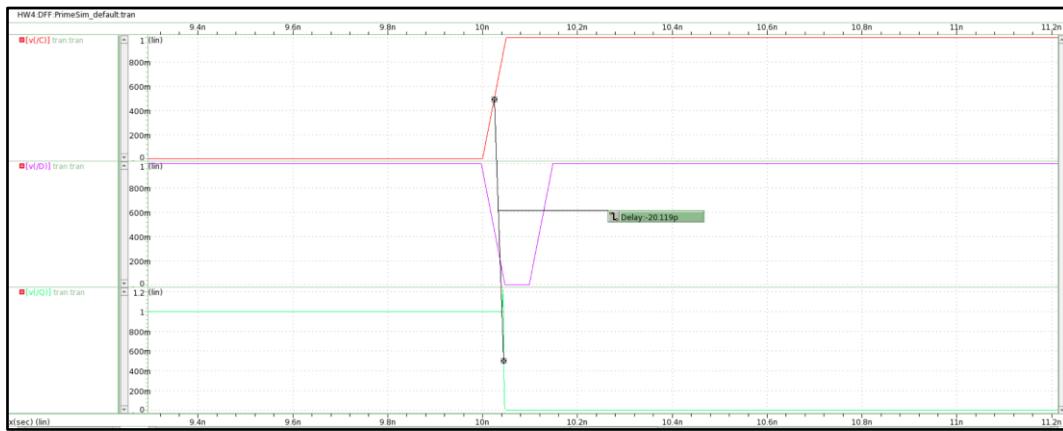


Figure 35 Falling input Tcq
Tcq for falling input = 20.119ps

Setup time	Rising	Falling
180nm	288ps	278ps
14nm	17.807ps	20.119ps

Table 5 Compared Tcq between 180nm & 14nm

- (d) Finish the layout, DRC, and LVS. Paste the photo of layout, DRC result and LVS result in your report. (8%)

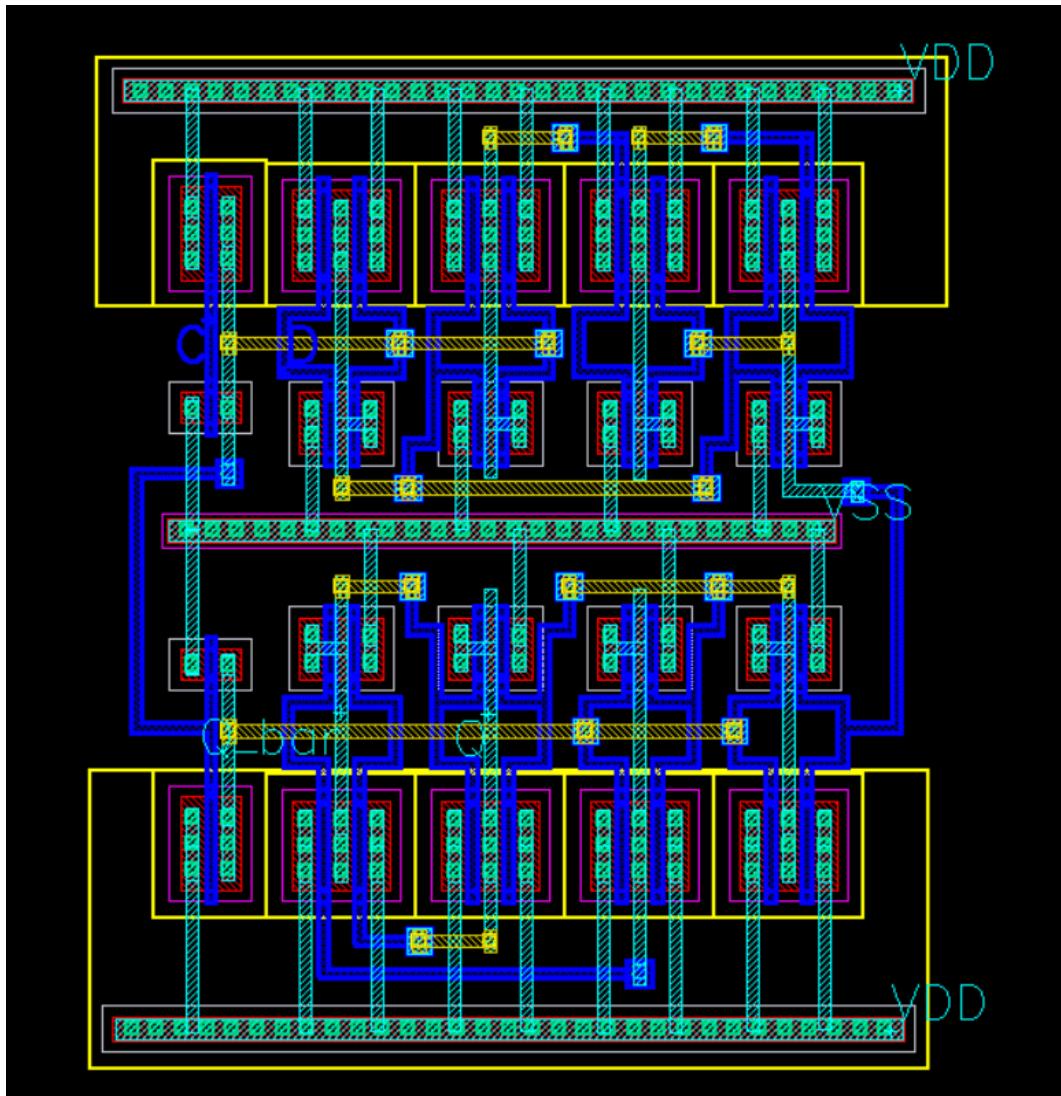


Figure 36 Layout

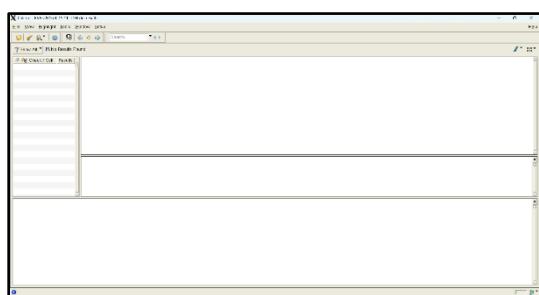


Figure 37 DRC

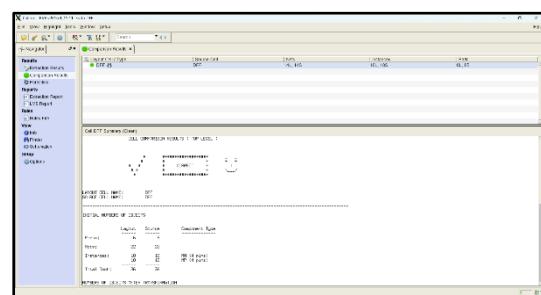


Figure 38 LVS

- (e) Run the post-layout simulation (post-sim) and compare it with pre-layout simulation (pre-sim) in (a), (b), and (c). (21%)

Setup time:

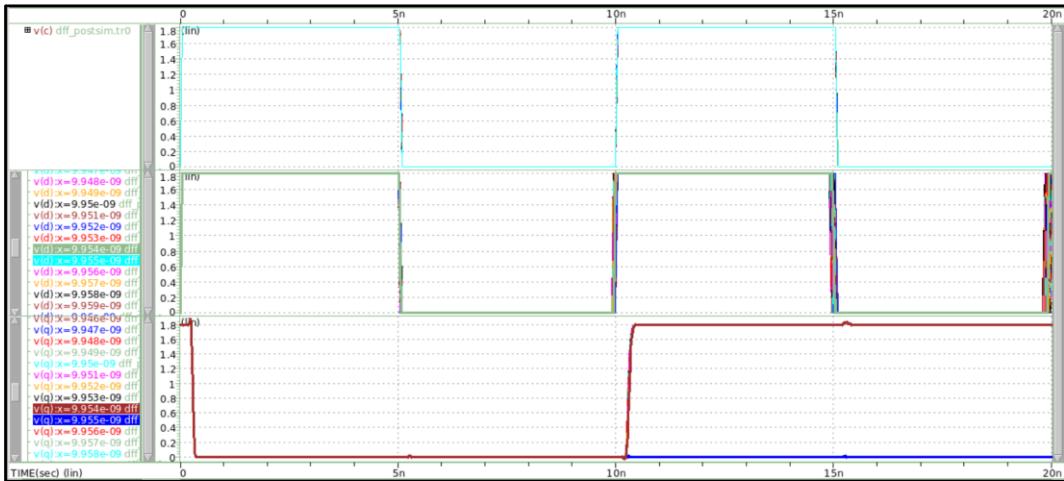


Figure 39 Sweep period for rising input

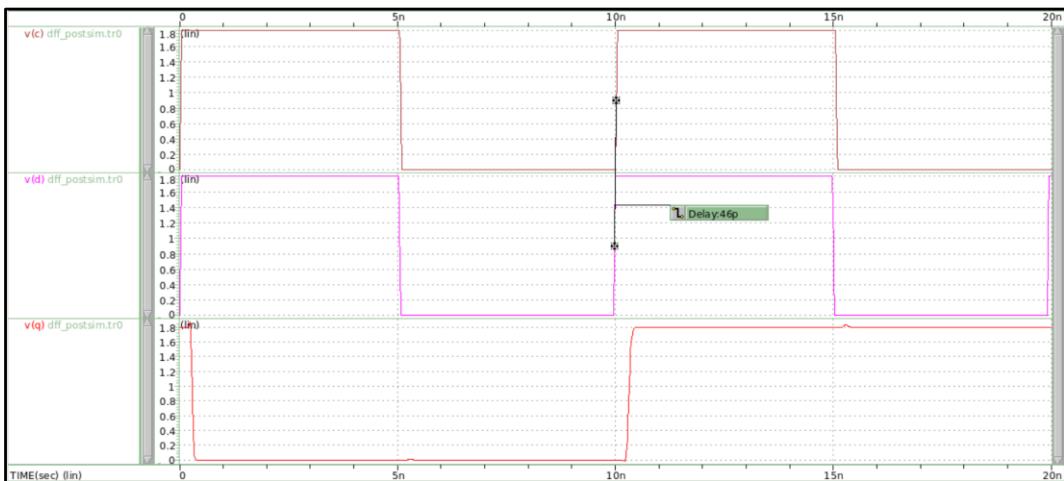


Figure 40 Rising input at 9.954ns period

Rising setup time = 46ps

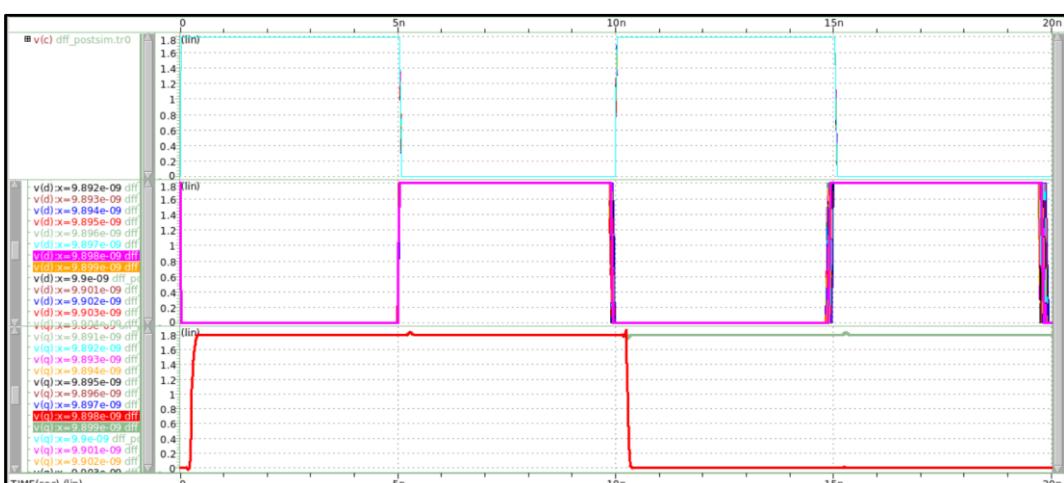


Figure 41 Sweep period for falling input

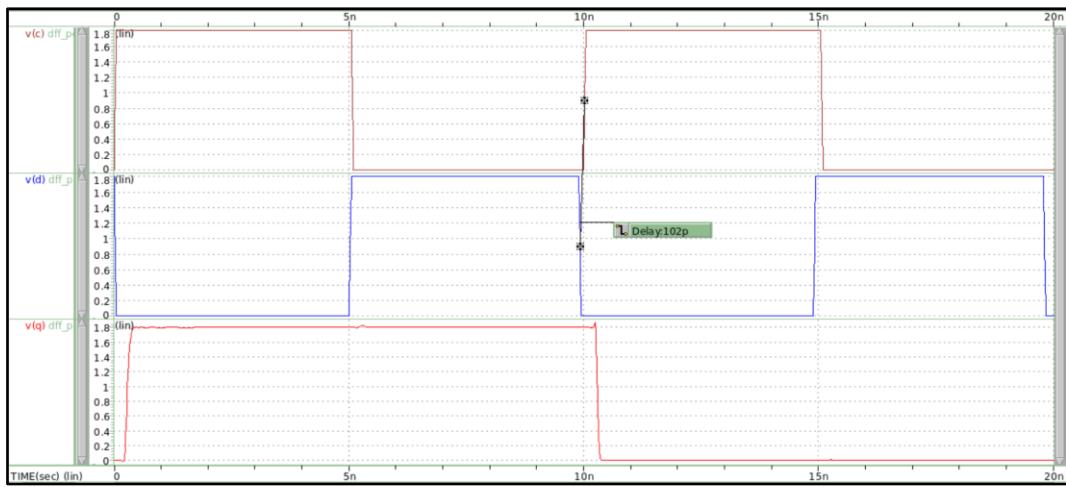


Figure 42 Falling input at 9.898ns period

Falling setup time = 102ps

Hold time:

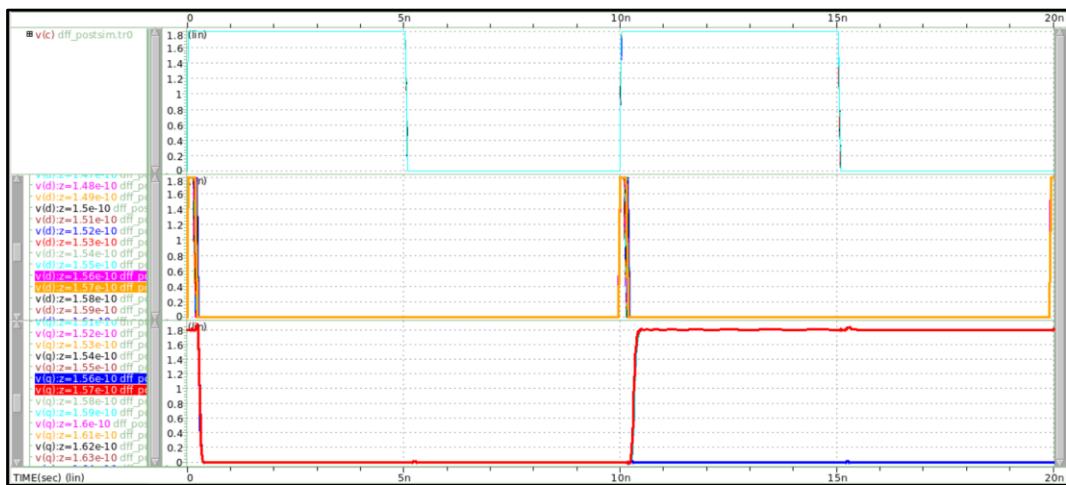


Figure 43 Sweep period width for rising input

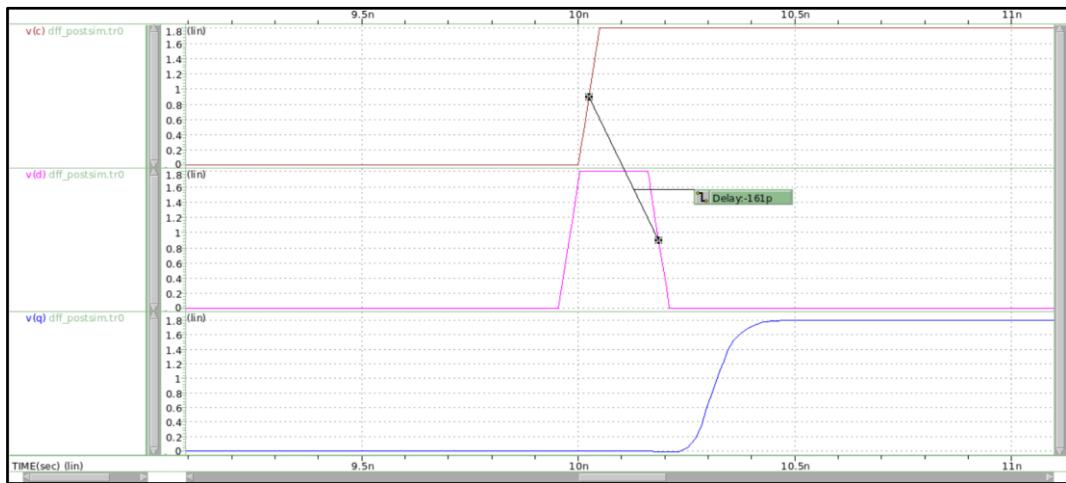


Figure 44 Rising input at 0.157ns period width

Rising hold time = 161ps

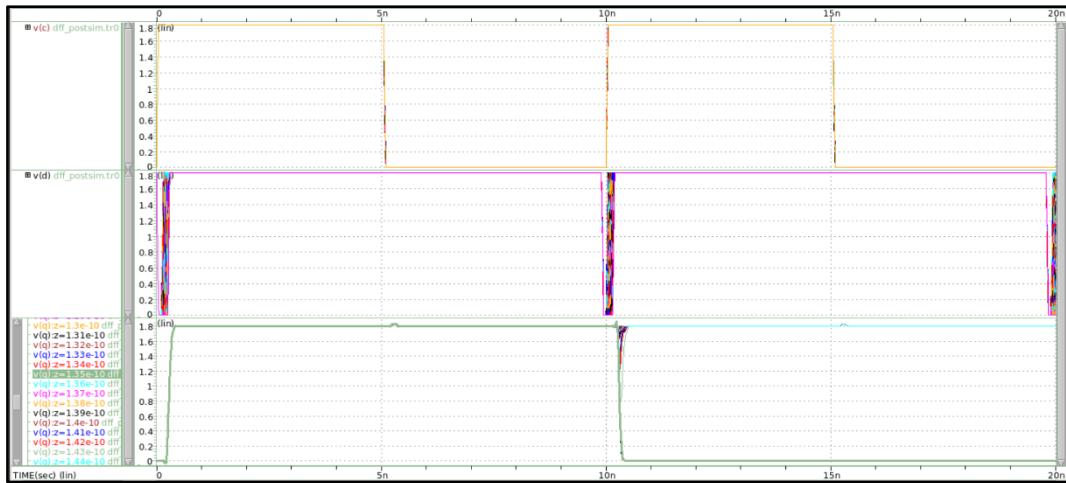


Figure 45 Sweep period width for falling input

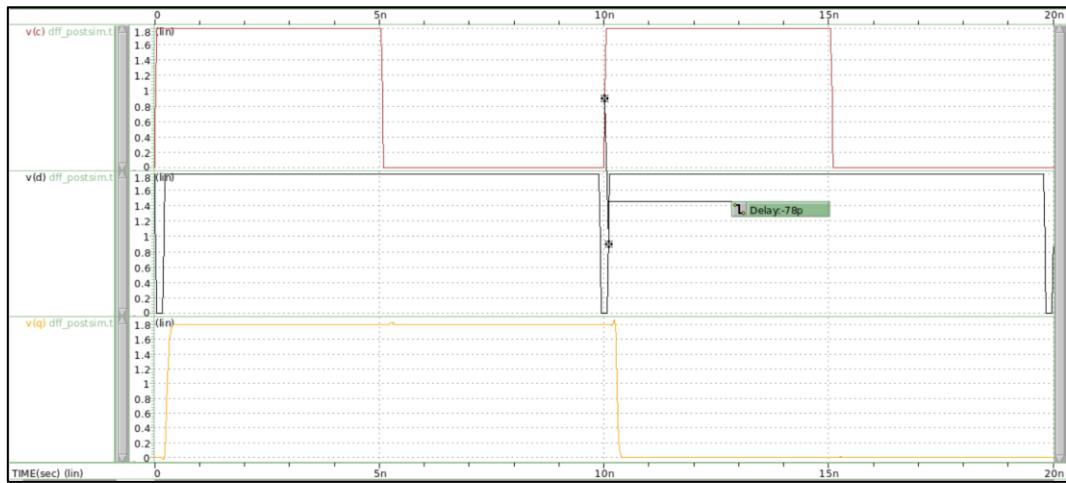


Figure 46 Falling input at 0.13ns period width

Falling hold time = 78ps

Tcq:

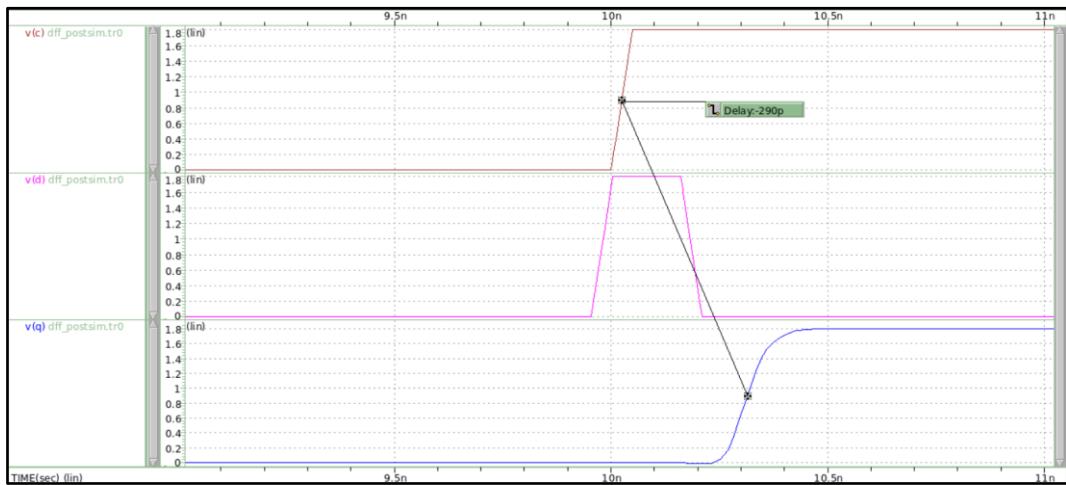


Figure 47 Rising input Tcq

Tcq for rising input = 290ps

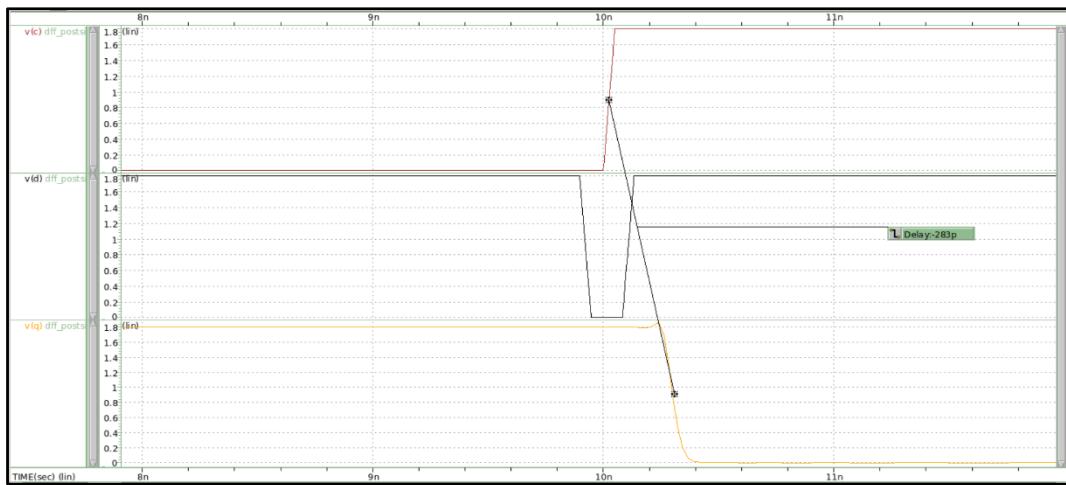


Figure 48 Falling input Tcq
Tcq for falling input = 283ps

	Input type	Presim	Postsim
Setup time	rising	34ps	46ps
	falling	75ps	102ps
Hold time	rising	106ps	161ps
	falling	32ps	78ps
Tcq	rising	288ps	290ps
	falling	278ps	283ps

Table 6 Compared presim & postsim

Postsim 因為加入寄生電容和一些電阻，所以 setup time 和 hold time 的時間都比 presim 長，Tcq 也較大。

2. Insert an inverter chain between 2 DFFs (shown in Fig.2) as a combinational logic to introduce a delay. (50%)

clk = 100MHz with $t_r = t_f = 50\text{ps}$, duty cycle = 50% and VDD = 1.8V

Simulate and observe the maximum and minimum delay failure condition while input = vdd and input = gnd.

- (a) Using the DFF you designed in previous question (15%)

$$T_{pd} \leq T_c - (T_{setup} + T_{pcq})$$

$$T_{cd} \geq T_{hold} - T_{ccq}$$

	Rising input	Falling input
T _{setup}	34ps	75ps
T _{hold}	106ps	32ps
T _{cq}	288ps (T _{pcq})	278ps (T _{ccq})
Max T _{pd}	9.678ns	
Min T _{cd}	-246ns	

Table 7 Calculate Max T_{pd} & T_{cd}

從計算結果可知 propagation delay 至少需要 9.678ns，如果大於的話會導致第二個 DFF 的 setup time 不足，輸出結果會出現 violation；contamination delay < 0ps，代表沒有提供 delay 也不會有 violation。

Maximum propagation delay

Input = VDD:

為了測試 combination logic 可以接受的 propagation delay 有多長，我採用了 2 組不同的 combination logic，分別是加了 4 顆和 6 顆 inverter 的電路，並加入 1pF 的電容製造 propagation delay，模擬結果如下。

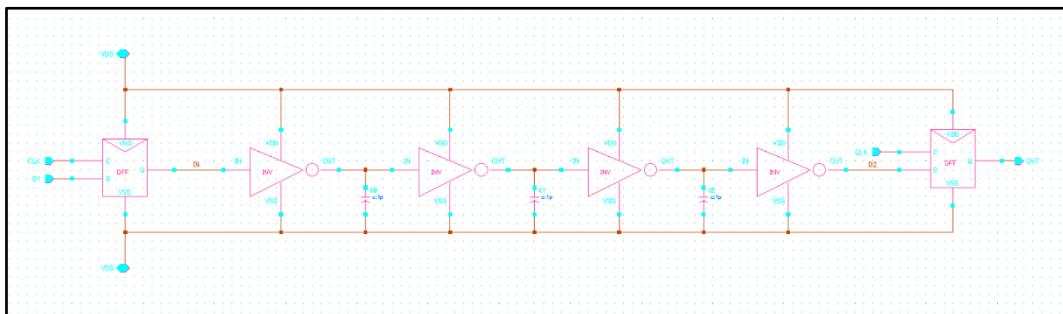


Figure 49 DFF + 4 inverter chain schematic

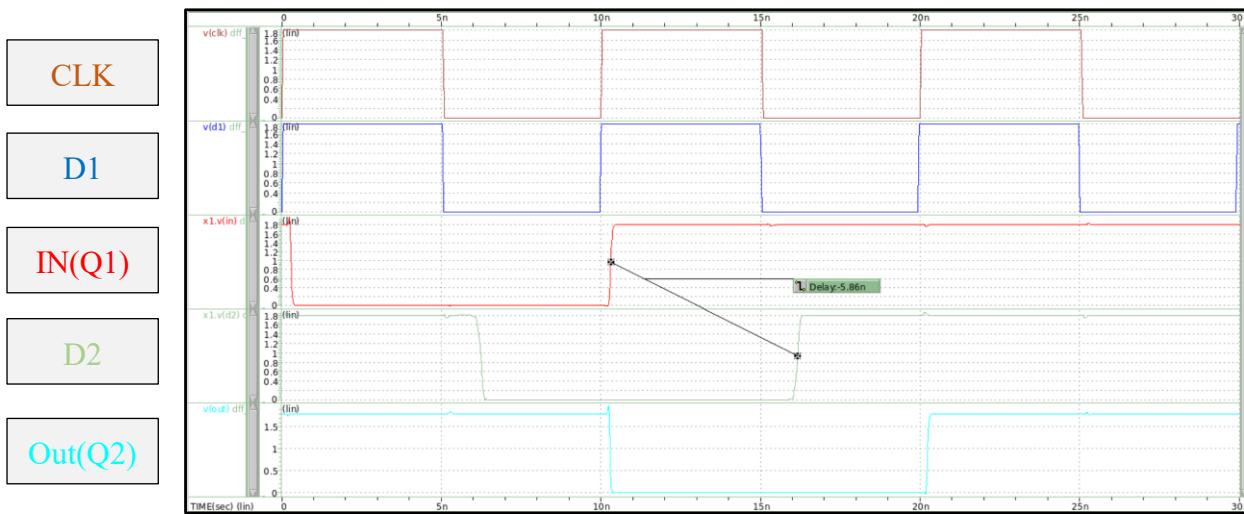


Figure 50 DFF + 4 inverter chain waveform

從結果可知在 4 顆 inverter 的 propagation delay 為 5.86，小於先前計算的 9.678ns，故輸出(OUT)正常。

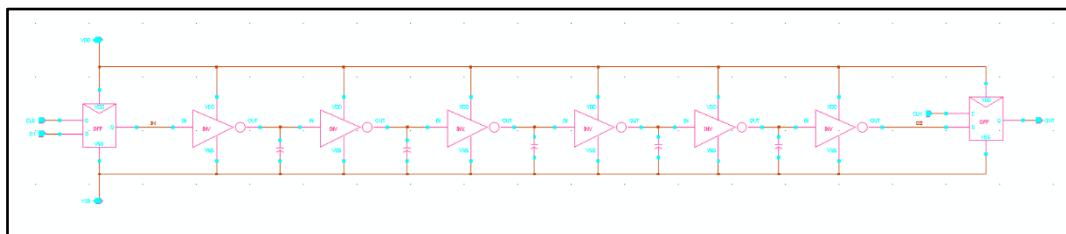


Figure 51 DFF + 6 inverter chain schematic

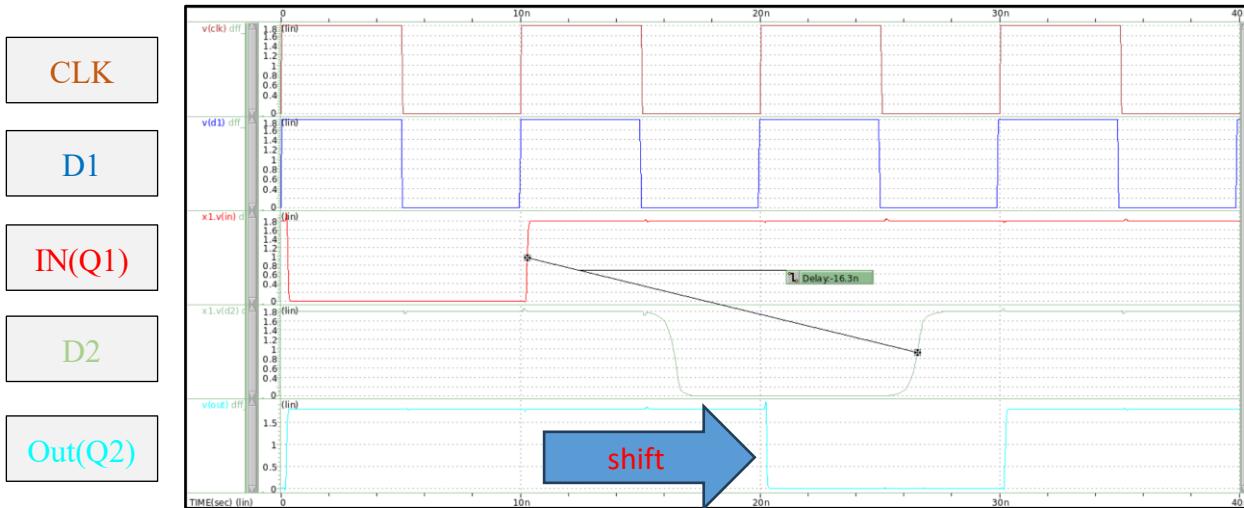


Figure 52 DFF + 6 inverter chain waveform

從結果可知在 6 顆 inverter 的 propagation delay 為 16.3ns，大於先前計算的 9.678ns，輸出(OUT)無法在下一個 posedge CLK 時轉態為一，電路出錯。

Input = GND:

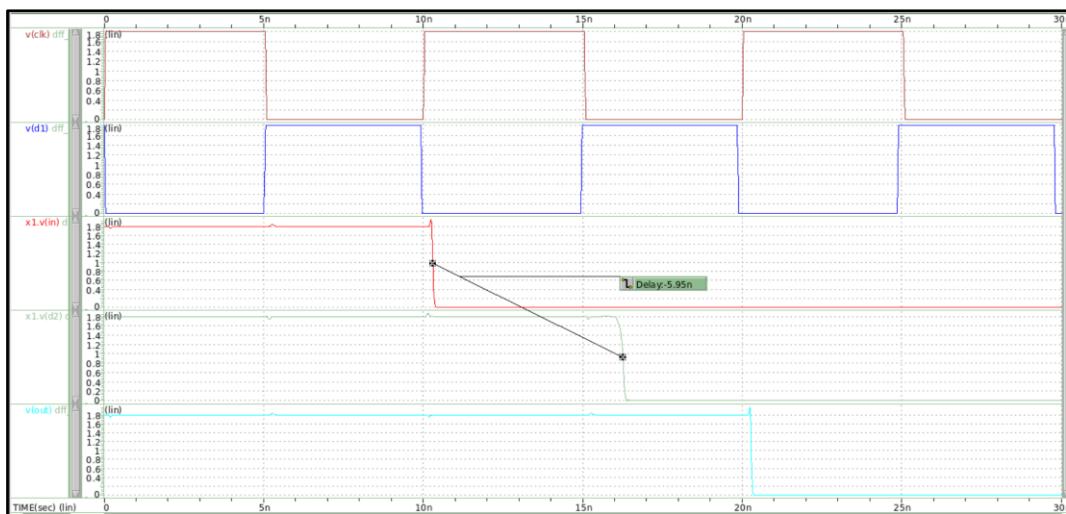
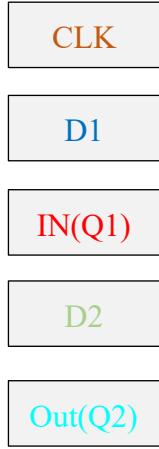


Figure 53 DFF + 4 inverter chain waveform

從結果可知在 4 顆 inverter 的 propagation delay 為 5.95ns，小於先前計算的 9.678ns，故輸出(OUT)正常。

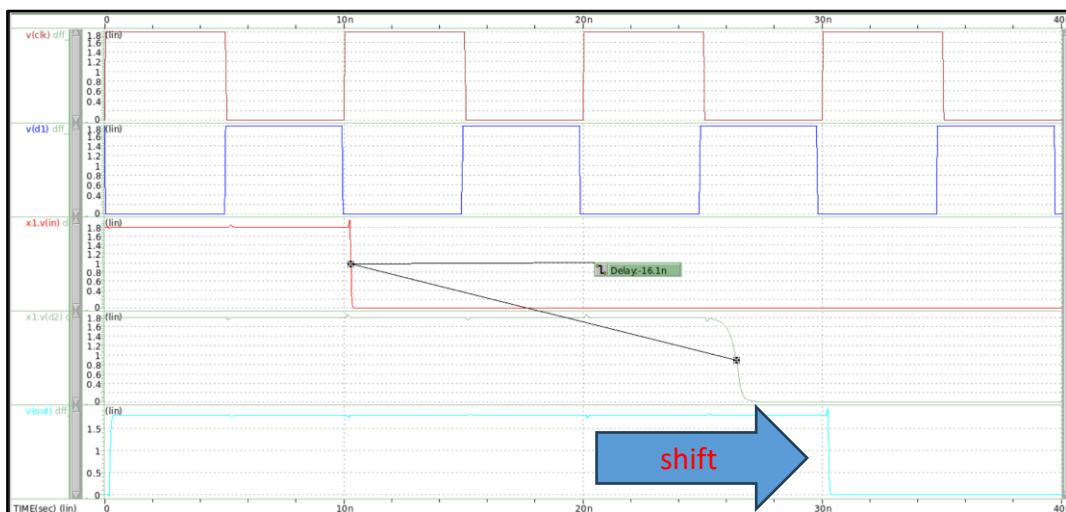
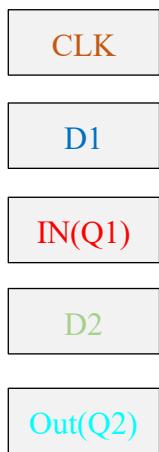


Figure 54 DFF + 6 inverter chain waveform

從結果可知在 6 顆 inverter 的 propagation delay 為 16.1ns，小於先前計算的 9.678ns，輸出(OUT)無法在下一個 posedge CLK 時轉態為一，電路出錯。

Minimum contamination delay

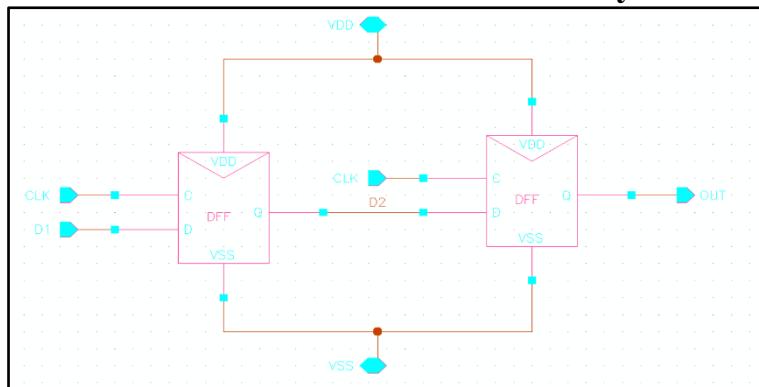


Figure 55 DFF with no combination logic

Input = VDD:

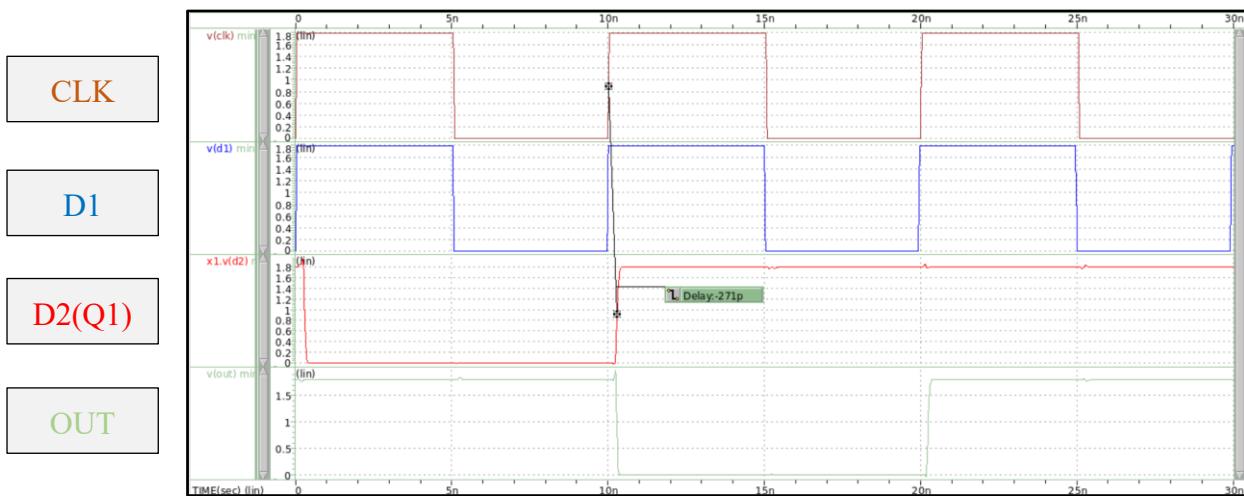


Figure 56 VDD input

Input = GND:

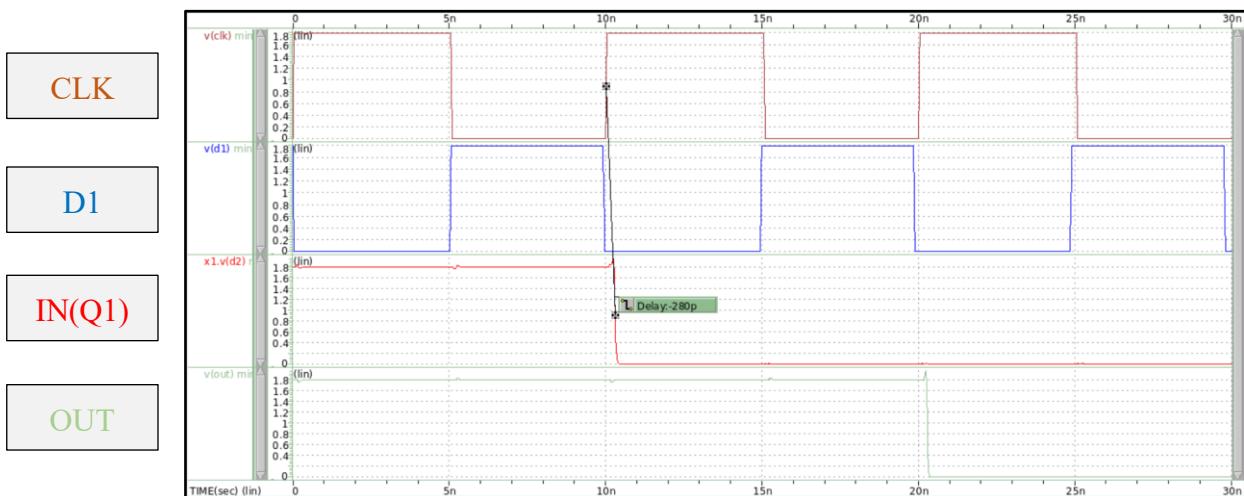


Figure 57 GND input

從結果可知無論 input 為 VDD 還是 GND 電路皆正常，因兩者的 hold time 接足夠，故電路可以正常運行。

- (b) Using the DFF in Fig.3 and with the inverter size (W/L) $n = 0.6\mu m/0.2\mu m$ and (W/L) $p = 1.8\mu m/0.2\mu m$, the transmission gate size (W/L) $n = (W/L) p = 0.8\mu m/0.2\mu m$. (15%)

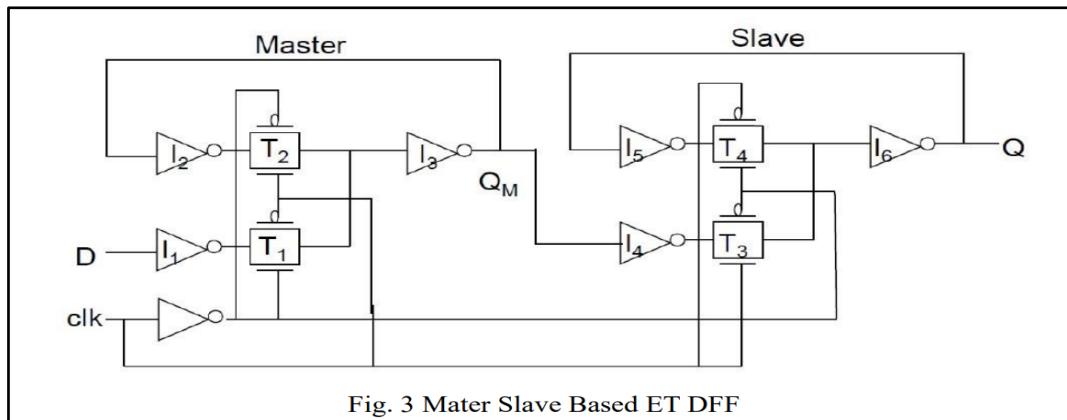


Figure 58

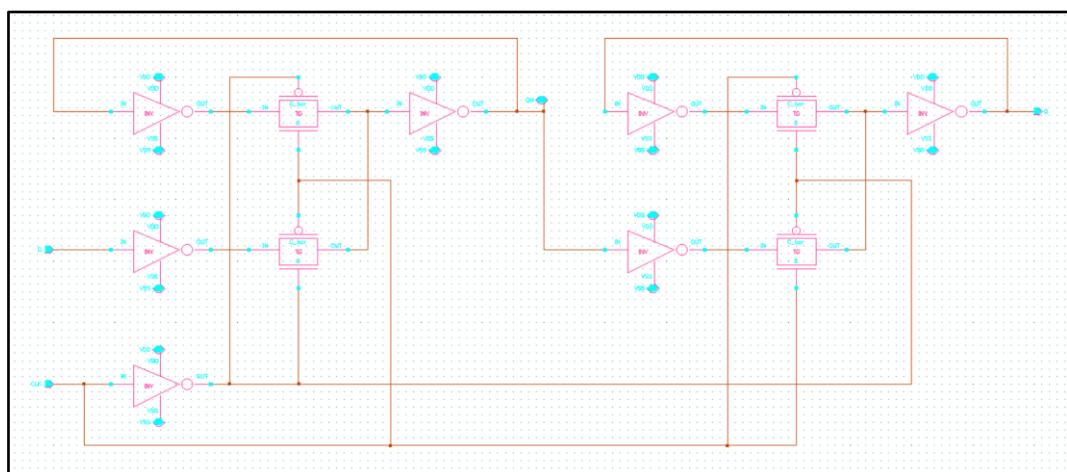
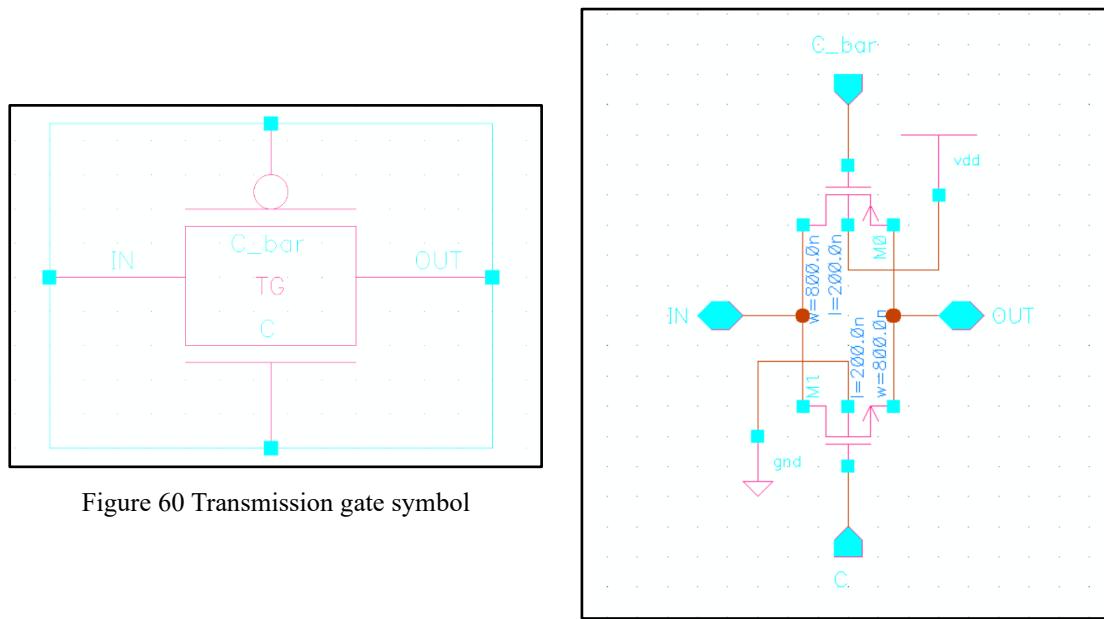


Figure 59 Master Slave Based ET DFF



Setup time:

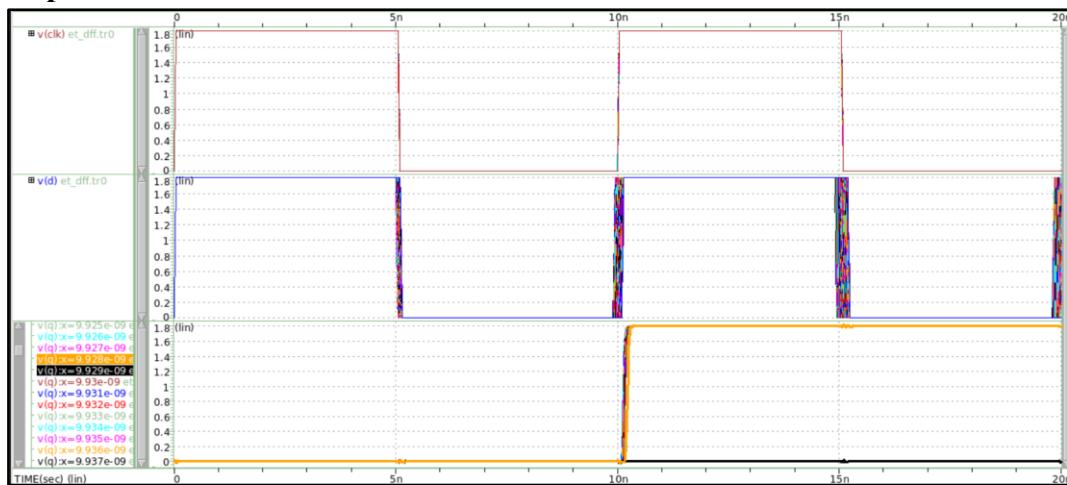


Figure 62 Find the rising setup time

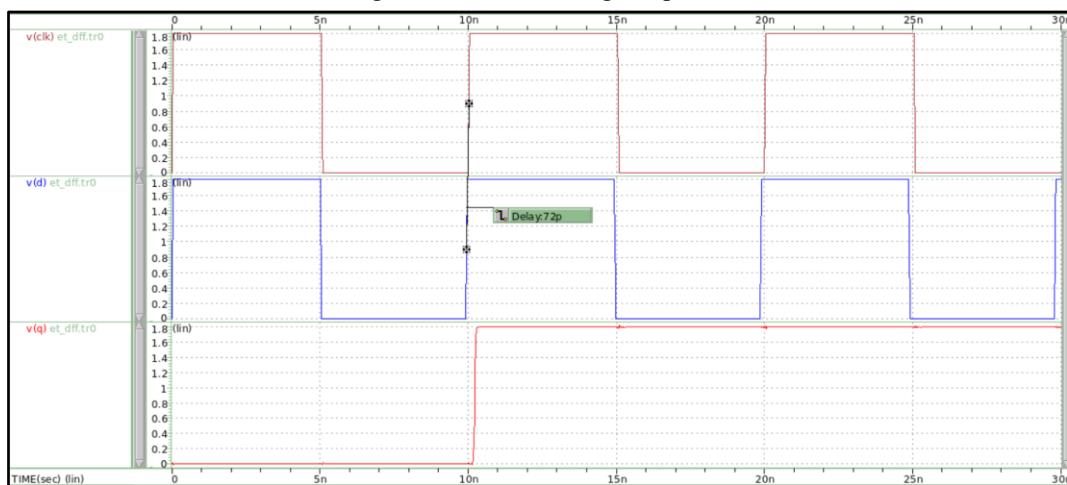


Figure 63 Rising setup time at period 9.928ns

Rising setup time = 72ps

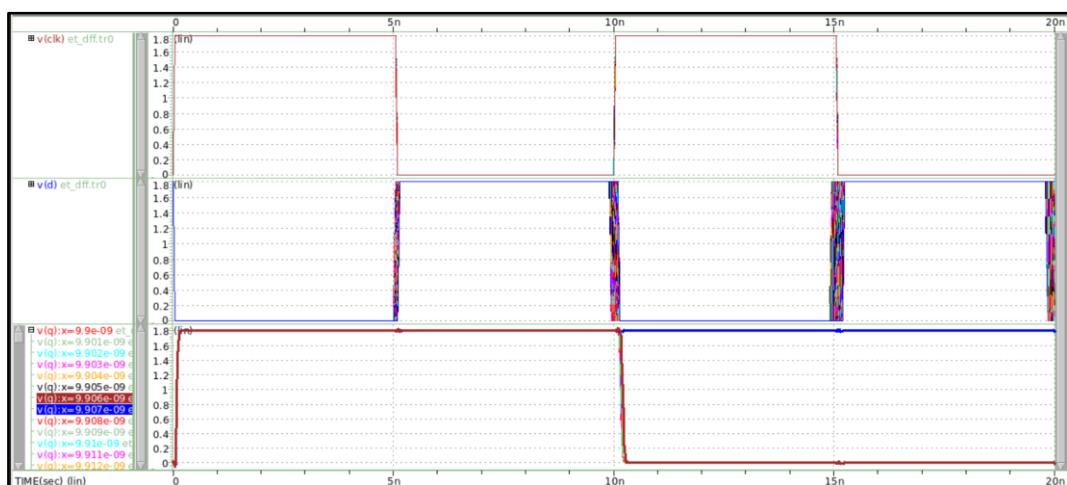


Figure 64 Find the falling setup time

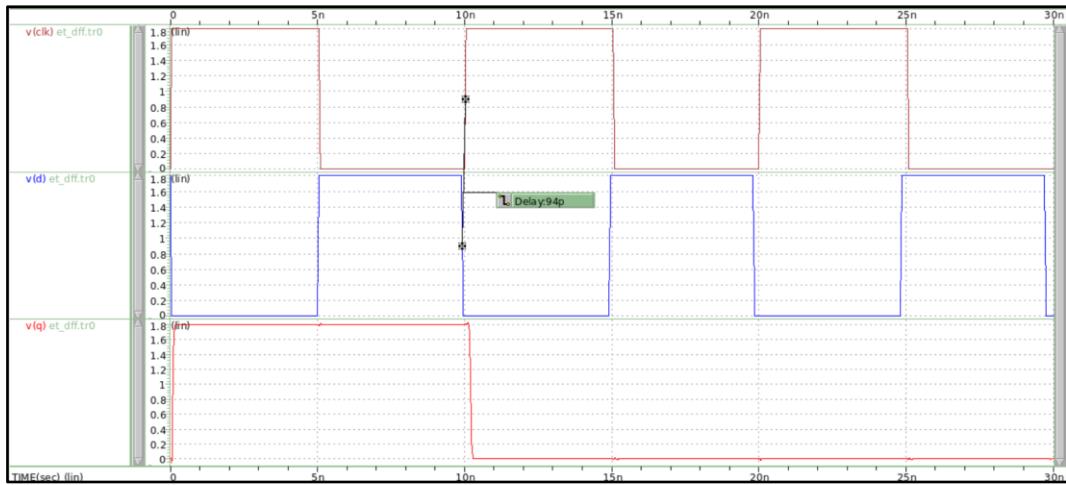


Figure 65 Falling setup time at period 9.906ns

Falling setup time = 94ps

Hold time:



Figure 66 Find the rising hold time

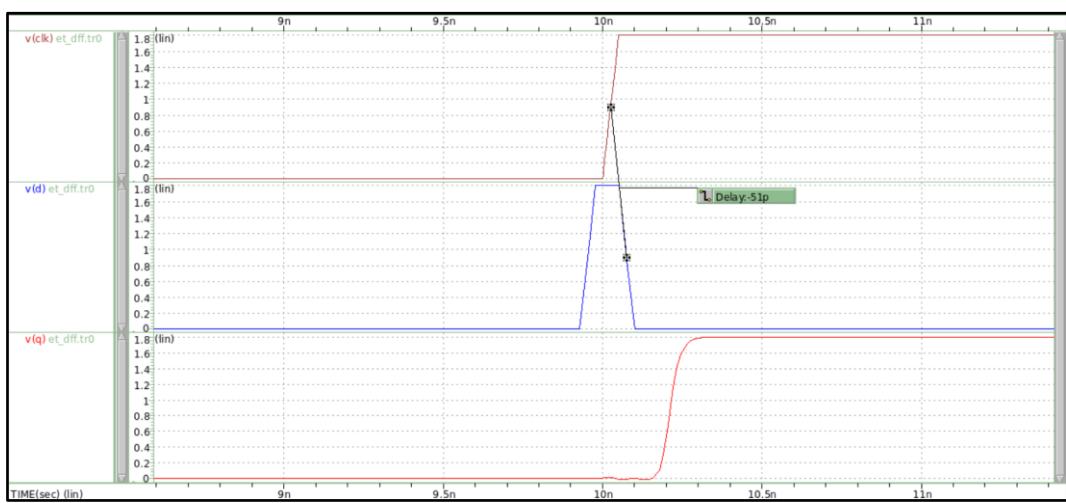


Figure 67 Rising setup time at period width 0.073ns

Rising hold time = 51ps

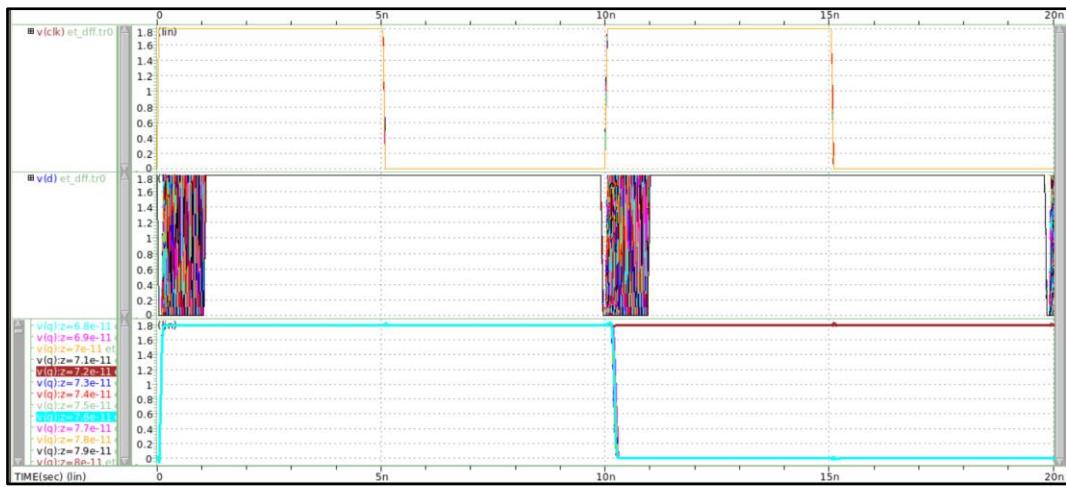


Figure 68 Find the falling hold time

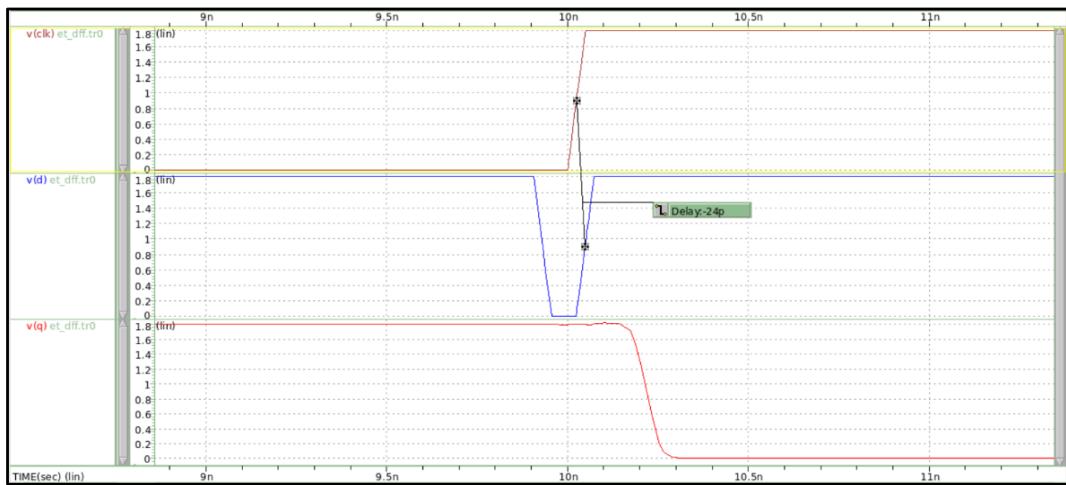


Figure 69 Falling setup time at period width 0.073ns

Falling hold time = 24ps

Tcq:

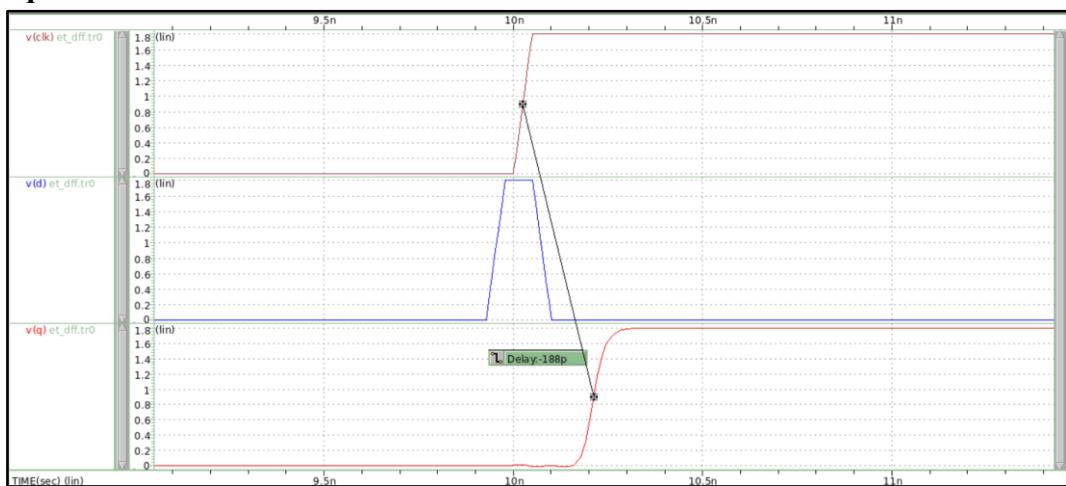


Figure 70 Rising Tcq

Tcq = 188ps

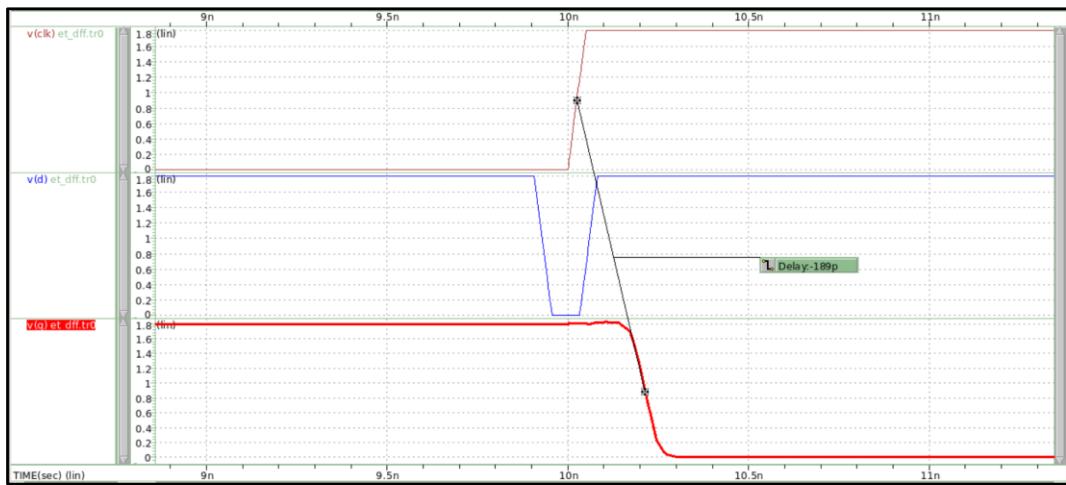


Figure 71 Falling Tcq

$$T_{pcq} = 189\text{ps}$$

	Rising input	Falling input
T_{setup}	72ps	94ps
T_{hold}	51ps	24ps
T_{cq}	188ps (T_{pcq})	189ps (T_{ccq})
Max T_{pd}	9.739ns	
Min T_{cd}	-164ns	

Table 8 Calculate Max T_{pd} & T_{cd}

Maximum propagation delay

Input= VDD:

與第一題相同，使用了 4 顆 inverter 和 6 顆 inverter 比較 2 種不同的 combinational circuit 的 propagation delay。

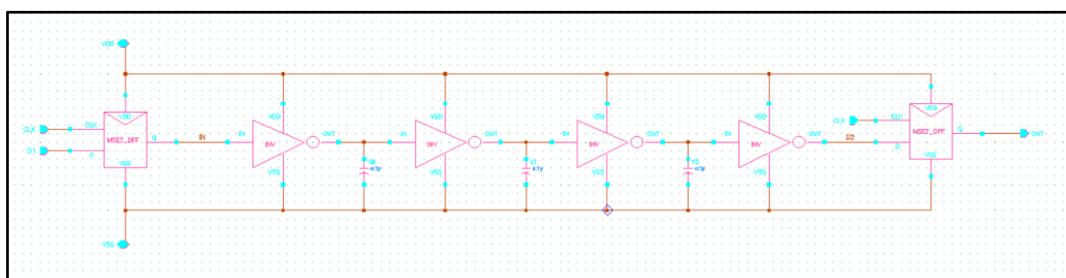


Figure 72 Master Slave Based ET DFF + 4 inverter schematic

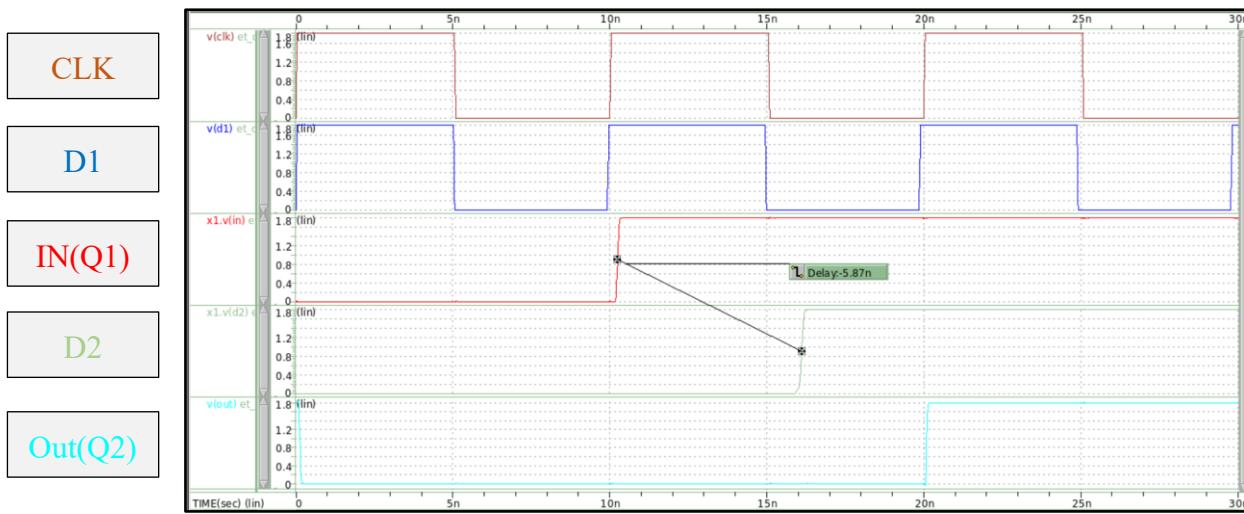


Figure 73 Master Slave Based ET DFF + 4 inverter waveform

從結果可知在 4 顆 inverter 的 propagation delay 為 5.87，小於先前計算的 9.739ns，故輸出(OUT)正常。

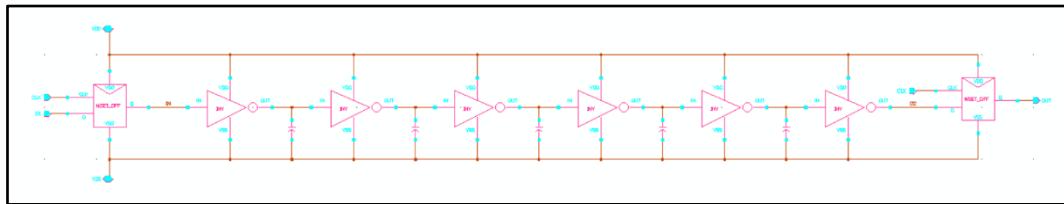


Figure 74 Master Slave Based ET DFF + 6 inverter schematic



Figure 75 Master Slave Based ET DFF + 6 inverter waveform

從結果可知在 6 顆 inverter 的 propagation delay 為 16.4ns，大於先前計算的 9.739ns，輸出(OUT)無法在下一個 posedge CLK 時轉態為一，電路出錯。

Input = GND:

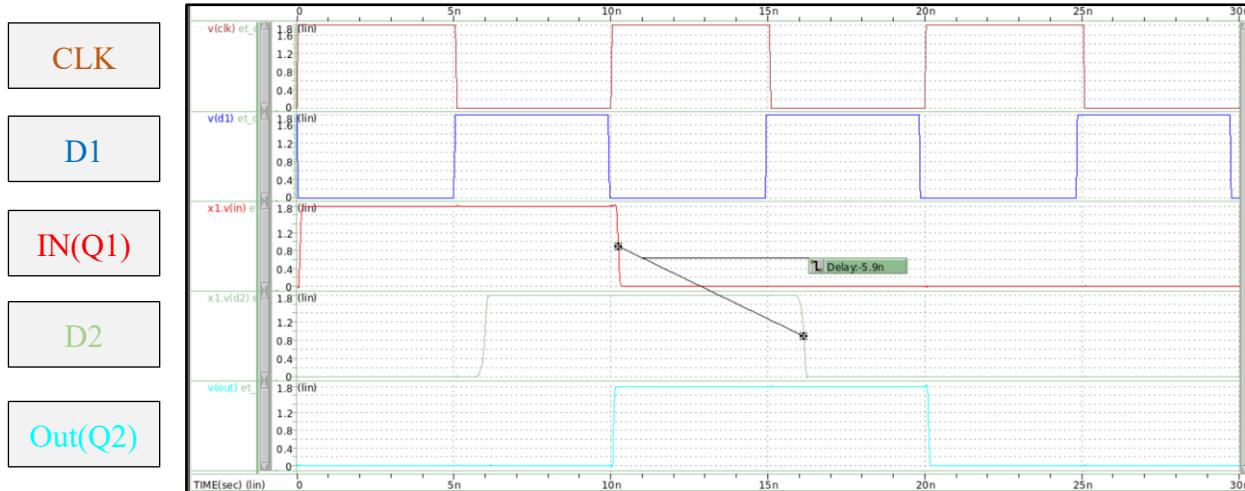


Figure 76 Master Slave Based ET DFF + 4 inverter waveform

從結果可知在 4 顆 inverter 的 propagation delay 為 5.9ns，小於先前計算的 9.739ns，故輸出(OUT)正常。



Figure 77 Master Slave Based ET DFF + 6 inverter waveform

從結果可知在 6 顆 inverter 的 propagation delay 為 15.9ns，大於先前計算的 9.739ns，輸出(OUT)無法在下一個 posedge CLK 時轉態為一，電路出錯。

Minimum contamination delay

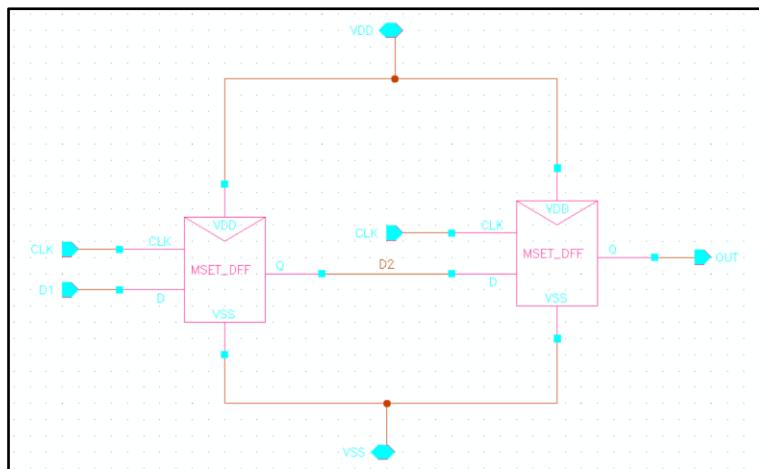


Figure 78 Master Slave Based ET DFF with no combination logic

Input= VDD:



Figure 79 VDD input

Input = GND:

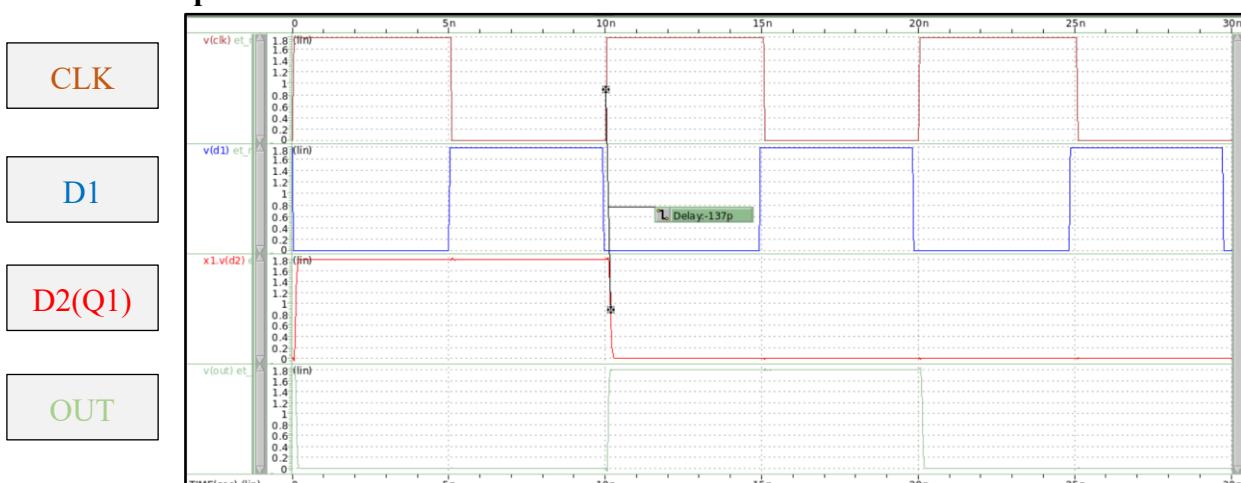


Figure 80 GND input

從結果可知無論 input 為 VDD 還是 GND 電路皆正常，因兩者的 hold time 接足夠，故電路可以正常運行。

- (c) Use the previous results in question1 (setup time and hold time) to hand calculate the maximum and minimum delay failure condition in (a). As for (b), do the same hand calculation as (a). (10%)

$$T_{pd} \leq T_c - (T_{setup} + T_{pcq})$$

$$T_{cd} \geq T_{hold} - T_{ccq}$$

	Rising input	Falling input
T _{setup}	34ps	75ps
T _{hold}	106ps	32ps
T _{cq}	288ps (T _{pcq})	278ps (T _{ccq})
Max T _{pd}	9.678ns	
Min T _{cd}	-246ns	

Table 9 condition in (a)

	Rising input	Falling input
T _{setup}	72ps	94ps
T _{hold}	51ps	24ps
T _{cq}	188ps (T _{pcq})	189ps (T _{ccq})
Max T _{pd}	9.739ns	
Min T _{cd}	-164ns	

Table 10 condition in (b)

(d) Please compare and comment the results of (a) and (b) with (c). (10%)

(a) 小題為 NAND gate 組成的 DFF，(b)為 inverter 和 transmission gate 組成的 DFF，透過使用兩個 level trigger 的 latch 電路加上相反的 CLK 可以製造一個 edge trigger 的 DFF。

兩者在 setup time 的差異，可以發現使用 transmission gate 的 DFF 會有較長的 setup time，原因是因為訊號 D 會經過 3 個 inverter 和 1 個 transmission gate，而 NAND gate 電路只需要經過 2 個 NAND，因 logic gate 的數量不同，故 delay 也不同，較多 logic 的電路也需要較多的 setup time。

與 setup time 相反，hold time 中 transmission gate 的 DFF 時間較短，原因同上，因為 logic 的數量較多，故 T_{pd} 也較大，使的 transmission gate 的 DFF 的輸入 hold time 下降。

(c) 小題由計算 delay 的兩個公式如下可知：

$$T_{pd} \leq T_c - (T_{setup} + T_{pcq})$$

$$T_{cd} \geq T_{hold} - T_{ccq}$$

因為 transmission gate 的 DFF 有較大的 setup time 和較小的 hold time，故計算後的 maximum propagation delay 也較大。