超大型積體電路設計

VLSI Design

Homework V

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Contents

1. Please design a 5-bit binary synchronous up counter with clock frequency CLK = 400MHz, VDD = 1.8V (default) , VSS = 0V. You can use any architecture to complete the design. Try to minimize the power consumption of the counter. You can adjust the value of VDD for minimizing the power meanwhile the counter works correctly, and the maximum glitch should be less than 80ps.

(a) Please describe how you design the counter and how to reduce the glitch and power consumption of counter. (40%)

(b) Please list the glitch in each number (0 ~ 31) and find the maximum glitch. (20%)

(c) Please measure the power of the counter. (5%)

本題沿用 hw4 的 DFF 與 unit inverter 規格。

Size	Inverter	2-inputs NAND
PMOS	1.8u/0.18u, m = 1	1.04u/0.18u, m = 1
NMOS	0.6u/0.18u, m = 1	1.2u/0.18u, m = 1

Table 1 Siz

Schematic

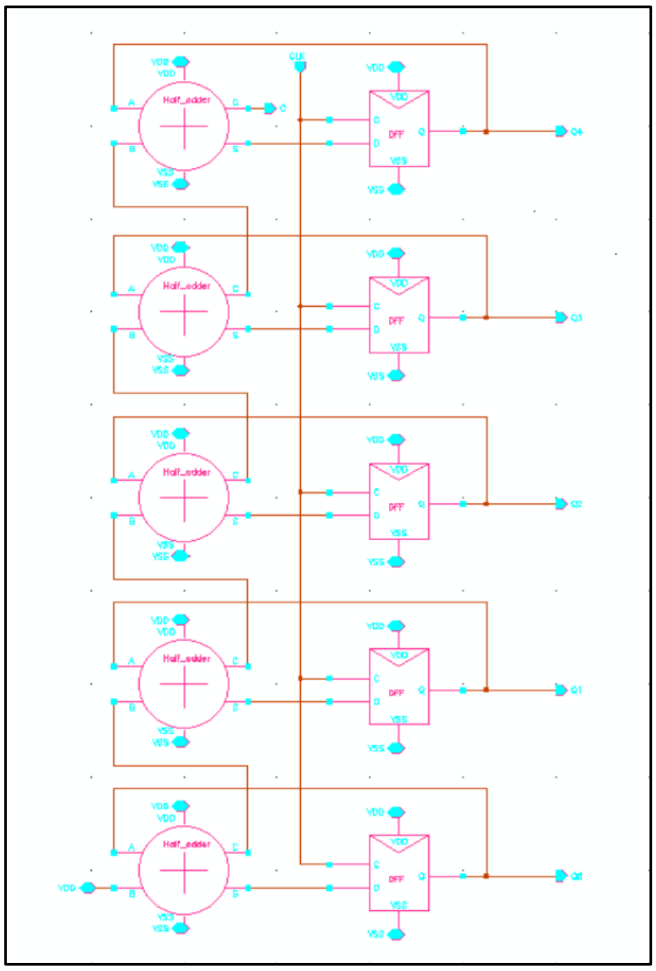

Figure 1 5-bit binary synchronous up counter schematic

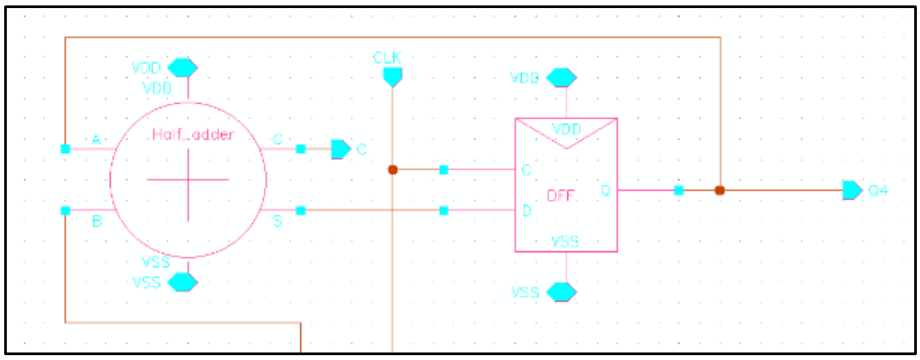

Figure 2 Each bit binary synchronous up counter schematic

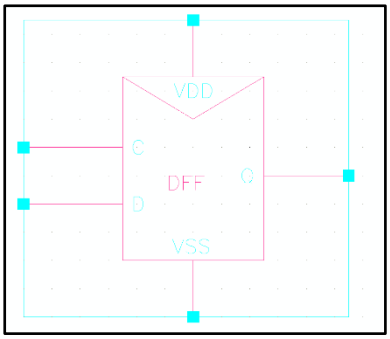

Figure 3 DFF symbol

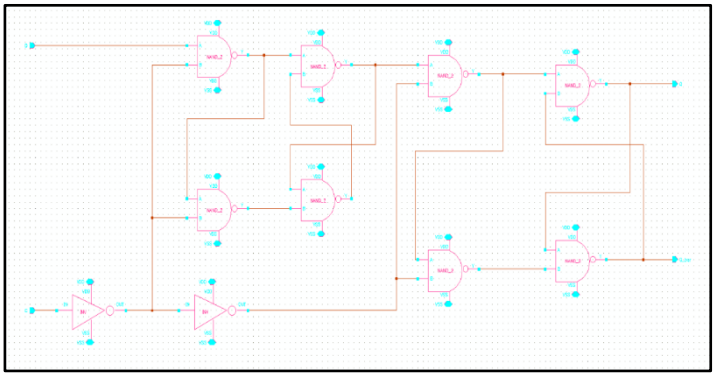

Figure 4 DFF schematic

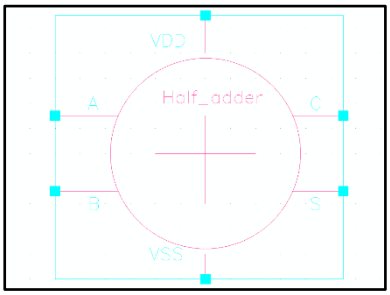

Figure 5 Half_adder symbol

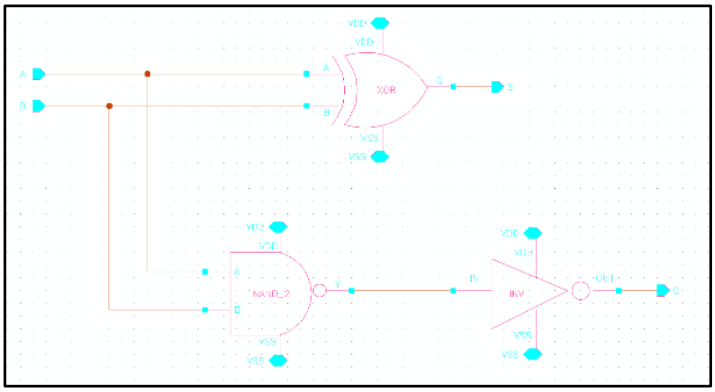

Figure 6 Half_adder schematic

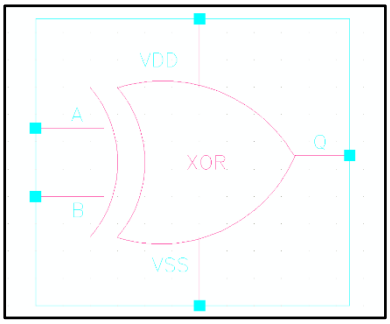

Figure 7 XOR symbol

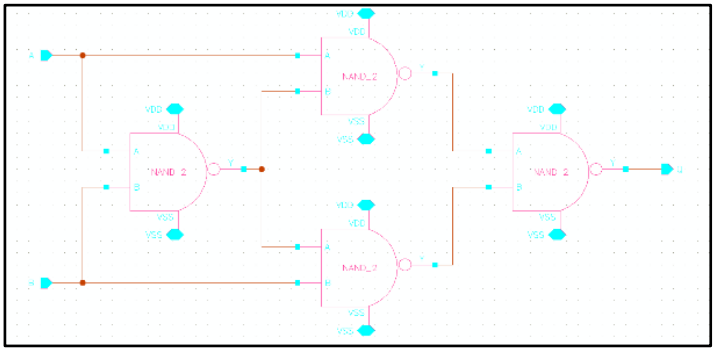

Figure 8 XOR schematic

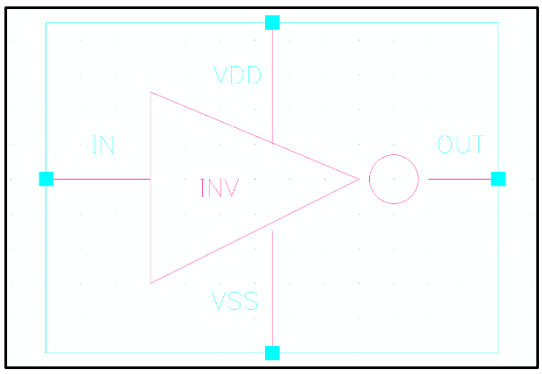

Figure 9 Unit inverter symbol

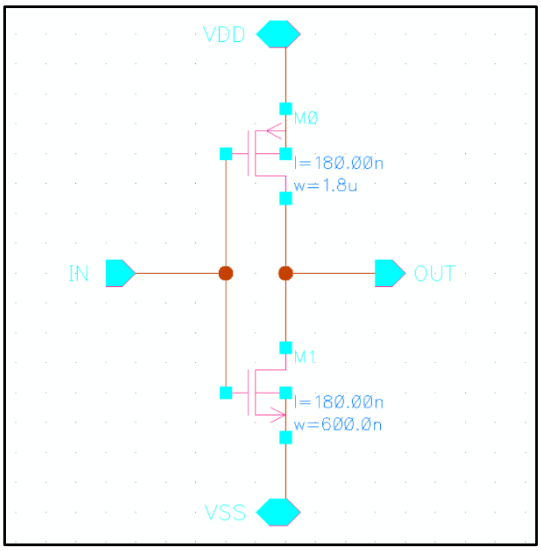

Figure 10 Unit inverter schematic

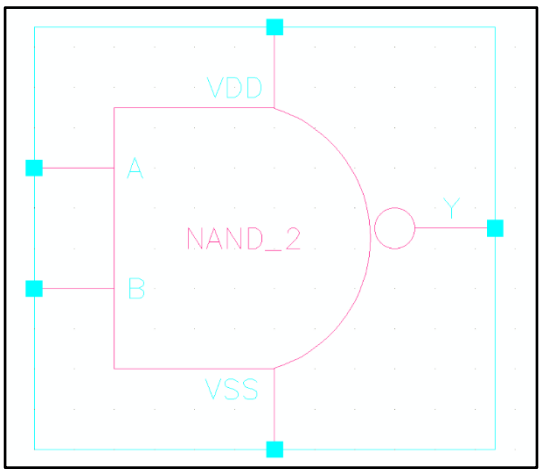

Figure 11 2-inputs NAND gate symbol

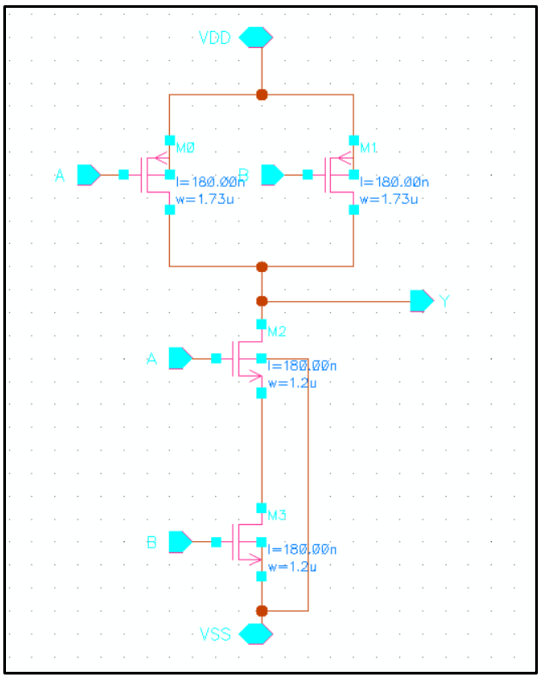

Figure 12 2-inputs NAND gate schematic

設計想法:

與講義上的 synchronous counter 相同，由 half adder 和 flip flop 組成，half adder 會產生 sum 和 carry，分別存進 flip flop 和下一級 half adder 輸入，來實現 counter 功能。其中大部分的底層的邏輯閘選擇使用 NAND 和 inverter 組合，原因是 NAND 相較於 NOR 可以使用較小的 MOS 尺寸，進而達到題目要求的降低功耗要求。

Glitch 原理:

Glitch 發生的原因是因為在計數時，同時有兩個 bit 的改變，因電壓在轉態過程所造成多餘且錯誤的值，例如在 1 轉換為 2 的過程，5bits 的 counter 會從 00001 變 00010，故中間會有一小段時間為第 4 個 bit 上升，第 5 個 bit 下降，因實際上 0 和 1 的變化是由電壓升降來實現，所以輸出會有一個瞬間會變為 00011，下方以 15~16 為例:

Figure 13

在 15~16 是由 01111→10000，轉態中會有 4 個 glitch 值，故分別為 31、30、28、24，在波型上可知當 glitch value = 24 時有最長的 glitch time，故在後面的表格我將最長的 glitch time 標示成紅色，表示完整的 glitch time。

造成這個現象的原因我認為和 data 的 rising 和 falling 有關，在 HW4 時討論了在 DFF 中 rising 和 falling 的差別，rsising 時間都比 falling 來的短，所以 glitch value 會先被拉大(所有 bit 都是 on 的狀態)。接著推測因 counter 的電路設計故 falling 會從低的 bit 依序 off。

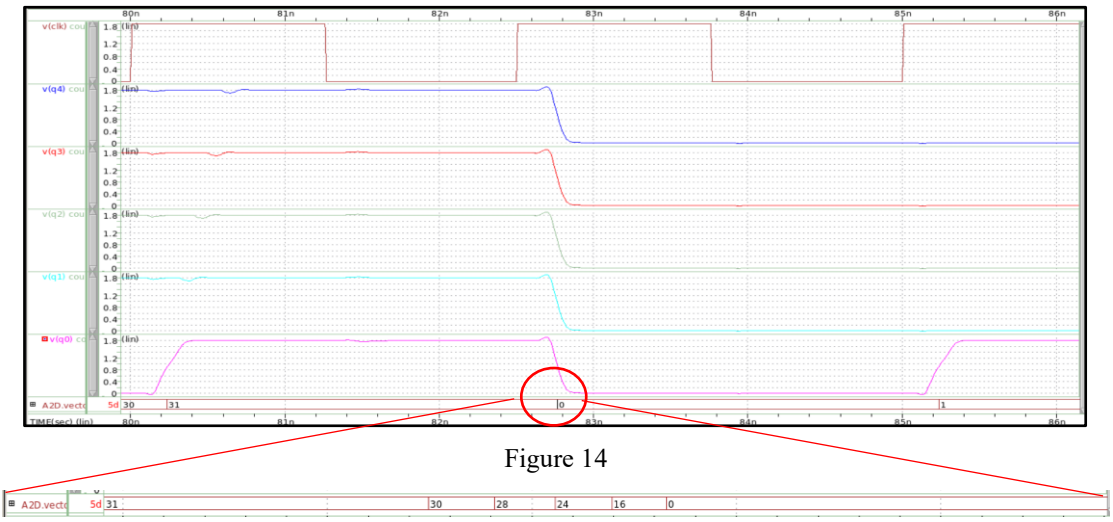

Figure 14

Figure16 為 31~0(11111→00000)的波型，推測因為都是 falling 的轉態，故相較前面的 glitch time 減少許多。

Result

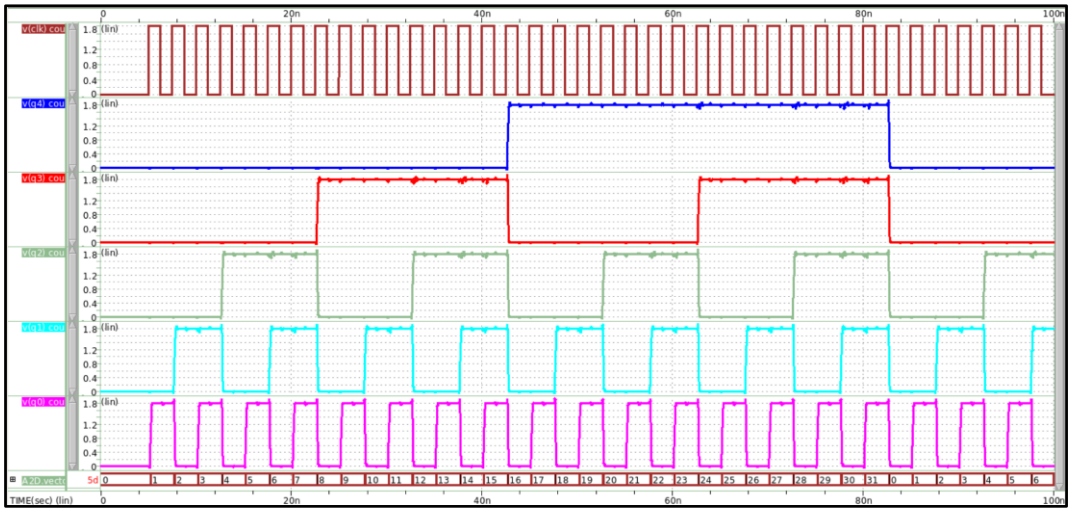

Figure 15 5-bit binary synchronous up counter waveform

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
glitch_1_2_->3=  28.0288p  targ=   7.7668n   trig=   7.7388n
glitch_3_4_->7=  28.0354p  targ=  12.7668n   trig=  12.7388n
glitch_3_4_->6=  28.1919p  targ=  12.7670n   trig=  12.7388n
glitch_5_6_->7=  28.0256p  targ=  17.7667n   trig=  17.7386n
glitch7_8_->15=  28.0270p  targ=  22.7659n   trig=  22.7379n
glitch7_8_->14=  28.1935p  targ=  22.7661n   trig=  22.7379n
glitch7_8_->12=  28.3389p  targ=  22.7662n   trig=  22.7379n
glitch9_10_->11=  27.9716p  targ=  27.7658n   trig=  27.7379n
glitch11_12_->15=  28.0180p  targ=  32.7666n   trig=  32.7386n
glitch11_12_->14=  28.1809p  targ=  32.7668n   trig=  32.7386n
glitch13_14_->15=  27.9693p  targ=  37.7667n   trig=  37.7387n
glitch15_16_->31=  27.9874p  targ=  42.7659n   trig=  42.7379n
glitch15_16_->30=  28.1519p  targ=  42.7660n   trig=  42.7379n
glitch15_16_->28=  28.3010p  targ=  42.7662n   trig=  42.7379n
glitch15_16_->24=  28.4369p  targ=  42.7663n   trig=  42.7379n
glitch17_18_->19=  27.9971p  targ=  47.7659n   trig=  47.7379n
glitch19_20_->23=  27.9983p  targ=  52.7659n   trig=  52.7379n
glitch19_20_->22=  28.1588p  targ=  52.7660n   trig=  52.7379n
glitch21_22_->23=  28.0264p  targ=  57.7659n   trig=  57.7379n
glitch23_24_->31=  27.9915p  targ=  62.7659n   trig=  62.7379n
glitch23_24_->30=  28.1544p  targ=  62.7660n   trig=  62.7379n
glitch23_24_->28=  28.2959p  targ=  62.7662n   trig=  62.7379n
glitch25_26_->27=  27.9933p  targ=  67.7658n   trig=  67.7378n
glitch27_28_->31=  28.0343p  targ=  72.7660n   trig=  72.7379n
glitch27_28_->30=  28.1938p  targ=  72.7661n   trig=  72.7379n
glitch29_30_->31=  28.0467p  targ=  77.7667n   trig=  77.7387n
glitch31_0_->30= 162.5383f  targ=  82.7669n   trig=  82.7667n
glitch31_0_->28= 147.0692f  targ=  82.7671n   trig=  82.7669n
glitch31_0_->24= 139.3144f  targ=  82.7672n   trig=  82.7671n
glitch31_0_->16= 133.4034f  targ=  82.7673n   trig=  82.7672n
pvdd=-744.5465u  from=   5.0000n     to=  85.0000n
```

Figure 16 Glitch & power consumption

Power consumption = 744.5465μW

上圖為每一個 glitch 的時間長度與 glitch 的值，由波形可以看出 glitch 僅發生在奇數變偶數的時刻，故只標出有 glitch 的時間，下方用表格表示

Number to number	Glitch value	Glitch time	
1~2	3	28.2088ps	
3~4	7	28.0354ps	
	6	28.1919ps	
5~6	7	28.0256ps	
7~8	15	28.0270ps	
	14	28.1935ps	
	12	28.3389ps	
9~10	11	27.9716ps	
11~12	15	28.0180ps	
	14	28.1809ps	
13~14	15	27.9693ps	
15~16	31	27.9874ps	
	30	28.1519ps	
	28	28.3010ps	
	24	28.4369ps	
17~18	19	27.9971ps	
19~20	23	27.9983ps	
	22	28.1588ps	
21~22	23	28.0264ps	
23~24	31	27.9915ps	
	30	28.1544ps	
	28	28.2959ps	
25~26	27	27.9933ps	
27~28	31	28.0343ps	
	30	28.1938ps	
29~30	31	28.0467ps	
31~0	30	162.5383fs	582.3253fs
	28	147.0692fs	
	24	139.3144fs	
	16	133.4034fs	

Table 2 Glitch(紅字代表該數字轉換的總 glitch time)

Maximum glitch = 28.4369ps

Glitch and power consumption reduce method:

I. Reduce the VDD to 1.1V

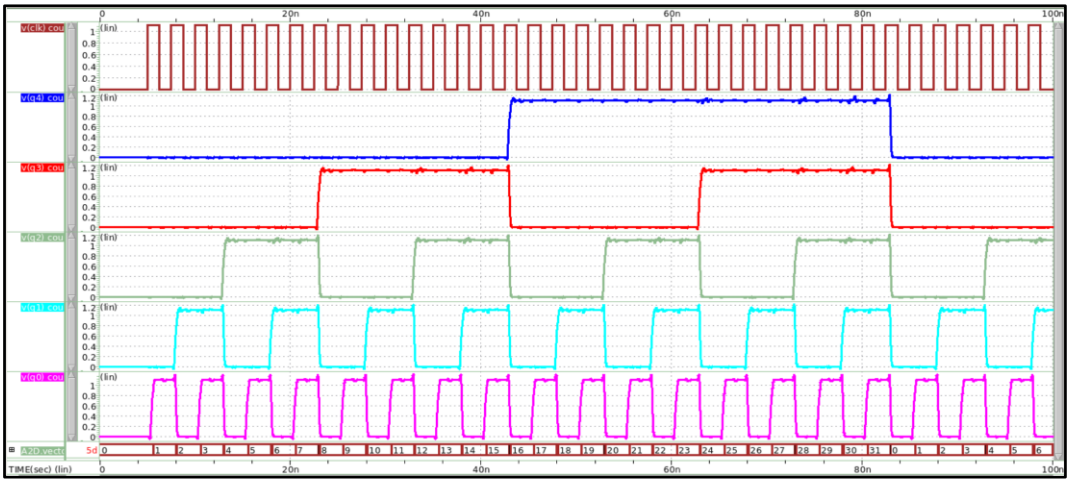

Figure 17 5-bit binary synchronous up counter waveform

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
glitch_1_2_->3=  78.2977p  targ=   8.0300n   trig=   7.9517n
glitch_3_4_->7=  78.4741p  targ=  13.0305n   trig=  12.9520n
glitch_3_4_->6=  79.1479p  targ=  13.0312n   trig=  12.9520n
glitch_5_6_->7=  78.4326p  targ=  18.0300n   trig=  17.9516n
glitch7_8_->15=  78.3765p  targ=  23.0304n   trig=  22.9520n
glitch7_8_->14=  79.0134p  targ=  23.0310n   trig=  22.9520n
glitch7_8_->12=  79.5790p  targ=  23.0316n   trig=  22.9520n
glitch9_10_->11=  78.1942p  targ=  28.0295n   trig=  27.9513n
glitch11_12_->15=  78.2415p  targ=  33.0303n   trig=  32.9521n
glitch11_12_->14=  78.9021p  targ=  33.0310n   trig=  32.9521n
glitch13_14_->15=  78.1507p  targ=  38.0294n   trig=  37.9513n
glitch15_16_->31=  78.5946p  targ=  43.0297n   trig=  42.9511n
glitch15_16_->30=  79.2462p  targ=  43.0304n   trig=  42.9511n
glitch15_16_->28=  79.8312p  targ=  43.0310n   trig=  42.9511n
glitch15_16_->24=  80.4022p  targ=  43.0315n   trig=  42.9511n
glitch17_18_->19=  78.1306p  targ=  48.0294n   trig=  47.9513n
glitch19_20_->23=  78.4186p  targ=  53.0305n   trig=  52.9520n
glitch19_20_->22=  79.0821p  targ=  53.0311n   trig=  52.9520n
glitch21_22_->23=  78.5621p  targ=  58.0304n   trig=  57.9519n
glitch23_24_->31=  78.2579p  targ=  63.0303n   trig=  62.9520n
glitch23_24_->30=  78.9578p  targ=  63.0310n   trig=  62.9520n
glitch23_24_->28=  79.5821p  targ=  63.0316n   trig=  62.9520n
glitch25_26_->27=  78.2572p  targ=  68.0296n   trig=  67.9513n
glitch27_28_->31=  78.5259p  targ=  73.0306n   trig=  72.9521n
glitch27_28_->30=  79.1723p  targ=  73.0313n   trig=  72.9521n
glitch29_30_->31=  78.4259p  targ=  78.0303n   trig=  77.9519n
glitch31_0_->30= 703.3738f  targ=  83.0310n   trig=  83.0303n
glitch31_0_->28= 634.0452f  targ=  83.0316n   trig=  83.0310n
glitch31_0_->24= 630.6190f  targ=  83.0323n   trig=  83.0316n
glitch31_0_->16= 749.5133f  targ=  83.0330n   trig=  83.0323n
pvdd=-259.4326u  from=   5.0000n     to=  85.0000n
```

Figure 18 Glitch & power consumption

Power consumption = 259.4326μW

選擇 VDD = 1.1V 的原因是因為可以維持電路正常運作，若 VDD=1V 電路將會出錯。

Number to number	Glitch value	Glitch time	
1~2	3	78.2977ps	
3~4	7	78.4741ps	
	6	79.1479ps	
5~6	7	78.4326ps	
7~8	15	78.3765ps	
	14	79.0134ps	
	12	79.5790ps	
9~10	11	78.1942ps	
11~12	15	78.2415ps	
	14	78.9021ps	
13~14	15	78.1507ps	
15~16	31	78.5946ps	
	30	79.2462ps	
	28	79.8312ps	
	24	80.4022ps	
17~18	19	78.1306ps	
19~20	23	78.4186ps	
	22	79.0821ps	
21~22	23	78.5621ps	
23~24	31	78.2579ps	
	30	78.9578ps	
	28	79.5821ps	
25~26	27	78.2572ps	
27~28	31	78.5259ps	
	30	79.1723ps	
29~30	31	78.4259ps	
31~0	30	703.3738fs	2.718ps
	28	634.0452fs	
	24	630.6190fs	
	16	749.5133fs	

Table 3 Glitch(紅字代表該數字轉換的總 glitch time)

Maximum glitch = 80.4022ps

降低 VDD 後可以發現 power consumption 明顯下降(744μW→259μW)，但 glitch 卻也上升多(28ps→78ps)，故有可能因此造成電路不正常運作。

II. Reduce the unit inverter size

Size	Inverter	2-inputs NAND
PMOS	0.9u/0.18u, m = 1	0.52u/0.18u, m = 1
NMOS	0.3u/0.18u, m = 1	0.6u/0.18u, m = 1

Table 4 Resize

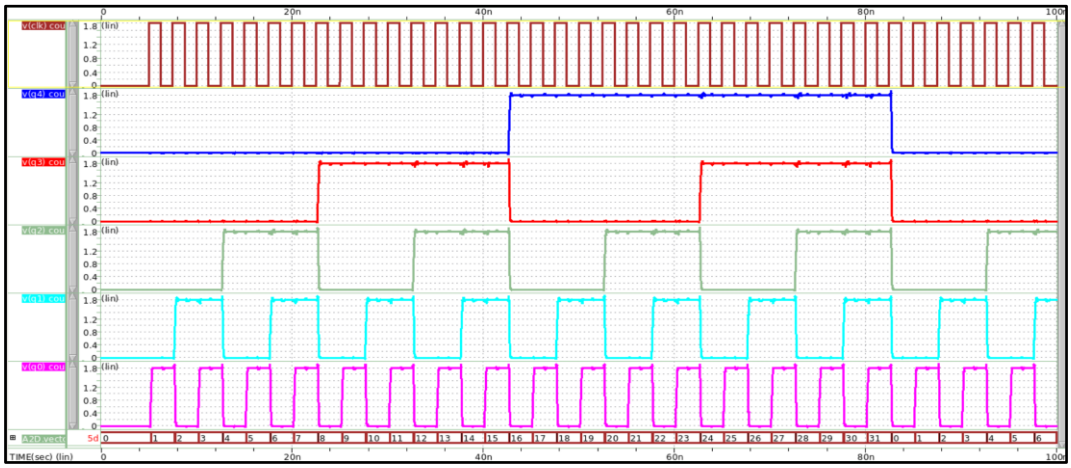

Figure 19 5-bit binary synchronous up counter waveform

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
glitch_1_2_->3=  28.1748p  targ=   7.7616n   trig=   7.7334n
glitch_3_4_->7=  28.1781p  targ=  12.7616n   trig=  12.7334n
glitch_3_4_->6=  28.3355p  targ=  12.7618n   trig=  12.7334n
glitch_5_6_->7=  28.2117p  targ=  17.7616n   trig=  17.7333n
glitch7_8_->15=  28.2012p  targ=  22.7617n   trig=  22.7335n
glitch7_8_->14=  28.3655p  targ=  22.7618n   trig=  22.7335n
glitch7_8_->12=  28.5083p  targ=  22.7620n   trig=  22.7335n
glitch9_10_->11=  28.2135p  targ=  27.7616n   trig=  27.7333n
glitch11_12_->15=  28.2120p  targ=  32.7616n   trig=  32.7334n
glitch11_12_->14=  28.3702p  targ=  32.7618n   trig=  32.7334n
glitch13_14_->15=  28.1764p  targ=  37.7616n   trig=  37.7334n
glitch15_16_->31=  28.1756p  targ=  42.7616n   trig=  42.7334n
glitch15_16_->30=  28.3370p  targ=  42.7618n   trig=  42.7334n
glitch15_16_->28=  28.4841p  targ=  42.7619n   trig=  42.7334n
glitch15_16_->24=  28.6180p  targ=  42.7621n   trig=  42.7334n
glitch17_18_->19=  28.1999p  targ=  47.7617n   trig=  47.7335n
glitch19_20_->23=  28.2100p  targ=  52.7626n   trig=  52.7344n
glitch19_20_->22=  28.3681p  targ=  52.7628n   trig=  52.7344n
glitch21_22_->23=  28.1499p  targ=  57.7625n   trig=  57.7343n
glitch23_24_->31=  28.1786p  targ=  62.7616n   trig=  62.7334n
glitch23_24_->30=  28.3408p  targ=  62.7618n   trig=  62.7334n
glitch23_24_->28=  28.4826p  targ=  62.7619n   trig=  62.7334n
glitch25_26_->27=  28.2120p  targ=  67.7626n   trig=  67.7344n
glitch27_28_->31=  28.1612p  targ=  72.7616n   trig=  72.7335n
glitch27_28_->30=  28.3210p  targ=  72.7618n   trig=  72.7335n
glitch29_30_->31=  28.1827p  targ=  77.7626n   trig=  77.7344n
glitch31_0_->30= 165.0519f  targ=  82.7618n   trig=  82.7617n
glitch31_0_->28= 148.1577f  targ=  82.7620n   trig=  82.7618n
glitch31_0_->24= 139.5179f  targ=  82.7621n   trig=  82.7620n
glitch31_0_->16= 132.9963f  targ=  82.7623n   trig=  82.7621n
pvdd=-387.3136u  from=   5.0000n     to=  85.0000n
```

Figure 20 Glitch & power consumption

Power consumption = 387.3136μW

Number to number	Glitch value	Glitch time	
1~2	3	28.1748ps	
3~4	7	28.1781ps	
	6	28.3355ps	
5~6	7	28.2117ps	
7~8	15	28.2012ps	
	14	28.3665ps	
	12	28.5083ps	
9~10	11	28.2135ps	
11~12	15	28.2120ps	
	14	28.3702ps	
13~14	15	28.1764ps	
15~16	31	28.1756ps	
	30	28.3370ps	
	28	28.4841ps	
	24	28.6180ps	
17~18	19	28.1999ps	
19~20	23	28.2100ps	
	22	28.3681ps	
21~22	23	28.1499ps	
23~24	31	28.1786ps	
	30	28.3408ps	
	28	28.4826ps	
25~26	27	28.2120ps	
27~28	31	28.1612ps	
	30	28.3210ps	
29~30	31	28.1827ps	
31~0	30	165.0510fs	585.7229fs
	28	148.1577fs	
	24	139.5179fs	
	16	132.9963fs	

Table 5 Glitch(紅字代表該數字轉換的總 glitch time)

Maximum glitch = 28.6180p

降低 unit inverter size 後可以發現 power consumption 也有下降，雖然沒有調低 VDD 來的顯著(744μW→387μW)，但在 glitch 卻和原本 size 時的時間差不多，沒有因此上升。

III. Reduce VDD & unit inverter size

在已知調低 unit inverter size 會降低 power 並且 glitch 不太放大的情況下，加上調低 VDD 可以大幅下降 power consumption，故結合兩者的優點，理論上，較小的 unit inverter size 可以在更低的 VDD 下正常運作電路如下。

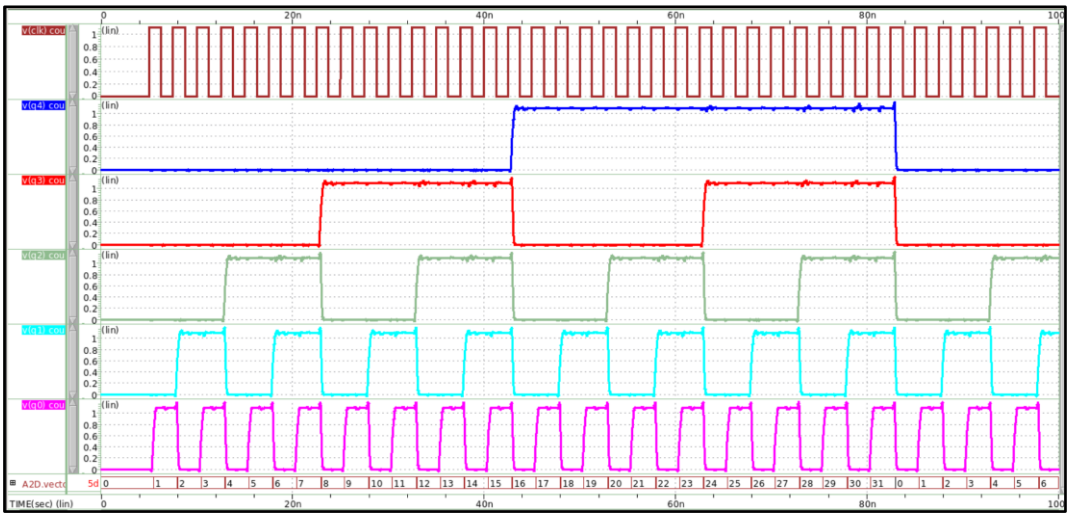

Figure 21 5-bit binary synchronous up counter waveform

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
glitch_1_2_->3=  75.1808p  targ=   8.0175n   trig=   7.9423n
glitch_3_4_->7=  75.4132p  targ=  13.0172n   trig=  12.9418n
glitch_3_4_->6=  76.0834p  targ=  13.0179n   trig=  12.9418n
glitch_5_6_->7=  75.1924p  targ=  18.0173n   trig=  17.9421n
glitch7_8_->15=  75.1010p  targ=  23.0173n   trig=  22.9422n
glitch7_8_->14=  75.8006p  targ=  23.0180n   trig=  22.9422n
glitch7_8_->12=  76.4258p  targ=  23.0186n   trig=  22.9422n
glitch9_10_->11=  75.1151p  targ=  28.0173n   trig=  27.9422n
glitch11_12_->15=  75.2598p  targ=  33.0174n   trig=  32.9421n
glitch11_12_->14=  75.9397p  targ=  33.0181n   trig=  32.9421n
glitch13_14_->15=  75.4027p  targ=  38.0175n   trig=  37.9421n
glitch15_16_->31=  75.4941p  targ=  43.0177n   trig=  42.9422n
glitch15_16_->30=  76.1558p  targ=  43.0184n   trig=  42.9422n
glitch15_16_->28=  76.7543p  targ=  43.0190n   trig=  42.9422n
glitch15_16_->24=  77.3213p  targ=  43.0195n   trig=  42.9422n
glitch17_18_->19=  75.3476p  targ=  48.0174n   trig=  47.9421n
glitch19_20_->23=  75.1106p  targ=  53.0174n   trig=  52.9423n
glitch19_20_->22=  75.7781p  targ=  53.0180n   trig=  52.9423n
glitch21_22_->23=  75.5536p  targ=  58.0179n   trig=  57.9423n
glitch23_24_->31=  75.1078p  targ=  63.0169n   trig=  62.9418n
glitch23_24_->30=  75.7310p  targ=  63.0175n   trig=  62.9418n
glitch23_24_->28=  76.3301p  targ=  63.0181n   trig=  62.9418n
glitch25_26_->27=  75.2596p  targ=  68.0173n   trig=  67.9421n
glitch27_28_->31=  75.5290p  targ=  73.0178n   trig=  72.9422n
glitch27_28_->30=  76.1776p  targ=  73.0184n   trig=  72.9422n
glitch29_30_->31=  75.0625p  targ=  78.0173n   trig=  77.9422n
glitch31_0_->30= 701.7234f  targ=  83.0179n   trig=  83.0172n
glitch31_0_->28= 638.0213f  targ=  83.0186n   trig=  83.0179n
glitch31_0_->24= 615.2443f  targ=  83.0192n   trig=  83.0186n
glitch31_0_->16= 740.3555f  targ=  83.0199n   trig=  83.0192n
pvdd=-134.6626u  from=   5.0000n     to=  85.0000n
```

Figure 22 Glitch & power consumption

Power consumption = 134.6626μW

Number to number	Glitch value	Glitch time	
1~2	3	75.1808ps	
3~4	7	75.4132ps	
	6	76.0834ps	
5~6	7	75.1924ps	
7~8	15	75.1010ps	
	14	75.8006ps	
	12	76.4258ps	
9~10	11	75.1151ps	
11~12	15	75.2598ps	
	14	75.9397ps	
13~14	15	75.4027ps	
15~16	31	75.4941ps	
	30	76.1558ps	
	28	76.7543ps	
	24	77.3213ps	
17~18	19	75.3476ps	
19~20	23	75.1106ps	
	22	75.7781ps	
21~22	23	75.5536ps	
23~24	31	75.1078ps	
	30	75.7310ps	
	28	76.3301ps	
25~26	27	75.2596ps	
27~28	31	75.5290ps	
	30	76.1776ps	
29~30	31	75.0625ps	
31~0	30	701.7234fs	2.695ps
	28	638.0213fs	
	24	615.2443fs	
	16	740.3555fs	

Table 6 Glitch(紅字代表該數字轉換的總 glitch time)

Maximum glitch = 77.3213ps

從結果來看，降低 VDD 和 unit inverter size 是可以並行的，因為結合兩者優點，使 power consumption 可以降到最低，maximum glitch 也符合題目要求的 80ps。

IV. Compared

	Power consumption	Maximum glitch
Original	744.5465μW	28.4369ps
Reduce VDD	259.4326μW	80.4022ps
Reduce size	387.3136μW	28.6180ps
Reduce both	134.6626μW	77.3213ps

Table 7 Compared

綜合 3 種降低 power consumption 和 maximum glitch 的策略，可以發現調低 VDD 是最有效可以降低 power consumption 的，但電路的 glitch 也因此上升，影響電路功能，相比之下降低 mos size 可以在不付出更多代價的情況下，也可以降低 power consumption。兩者結合雖然 glitch 也上升，但 size 調小後再降低 VDD 的 glitch 也較會因此縮小一些，有更大的容錯空間。

2. Please design a 5-bit pseudo-random-bit-sequence (PRBS) generator with Linear Feedback Shift Register (LFSR) with clock frequency CLK = 400MHz, VDD = 1.8V (default), VSS = 0V. Try to minimize the power consumption of the PRBS generator.

(a) Please describe how you design the PRBS generator and show the pseudo-randomsequence result to prove your design. (20%)

Linear shift feedback register(LFSR)原理:

在電路上實現 5-bits 的 LFSR 需要用 5 個 flip flop 和 1 個 XOR gate，可以透過更換 XOR 的 input 得到不同的偽隨機 bits stream，會稱為偽隨機是因為產生的亂數是可以計算的，但 LFSR 無法產生為零的 bits。

以 5-bits 為例，LFSR 可以產生最多 31 種(2^n-1)不同 bits 為一循環的 bits stream，除此之外也可以產生每一循環都更少 bits 的搭配，下方舉兩個例子比較差異。

Type1: XOR inputs Q [4] & Q [5]

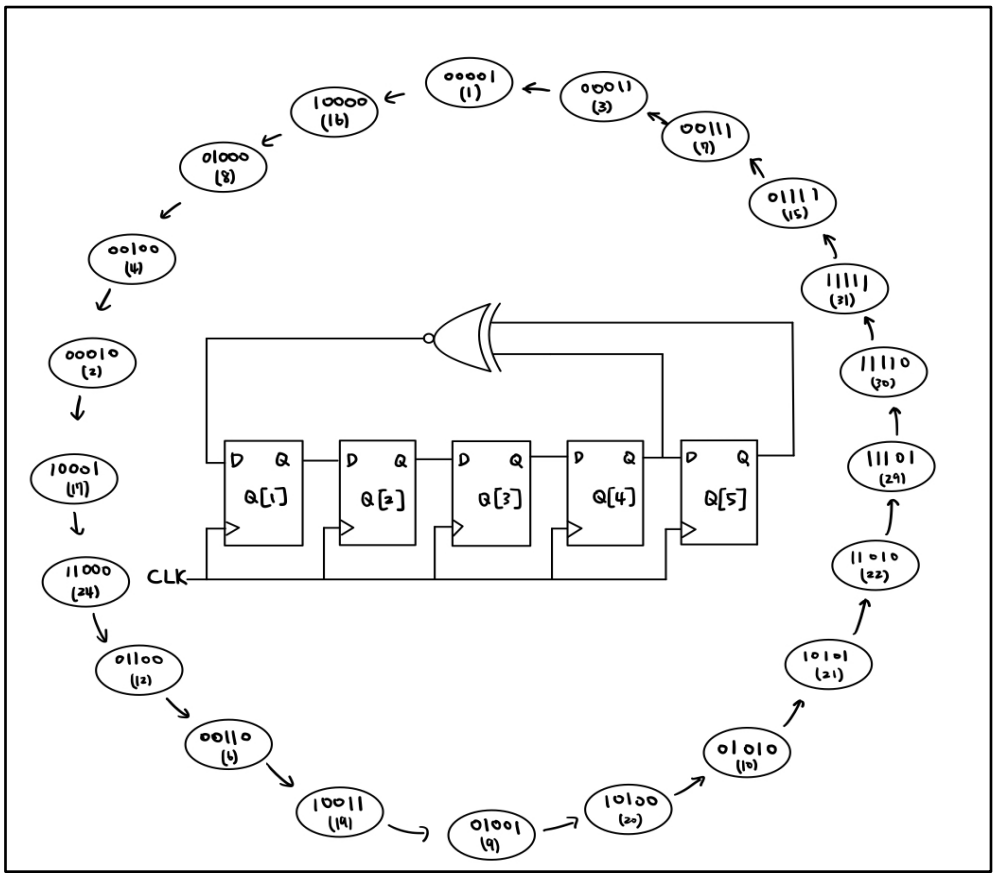

Figure 23 5-bits LFSR circuit design & state diagram

由推導 state diagram 可知將 XOR inputs 接在 Q [4]和 Q [5]可以得到 21 個 bits 為一循環的 LFSR。

Type2: XOR inputs Q [3] & Q [5]

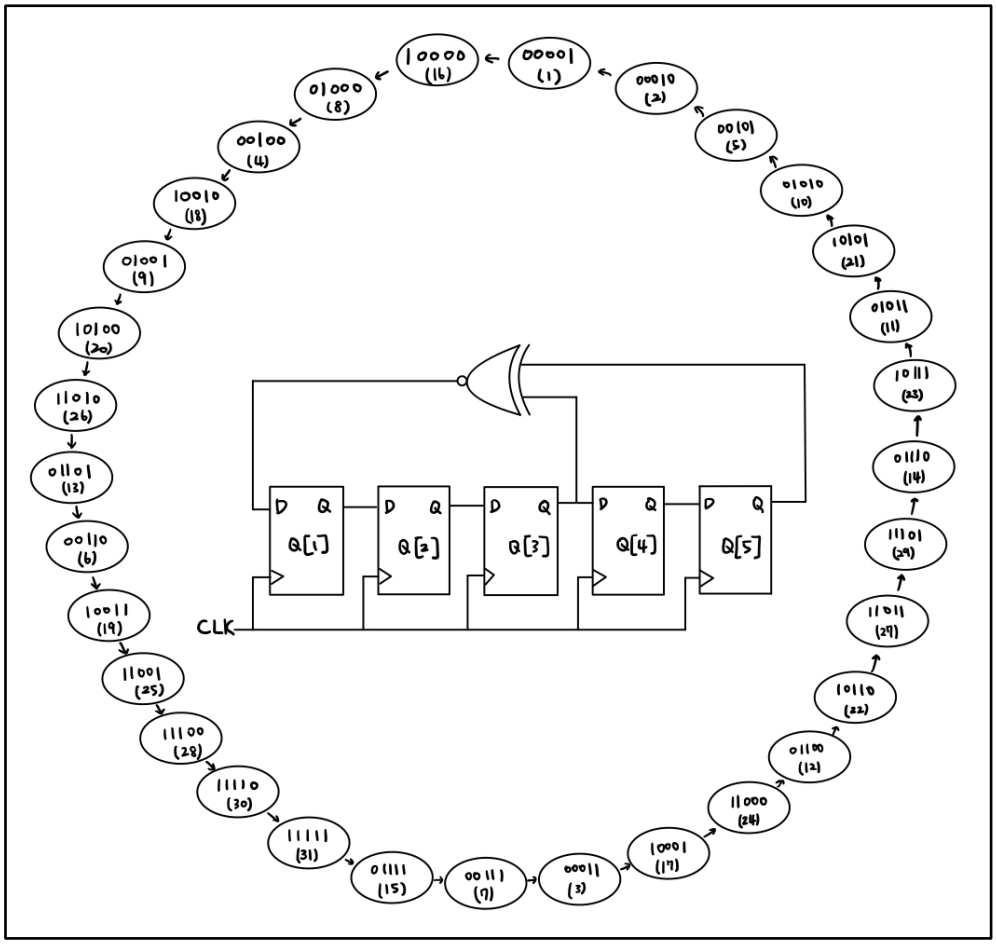

Figure 24 5-bits LFSR circuit design & state diagram

由推導 state diagram 可知將 XOR inputs 接在 Q [3]和 Q [5]可以得到 31 個 bits 為一循環的 LFSR。相比第一種設計，接在 Q[3]可以產生更多的偽隨機亂數，故本題採用第二種設計方法。

Schematic:

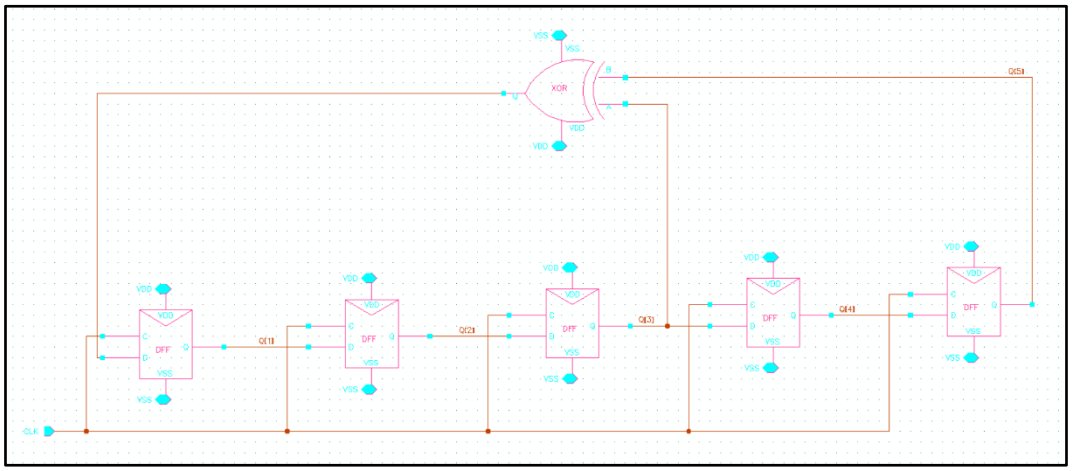

Figure 25

(b) Please measure the power of the PRBS generator. (5%)

此處採用與第一題相同的元件尺寸。

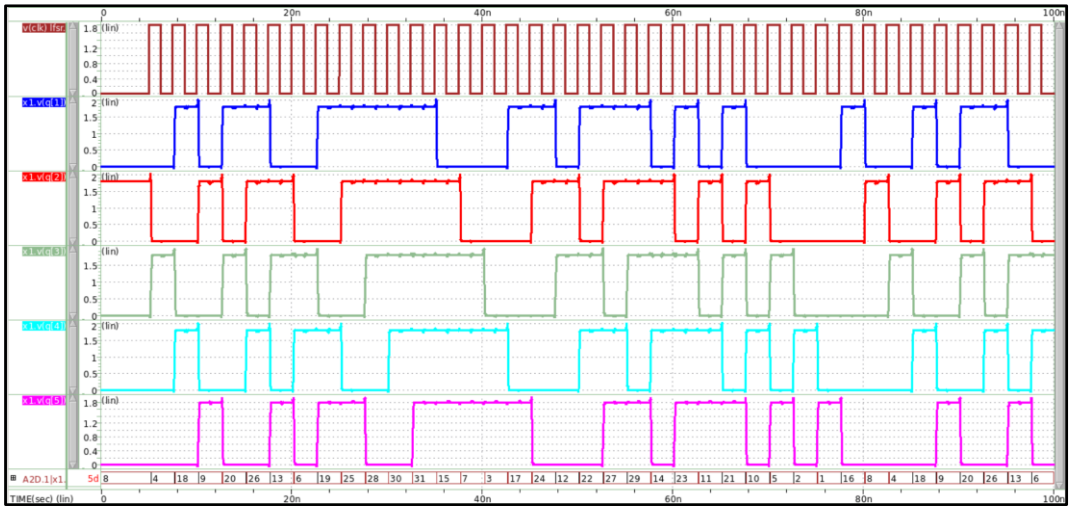

Figure 26 5-bit LFSR waveform

模擬與推導結果相符。

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
pvdd=-585.6083u  from=   5.0000n     to=  82.5000n
```

Power consumption = 585.6083μW

Minimize power consumption method

I. Reduce the VDD to 1.1V

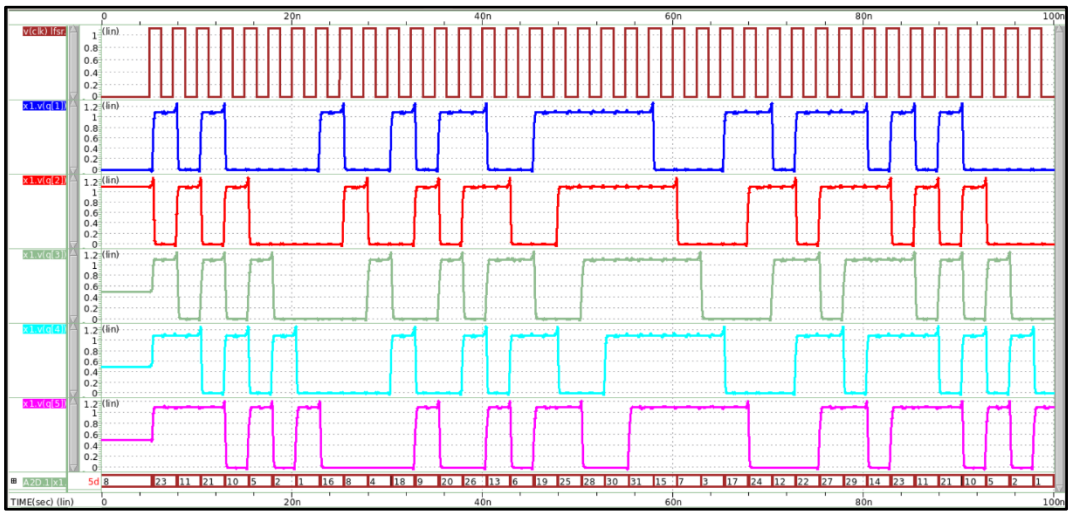

Figure 27 5-bit LFSR waveform

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
pvdd=-200.8452u  from=   5.0000n     to=  82.5000n
```

Power consumption = 200.8452μW

II. Reduce the unit inverter size

Size	Inverter	2-inputs NAND
PMOS	0.9u/0.18u, m = 1	0.52u/0.18u, m = 1
NMOS	0.3u/0.18u, m = 1	0.6u/0.18u, m = 1

Table 8 Resize

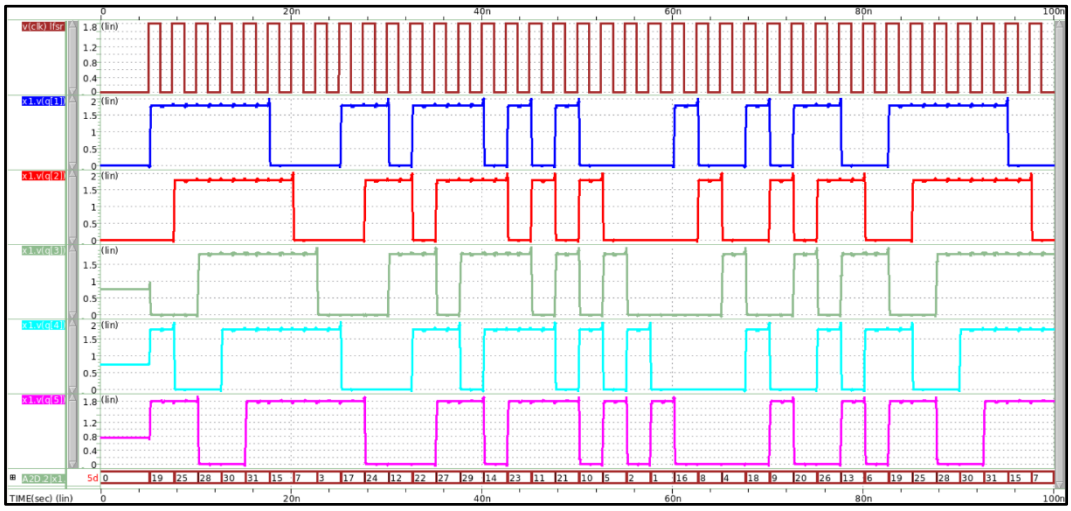

Figure 28 5-bit LFSR waveform

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
pvdd=-306.0010u  from=   5.0000n     to=  82.5000n
```

Power consumption = 306.0010μW

III. Reduce VDD & unit inverter size

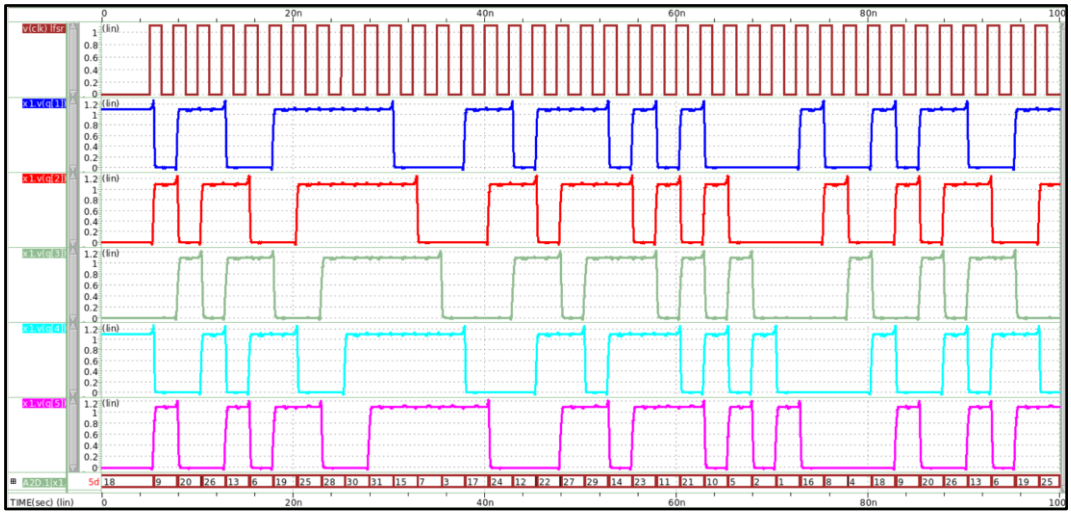

Figure 29 5-bit LFSR waveform

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
pvdd=-104.6785u  from=   5.0000n     to=  82.5000n
```

Power consumption = 104.6785μW

IV. Compared

	Original	Reduce VDD	Reduce size	Reduce both
Power consumption	585.6083μW	200.8452μW	306.0010μW	104.6785μW

Table 9 Compared

綜合 3 種降低 power consumption 和 maximum glitch 的策略，可以發現趨勢與第一題相同，調低 VDD 是有效可以降低 power consumption 的，降低 size 效益最差，兩者皆降的表現最佳。