超大型積體電路設計

VLSI Design

Final project

Group 15

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Content

I. Block Diagram

1. Draw top view of your system design and explain why you choose this architecture and how your design operated.
2. Draw sub-block in gate level and transistor level hierarchical and explain why you use them.

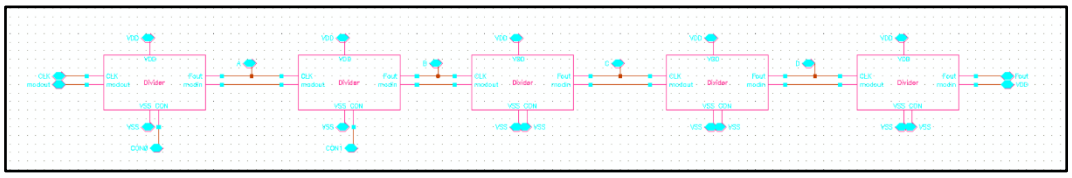

Figure 1 Multi Modulus Frequency Divider

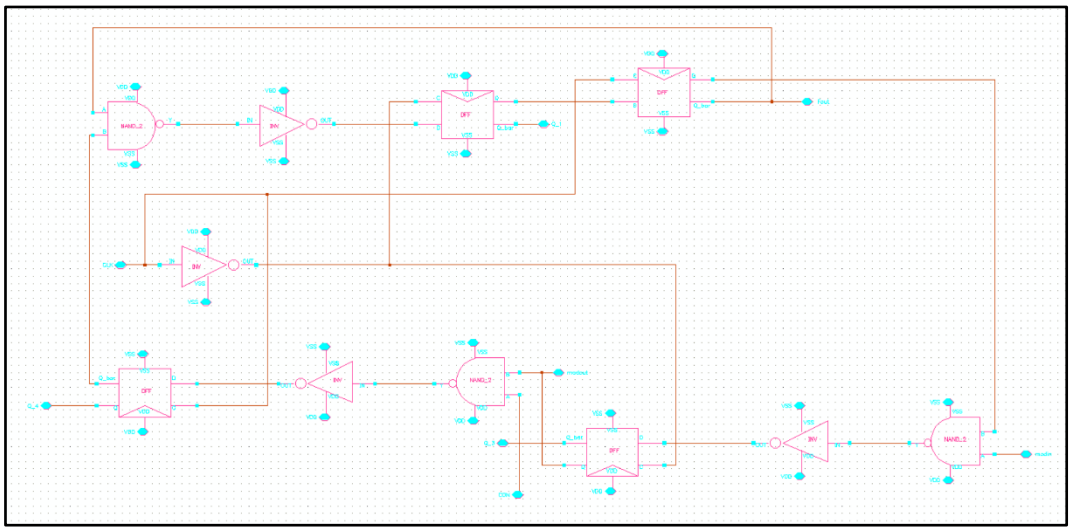

Figure 2 2/3 Divider

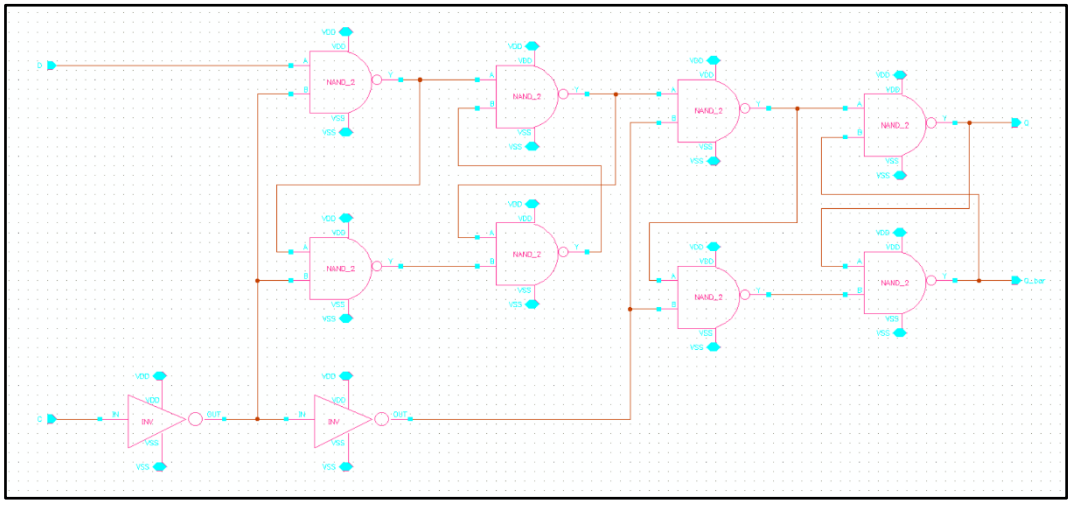

Figure 3 DFF

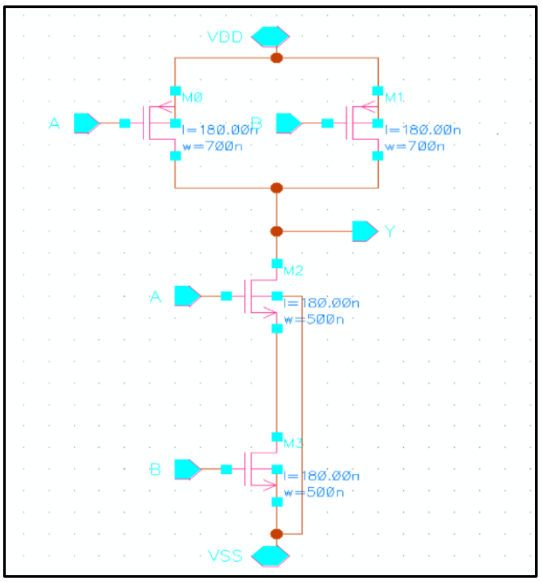

Figure 5 NAND

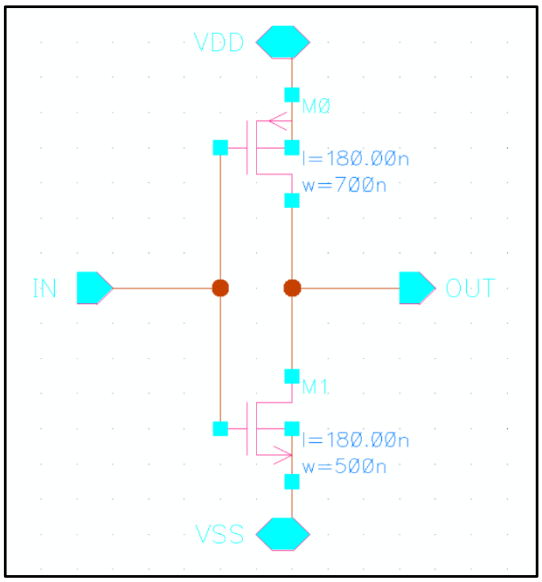

Figure 4 Inverter

i. 尺寸架構設計

首先我們進行 unit inverter μ 的比例測量，透過模擬得到 μ = 4.13。為了達到最小的延遲，我們透過計算確定 unit inverter 的 Pmos size 與 Nmos size 應該為 2:1，而 2-input NAND 的 Pmos size 與 Nmos size 應該為 2:2。經過一系列模擬後發現，電路上的電阻和電容可能影響了性能，使 NMOS size 可以更小，我們最終確定 Pmos size 與 Nmos size 為 1:1.2 時，能夠達到比原本更小功耗和更高頻率的效果。這種尺寸的設計不僅經過測試，在 5 個 corner 的情況下都能正常運作，同時也考慮到了 layout 的方便性。所以統一了 unit inverter 和 2-input NAND 的 SIZE，我們最終確定它們的 Pmos size 與 Nmos size 分別為 700n 和 500n。

ii. 電路架構設計

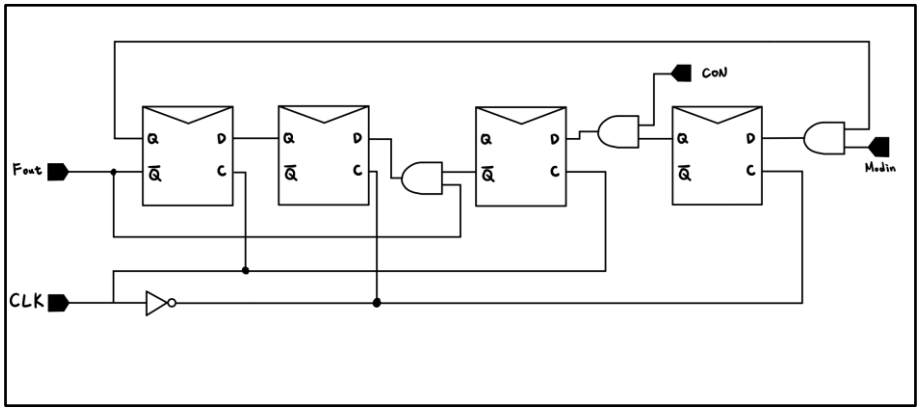

Figure 6 2/3 divider block diagram

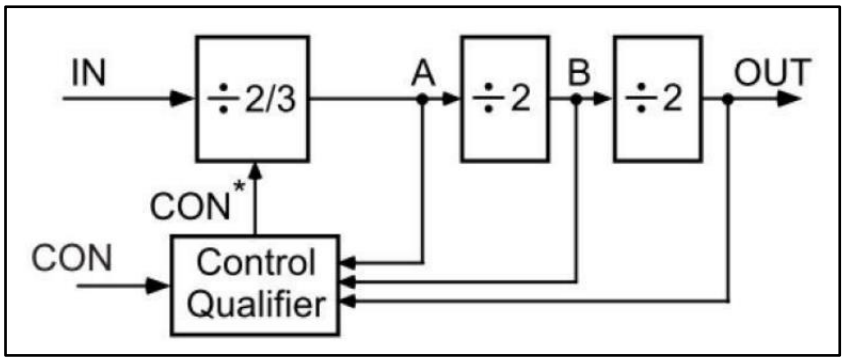

Figure 7

除頻器的電路架構如上圖所示是一個 8/9 的除頻器，透過第一個 CON 的訊號控制輸出 OUT 的輸出。而這次的題目是 32/33/34/35 的除頻器，所以為了達成目的，需要在後面多接一顆 2 的除頻器然後前面需要再多接一顆 2/3 的除頻器種共有 5 顆。前面兩顆 2/3 的除頻器分別接上 CON0 跟 CON1，當需要 32 的倍數時 CON0 = 0 跟 CON1 = 0，當需要 33 的倍數時 CON0 = 1 跟 CON1 = 0，當需要 34 的倍數時 CON0 = 0 跟 CON1 = 1，當需要 35 的倍數時 CON0 = 1 跟 CON1 = 1。

為了方便性，除頻器裡面的架構我們選擇的是使用 D flip-flop 來設計，因為這個架構所需要用到的元件除了剛剛提到的 D flip-flop 外只需要用到 2-input NAND 跟 inverter 而已，這些元件在前幾次功課已經設計過也 layout 過，知道怎樣設計有最小的 delay 設計上會比較方便。但是在查資料時發現，使用 T flip-flop 來設計 divider 可以有最快頻率，只是因為我們電路設計上有出問題，一直跑不出結果所以這次沒有使用。

II. Layout

1. Print-screen the whole design (with size & area) and sub-blocks.

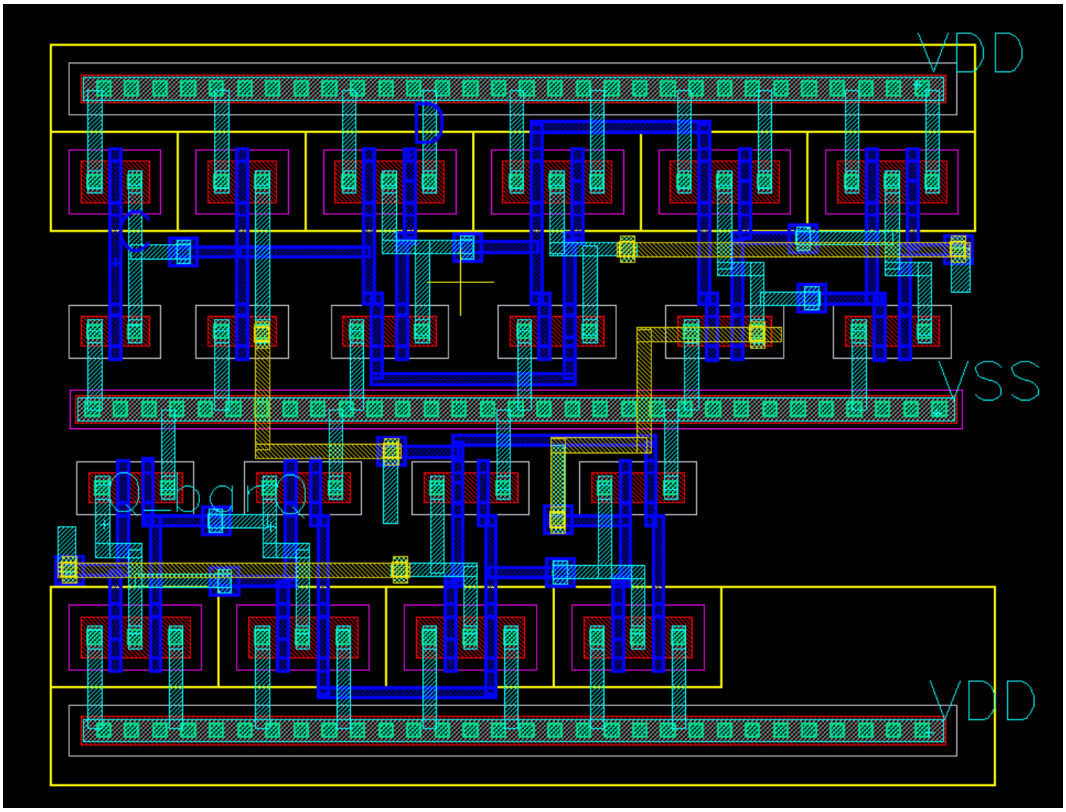

Figure 8 DFF

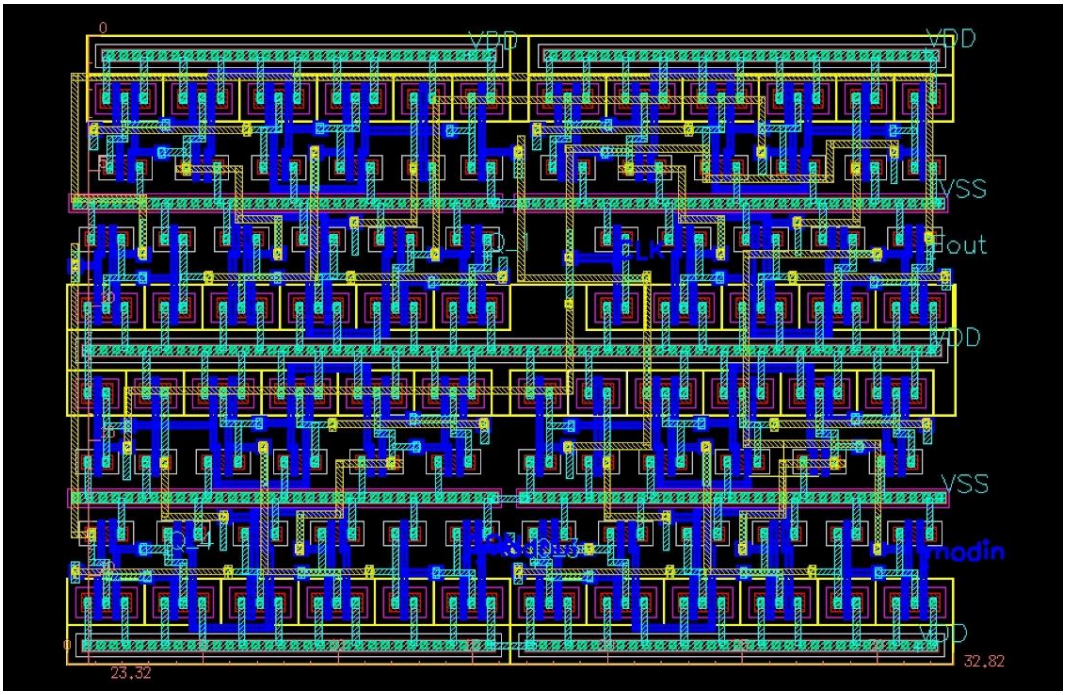

Figure 9 2/3 Divider

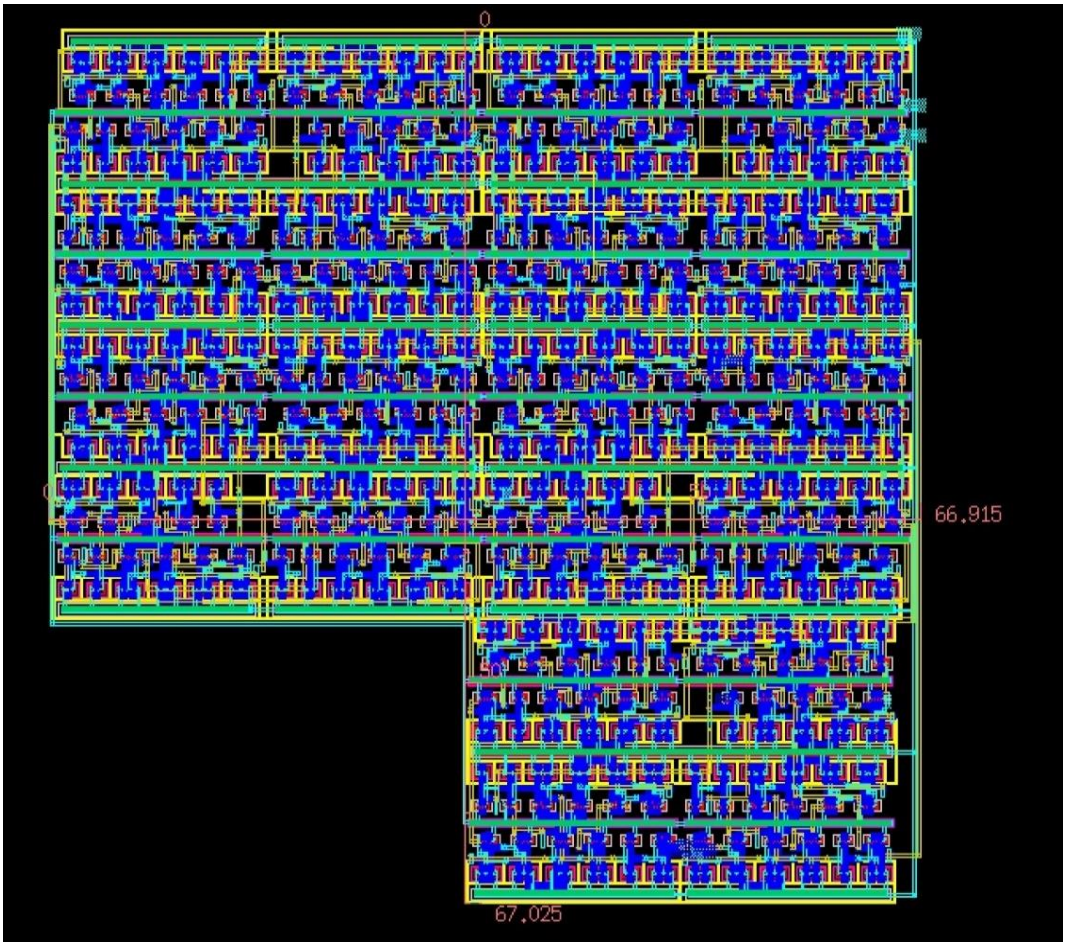

Figure 10 Multi Modulus Frequency Divider Layout

Area = 67.025 x 66.915 = 4484.978µm^2

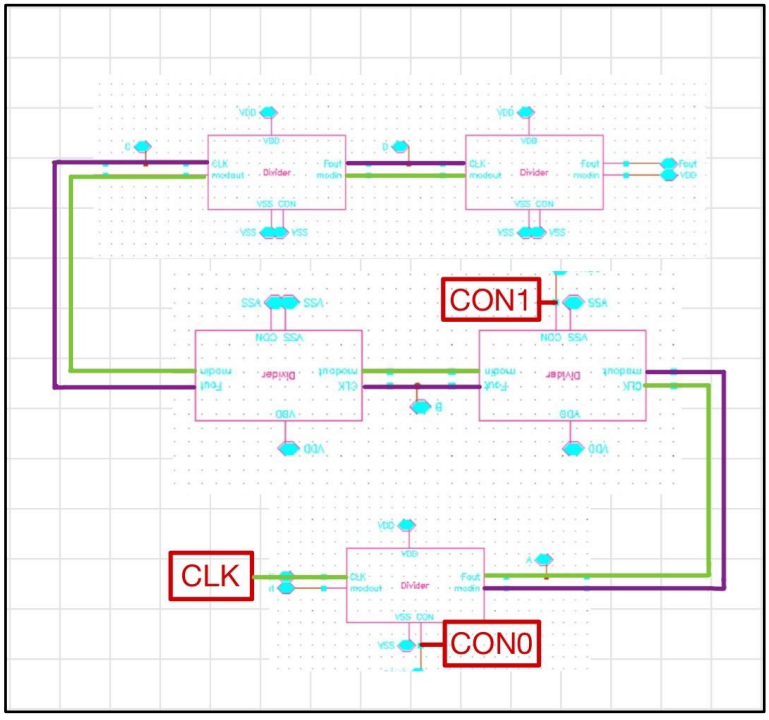

Figure 11 Multi Modulus Frequency Divider block diagram

2. DRC summary with no error (excluding the optional rules).

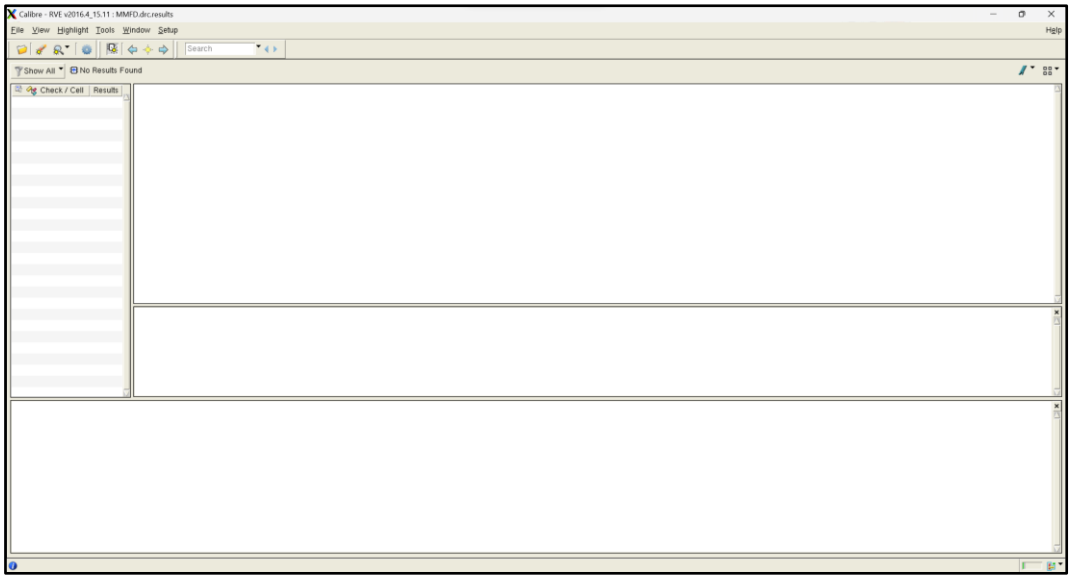

Figure 12 DRC

3. LVS report.

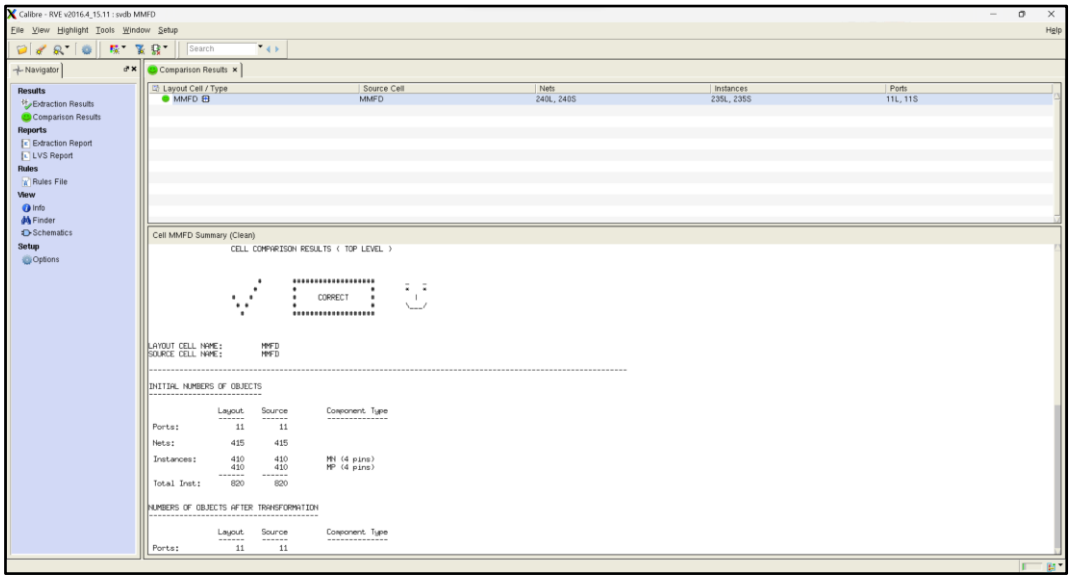

Figure 13 LVS

III. Simulation result

1. Pre-sim results & post-sim results, need to compare and explain the difference between them.

Fmax:

Corner	TT	SS	FF	SF	FS
Pre-sim	1GHz	312.5MHz	1.25GHz	625MHz	909.1MHz
Post-sim	833MHz	263.2MHz	1.11GHz	455MHz	833MHz

Power:

TT

Mode	32	33	34	35	Average
Pre-sim	1.3646mW	1.3440mW	1.3442mW	1.3254mW	1.3446mW
Post-sim	1.3495mW	1.3283mW	1.3288mW	1.3094mW	1.3290mW

SS

Mode	32	33	34	35	Average
Pre-sim	501.5137μW	493.9742μW	494.1036μW	487.1971μW	494.1972μW
Post-sim	476.2655μW	474.0427μW	474.1646μW	467.3202μW	472.9483μW

FF

Mode	32	33	34	35	Average
Pre-sim	1.7365mW	1.7101mW	1.7105mW	1.6863mW	1.7109mW
Post-sim	1.8405mW	1.8115mW	1.8121mW	1.7855mW	1.8124mW

SF

Mode	32	33	34	35	Average
Pre-sim	956.2825μW	941.8394μW	942.2794μW	928.8981μW	942.3249μW
Post-sim	812.9653μW	800.3522μW	800.5617μW	789.0145μW	800.7234μW

FS

Mode	32	33	34	35	Average
Pre-sim	1.2402mW	1.2214mW	1.2217mW	1.2046mW	1.2219mW
Post-sim	1.3517mW	1.3305mW	1.3309mW	1.3115mW	1.3312mW

比較 presim 和 postsim 的結果，postsim 的頻率相比 presim 略為下降，推測是因為 postsim 的電路會加入更多寄生電容與電阻導致的。較特別的是 postsim 的 power 都較 presim 小，原本認為加入寄生電容與電阻會使功耗上升，但模擬結果卻相反。

2. Waveforms (cursor is needed) and tables (filled with measured data) for all modulus modes.

Pre-sim:

Mode =32

Mode =33

Mode =34

Mode =35

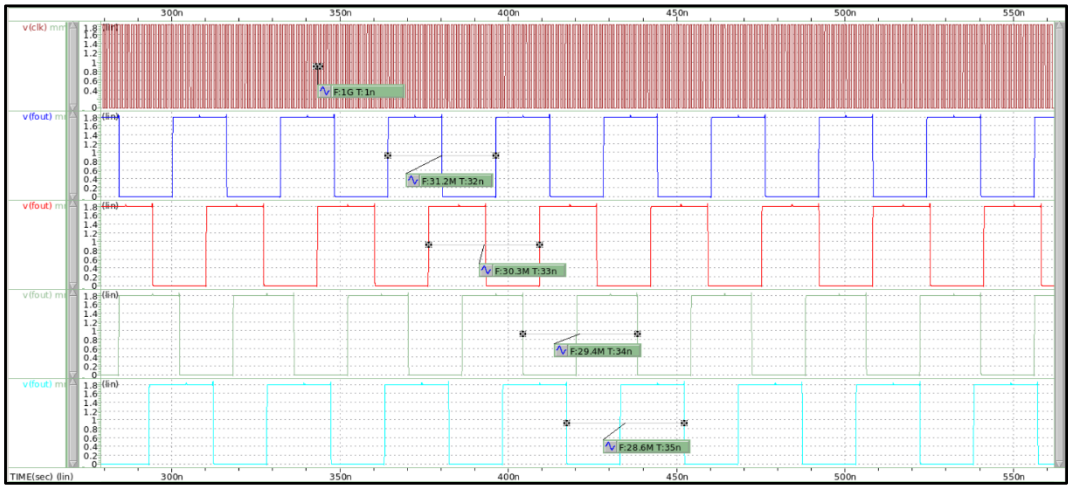

Figure 14 TT corner

Mode =32

Mode =33

Mode =34

Mode =35

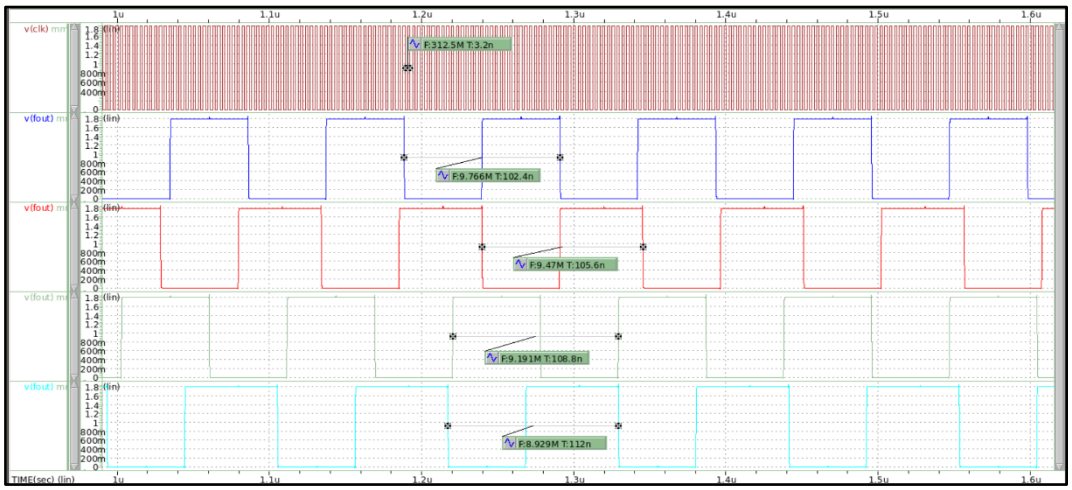

Figure 15 SS corner

Mode =32

Mode =33

Mode =34

Mode =35

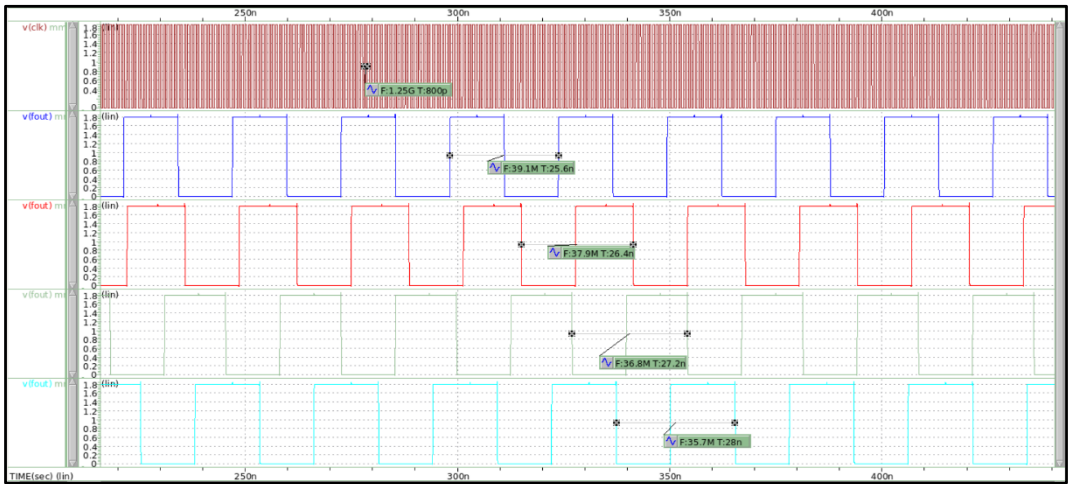

Figure 16 FF corner

Mode =32

Mode =33

Mode =34

Mode =35

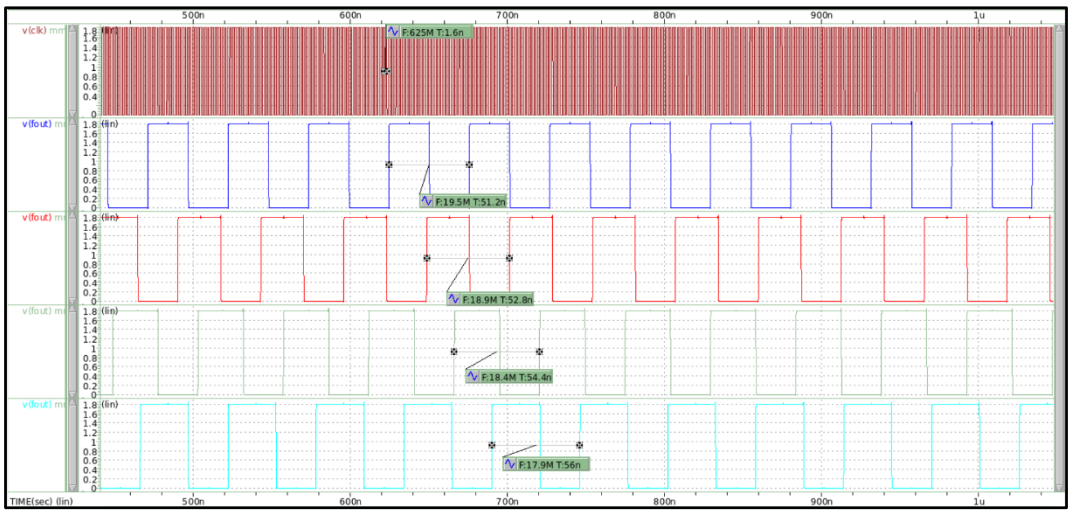

Figure 17 SF corner

Mode =32

Mode =33

Mode =34

Mode =35

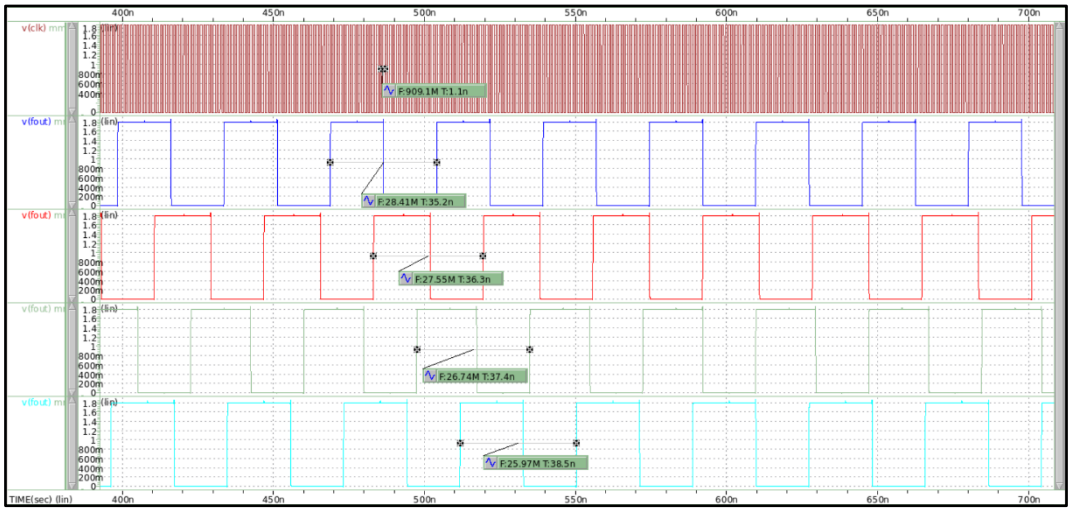

Figure 18 FS corner

Corner	Fmax	Power_div32	Power_div33	Power_div34	Power_div35
TT	1GHz	1.3646mW	1.3440mW	1.3442mW	1.3254mW
SS	312.5 MHz	501.5137µW	493.9742µW	494.1036µW	487.1971µW
FF	1.25GHz	1.7365mW	1.7101mW	1.7105mW	1.6863mW
SF	625 MHz	956.2825µW	941.8394µW	942.2794µW	928.8981µW
FS	909.1 MHz	1.2402mW	1.2214mW	1.2217mW	1.2046mW

Post-sim:

Mode =32

Mode =33

Mode =34

Mode =35

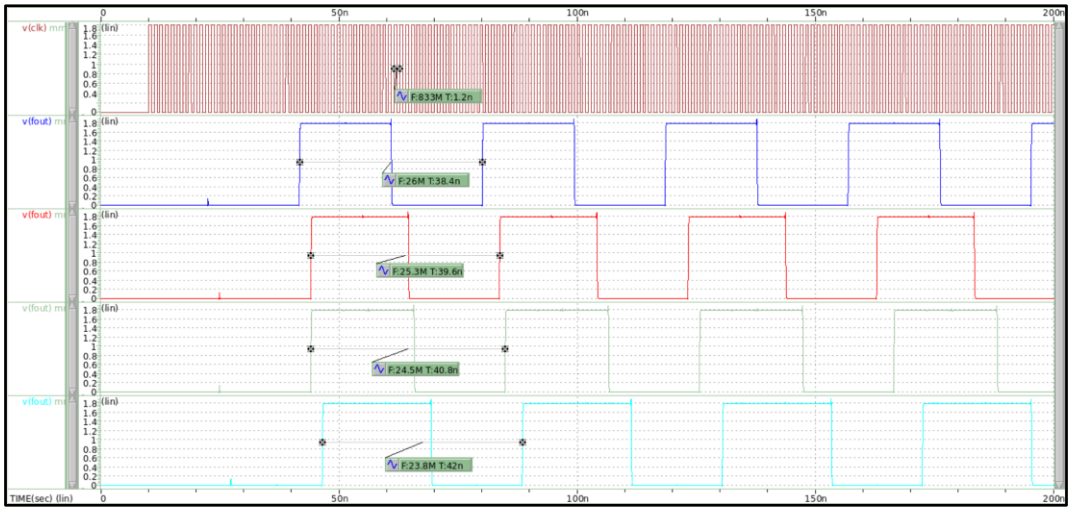

Figure 19 TT corner

Mode =32

Mode =33

Mode =34

Mode =35

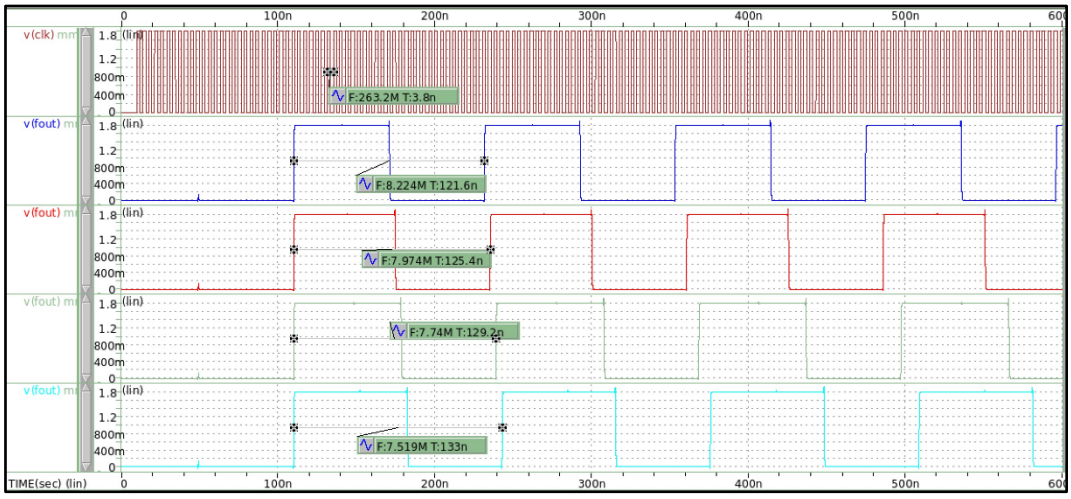

Figure 20 SS corner

Mode =32

Mode =33

Mode =34

Mode =35

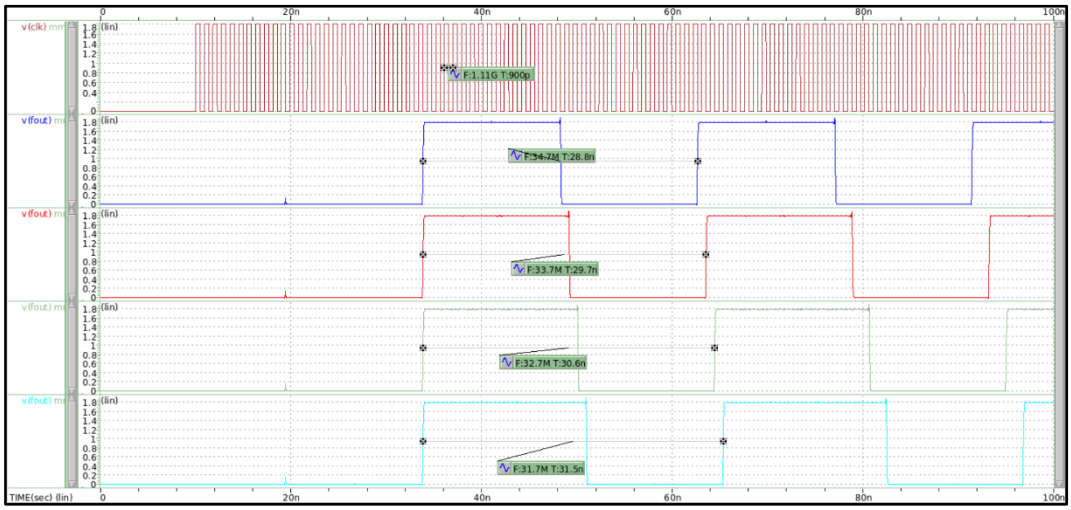

Figure 21 FF corner

Mode =32

Mode =33

Mode =34

Mode =35

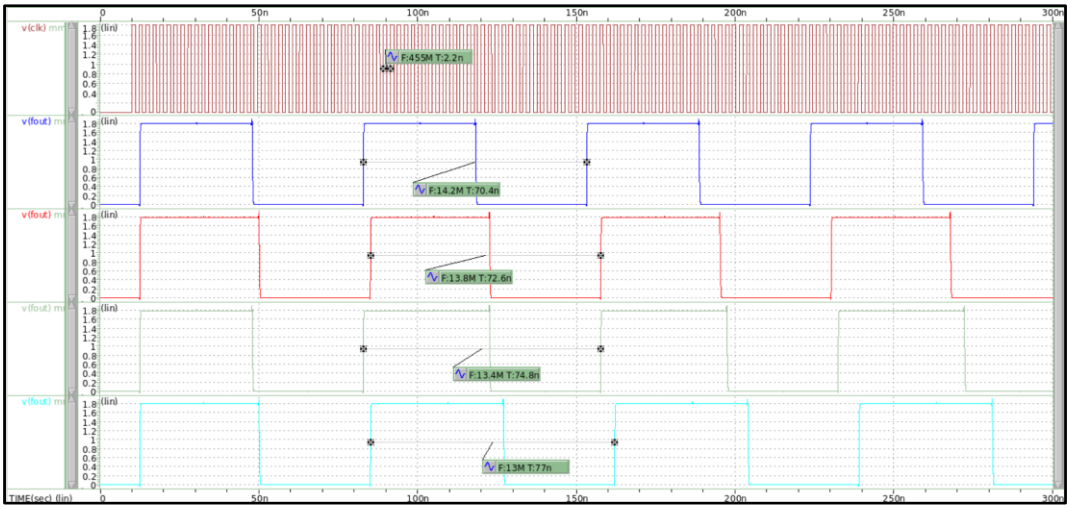

Figure 22 SF corner

Mode =32

Mode =33

Mode =34

Mode =35

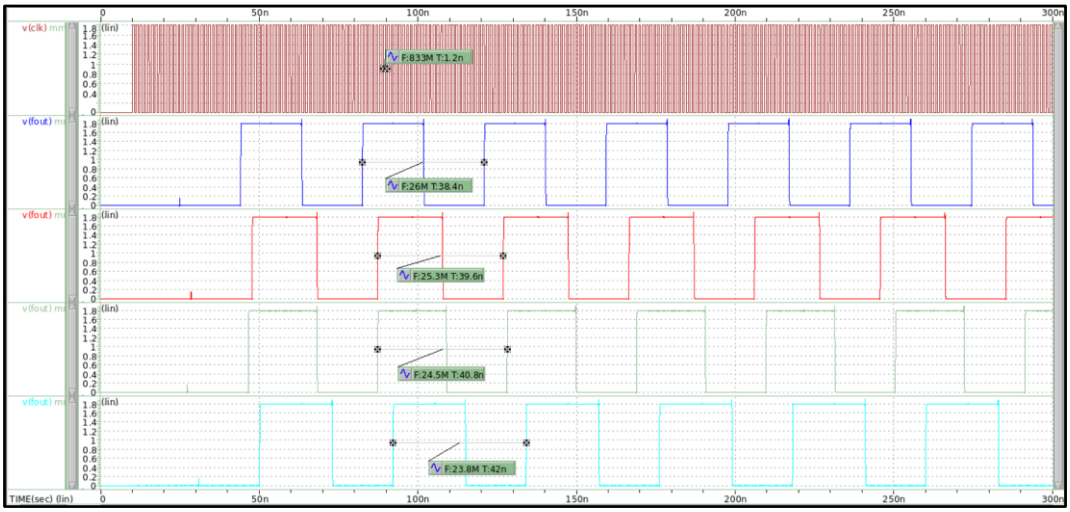

Figure 23 FS corner

Corner	Fmax	Power_div32	Power_div33	Power_div34	Power_div35	Area (μm^2)	FoM
TT	833MHz	1.3495mW	1.3283mW	1.3288mW	1.3094mW	**4484.978**	0.140
SS	263.2MHz	476.2655µW	474.0427µW	474.1646µW	467.3202µW		
FF	1.11GHz	1.8405mW	1.8115mW	1.8121mW	1.7855mW		
SF	455MHz	812.9653µW	800.3522µW	800.5617µW	789.0145µW		
FS	833MHz	1.3517mW	1.3305mW	1.3309mW	1.3115mW		

$$FoM = \frac{f_{max}}{Power \times Area} = 0.140 \ \frac{GHz}{W \times \mu m^2}$$

4. Discussion

首先看 presim 的結果，可以發現在 5 個 corner 下，TT 的 performance 與理論上相同在最中間，SS 的 frequency 最小，FF 的 frequency 最大，SF 相比 FS 的 frequency 小，推測是因為 DFF 中的 NAND 是 NMOS 串聯，故對 frequency 影響較大。Frequency 較快的 trade off 是電路的 power 會較大，故 FF 的 power 較大，SS 最小。在 4 個 mode(32、33、34、35)的比較下，可以發現 32 的 power 都較大，而 35 的 power 都較小。再看 postsim 的結果，模擬趨勢都與 presim 相同。

經過 1 個禮拜的努力終於完成了這份報告，當 layout 完成時，DRC 跟 LVS 通過後的當下滿滿的成就感。從要 layout 時就花了不少時間，主要是因為這次的題目會用到 5 個除頻器串聯在一起，在排版上沒這麼的方便，原本打算每個 divider 都 layout 成長寬比為一比五的長條形，然後在把 5 個 divider 併在一起就可以 layout 出一個完整的正方形，但是在實際 layout 上發現有點困難，主要是在 layout 單一個 divider 時如果要長條形，最後 metal 很難接，必須拉好幾條線連接頭尾以及 input 跟 output 線會在裡面不好拉出來，所以最後折衷的發法是把 divider layout 成二比三的長條形，然後一排兩個接在一起，最後會有一個自己接在最底下，雖然最後 layout 出來的形狀會少一個角，單是長跟寬差不多，也算是一個正方形了。

在這個作業中因為有 FoM 的比較，所以會有 trade off 需要取捨，主要是在提高頻率的設計中，功耗可能因此上升。面積較小的設計，基本上會有較好的 performance，這會取決於 layout 時的面積，產生的寄生電容對電路的影響，但要使面積下降，主要還是要從電路設計架構下手，如果在電路上可以使用較少的元件，例如將 D Flip Flop 換成其他種 Flip Flop 設計。