

[SoC Lab] Lab2

tags: SoC Lab, SOC Design

Student ID Name

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附上此篇Hackmd Link : <https://hackmd.io/@Sheng08/Hy8gkU2ep>

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 - Lab 2
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 - What is observed & learned
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 - Screen dump
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 - Note
 - 名詞解釋
 - 觀念補充
 - Troubleshooting
 - 補充

Lab 2

- https://github.com/bol-edu/course-lab_2

Brief introduction about the overall system

本次Lab2實驗中，主題為實作FIR並且使用兩種不同的Interface實作，分別為**AXI_Master**與**AXI_Stream**來傳輸測試資料。

設定這兩種Interface的方式也各有不同：

- AXI_Master: 透過 directive(.tcl) 設定
- AXI_Stream: 則使用 pragma (相似 Lab1) 設定

根據實驗結果，可以發現當需要傳輸大量資料時，

- **AXI_Master**在時間上(Latency)的表現較佳，其原因為**AXI_Stream**需依賴於額外的AXI_DMA資源協助且資料傳輸方式是基於FIFO，因此資料是逐一傳輸。
- **AXI_Master**則有Memory-mapping的特性，能直接地映射記憶體位址。

因此，如果需要以隨機存取的方式獲取測試資料，**AXI_Master**是較佳的選擇；而相對於連續地存取記憶體測試資料，則建議使用**AXI_Stream**。

What is observed & learned

Differences between MAXI and Stream interface

	MAXI	Stream
Latency of Kernel function	724 fast	6603
Execution time in online FPGA	0.26ms(0.00026s) fast	0.87ms (0.00087s)
Kernel func arguments	Pointer to an Array	hls:stream
Address Idea	Yes	No
Direction	Input/Output	Input / Output only
DMA	Not Need	Need
Storage for test data	Create Buffer	Define Stream

Differences between csim and cosim

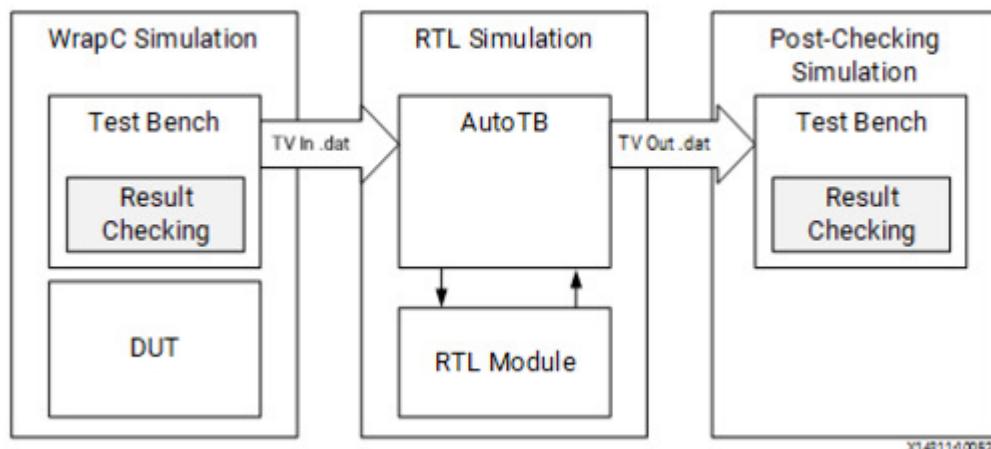
- **C Simulation:**

- 目的: 驗證C/C++的算法邏輯正確性
- 說明: 為初步的模擬階段，只涉及C/C++程式，不涉及任何硬體描述語言。基本上，這階段確保C/C++程式在未進行任何合成或硬體轉換的情況下運行正確性
- **Test bench** 和 **Top function** 會一同編譯成同一個執行檔(executable file)

- **Co Simulation:**

- 目的: 驗證合成後的HDL程式碼與C/C++原始碼的行為是否一致。
- 說明: 在這階段，原始C/C++程式碼和其合成的HDL程式碼將同時模擬。這是確保合成後的HDL實現與原始演算邏輯在功能上保持一致
- **Top function** 會在 Simulator 運行。而資料(test data)會於**Test bench** 和 Simulator 各自所執行的 process 之間傳輸

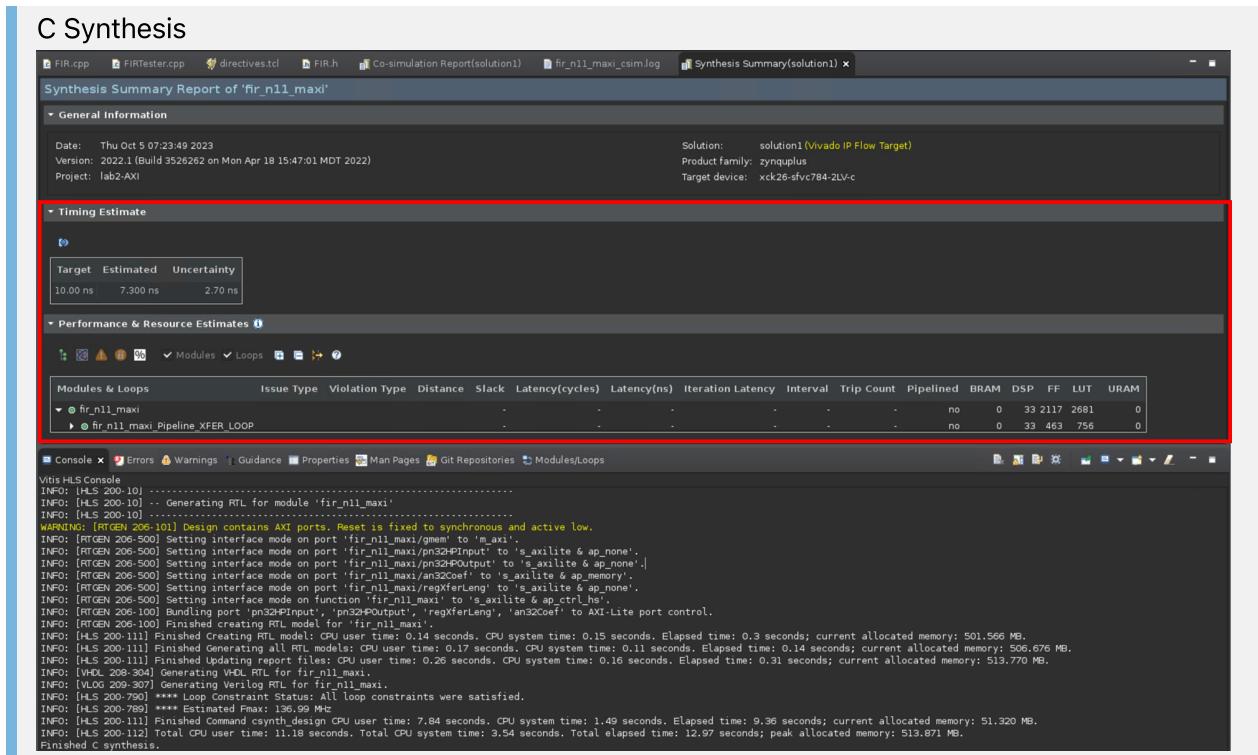
Figure: C/RTL Verification Flow



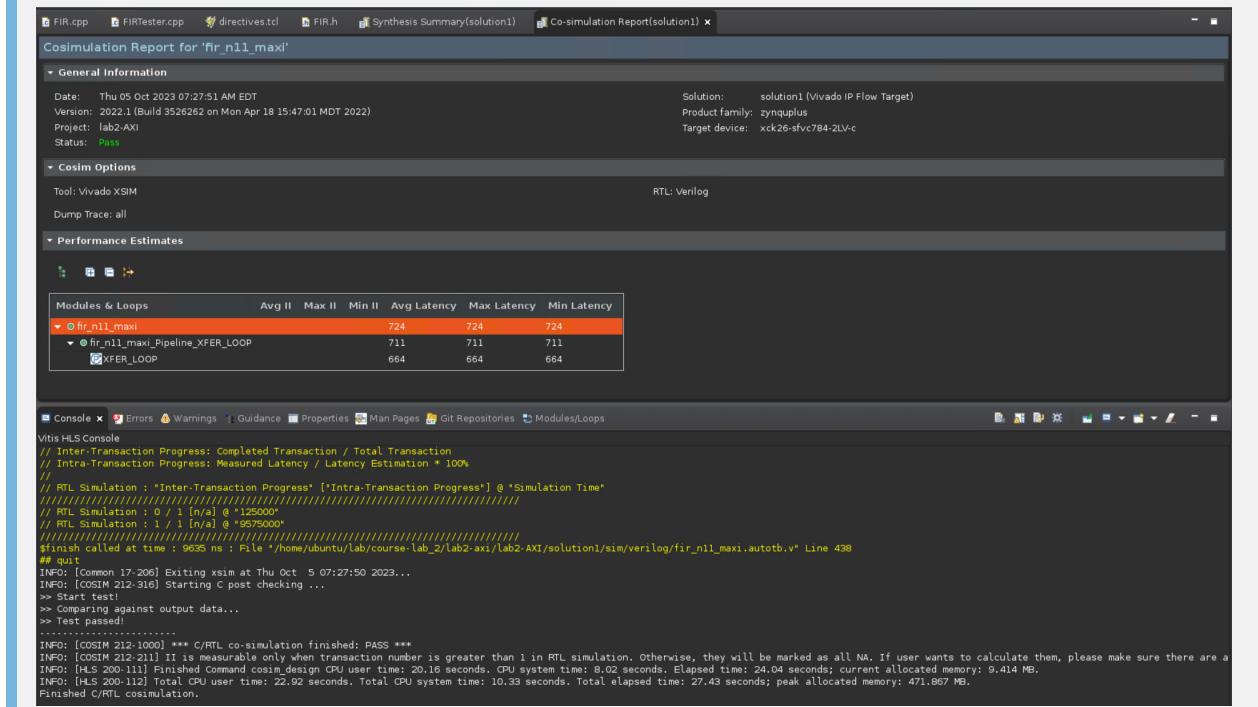
Screen dump

[FIRN11MAXI] FIR AXI-Master Interface

- Performance



Co-Simulation



csynth.rpt

Performance & Resource Estimates:													
Modules & Loops		Issue Type	Latency Stack (cycles)	Latency (ns)	Iteration Interval	Trip Count	Pipelined	BRAM	DSP	FF	LUT	URAM	
fir_n11_maxi		-	0.00	-	-	-	-	nol	33 (2%)	2117 (-0%)	2681 (2%)	-	
fir_n11_maxi_Pipeline_XFER_LOOP		-	0.00	-	-	-	-	nol	33 (2%)	463 (-0%)	756 (-0%)	-	
o XFER_LOOP		-	7.30	-	-	4	1	yes	-	-	-	-	

fir_n11_maxi_csynth.rpt

Performance Estimates																															
Timing:																															
* Summary:																															
<table border="1"> <thead> <tr> <th>Clock</th> <th>Target</th> <th>Estimated</th> <th>Uncertainty</th> </tr> </thead> <tbody> <tr> <td>lap_clk</td> <td>10.00 ns</td> <td>7.300 ns</td> <td>2.70 ns</td> </tr> </tbody> </table>														Clock	Target	Estimated	Uncertainty	lap_clk	10.00 ns	7.300 ns	2.70 ns										
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lap_clk	10.00 ns	7.300 ns	2.70 ns																												
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<table border="1"> <thead> <tr> <th>Latency (cycles)</th> <th>Latency (absolute)</th> <th>Interval</th> <th>Pipeline</th> </tr> <tr> <th>min</th> <th>max</th> <th>min</th> <th>max</th> <th>min</th> <th>max</th> <th>Type</th> </tr> </thead> <tbody> <tr> <td>?</td> <td>?</td> <td>?</td> <td>?</td> <td>?</td> <td>?</td> <td>nol</td> </tr> </tbody> </table>														Latency (cycles)	Latency (absolute)	Interval	Pipeline	min	max	min	max	min	max	Type	?	?	?	?	?	?	nol
Latency (cycles)	Latency (absolute)	Interval	Pipeline																												
min	max	min	max	min	max	Type																									
?	?	?	?	?	?	nol																									
* Detail:																															
* Instance:																															
<table border="1"> <thead> <tr> <th>Instance</th> <th>Module</th> <th>Latency (cycles)</th> <th>Latency (absolute)</th> <th>Interval</th> <th>Pipeline</th> </tr> <tr> <th>grp_fir_n11_maxi_Pipeline_XFER_LOOP_fu_242</th> <th>fir_n11_maxi_Pipeline_XFER_LOOP</th> <td>?</td> <td>?</td> <td>?</td> <td>?</td> <td>nol</td> </tr> </thead> </table>														Instance	Module	Latency (cycles)	Latency (absolute)	Interval	Pipeline	grp_fir_n11_maxi_Pipeline_XFER_LOOP_fu_242	fir_n11_maxi_Pipeline_XFER_LOOP	?	?	?	?	nol					
Instance	Module	Latency (cycles)	Latency (absolute)	Interval	Pipeline																										
grp_fir_n11_maxi_Pipeline_XFER_LOOP_fu_242	fir_n11_maxi_Pipeline_XFER_LOOP	?	?	?	?	nol																									
* Loop:																															
N/A																															

- Utilization

IMPLEMENTED DESIGN - Som Vision Platform Board

Project Summary Device Overview Dashboard Board Part Sources Netlist Subblock Properties Netlist

Display name: Kria KV260 Vision AI Starter Kit
Board part name: xilinx.com:kv260_som:part0:1.3
Board revision: Rev_B01
Connectors: No connections
Repository path: /tools/Xilinx/Vivado/2022.1/data/hub/boards
URL: www.xilinx.com
Board overview: Kria KV260 Vision AI starter Kit
[Changes](#)



Synthesis

Status: ✓ Complete	Messages: 795 warnings
Active run: synth_1	Part: Som Vision Platform Board
Strategy: Vivado Synthesis Defaults	Report Strategy: Vivado Synthesis Default Reports
Report Strategy: Automatically selected checkpoint	Incremental synthesis: None

DRC Violations

Summary: 73 warnings
[Implemented DRC Report](#)

Implementation

Status: ✓ Complete	Messages: 74 warnings
Active run: impl_1	Part: Som Vision Platform Board
Strategy: Vivado Implementation Defaults	Report Strategy: Vivado Implementation Default Reports
Report Strategy: Implemented Power Report	Incremental implementation: None

Timing

Worst Negative Slack (WNS): 2.896 ns
Total Negative Slack (TNS): 0 ns
Number of Falling Endpoints: 0
Total Number of Endpoints: 24159
Implemented Timing Report

Utilization

Post-Synthesis | Post-Implementation

Graph | Table

Utilization (%)

Power

Total On-Chip Power: 2.761 W
Junction Temperature: 31.4 °C
Thermal Margin: 53.6 °C (22.8 W)
Effective 9JA: 2.3 °C/W
Power supplied to off-chip devices: 0 W
Confidence level: Medium
Implemented Power Report

Summary | **Route Status** | **Failed Nets**

Tcl Console | Messages | Log | Reports | Intelligent Design Runs | Design Runs | DRC | Methodology | Power | Timing

- Interface

csynth.rpt

= HW Interfaces										
* M_AXI										
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+										
Interface Data Width Address Width Latency Offset Register Max Widens Max Read Max Write Num Read Num Write										
(SW→HW) Bitwidth Burst Length Burst Length Outstanding Outstanding										
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+										
m_axi_gmem 32 → 32 64 0 slave 0 0 16 16 16 16										
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+										
* S_AXILITE Interfaces										
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+										
Interface Data Width Address Width Offset Register										
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+										
s_axi_control 32 7 16 0										
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+										
* S_AXILITE Registers										
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+										
Interface Register Offset Width Access Description Bit Fields										
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+										
s_axi_control CTRL 0x00 32 RW Control signals 0=AP_START 1=AP_DONE 2=AP_IDLE 3=AP_READY 7=AUTO_RESTART 9=INTERRUPT										
s_axi_control GIER 0x04 32 RW Global Interrupt Enable Register 0=Enable										
s_axi_control IP_IER 0x08 32 RW IP Interrupt Enable Register 0=CHAN0_INT_EN 1=CHAN1_INT_EN										
s_axi_control IP_ISR 0x0c 32 RW IP Interrupt Status Register 0=CHAN0_INT_ST 1=CHAN1_INT_ST										
s_axi_control pn32HPInput_1 0x10 32 W Data signal of pn32HPInput										
s_axi_control pn32HPInput_2 0x14 32 W Data signal of pn32HPInput										
s_axi_control pn32HPOutput_1 0x1c 32 W Data signal of pn32HPOutput										
s_axi_control pn32HPOutput_2 0x20 32 W Data signal of pn32HPOutput										
s_axi_control regXferLeng 0x28 32 W Data signal of regXferLeng										
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+										
* TOP LEVEL CONTROL										
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+										
Interface Type Ports										
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+										
ap_clk clock ap_clk										
ap_rst_n reset ap_rst_n										
interrupt interrupt interrupt										
ap_ctrl ap_ctrl_hs										
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+										

fir_n11_maxi_csynth.rpt

= Interface						
* Summary:						
+-----+-----+-----+-----+-----+-----+-----+						
RTL Ports Dir Bits Protocol Source Object C Type						
+-----+-----+-----+-----+-----+-----+-----+						
s_axi_control_AWVALID in 1 s_axi control array						
s_axi_control_AWREADY out 1 s_axi control array						
s_axi_control_AWADDR in 7 s_axi control array						
s_axi_control_WVALID in 1 s_axi control array						
s_axi_control_WREADY out 1 s_axi control array						
s_axi_control_WDATA in 32 s_axi control array						
s_axi_control_WSTRB in 4 s_axi control array						
s_axi_control_ARVALID in 1 s_axi control array						
s_axi_control_ARREADY out 1 s_axi control array						
s_axi_control_ARADDR in 7 s_axi control array						
s_axi_control_RVALID out 1 s_axi control array						
s_axi_control_RREADY in 1 s_axi control array						
s_axi_control_RDATA out 32 s_axi control array						
s_axi_control_RRESP out 2 s_axi control array						
s_axi_control_BVALID out 1 s_axi control array						
s_axi_control_BREADY in 1 s_axi control array						
s_axi_control_BRESP out 2 s_axi control array						

s_axi_control_BRESP	out	2	s_axi	control	array
ap_clk	in	1	ap_ctrl_hs	fir_n11_maxi	return value
ap_rst_n	in	1	ap_ctrl_hs	fir_n11_maxi	return value
interrupt	out	1	ap_ctrl_hs	fir_n11_maxi	return value
m_axi_gmem_AWVALID	out	1	m_axi	gmem	pointer
m_axi_gmem_AWREADY	in	1	m_axi	gmem	pointer
m_axi_gmem_AWADDR	out	64	m_axi	gmem	pointer
m_axi_gmem_AWID	out	1	m_axi	gmem	pointer
m_axi_gmem_AWLEN	out	8	m_axi	gmem	pointer
m_axi_gmem_AWSIZE	out	3	m_axi	gmem	pointer
m_axi_gmem_AWBURST	out	2	m_axi	gmem	pointer
m_axi_gmem_AWLOCK	out	2	m_axi	gmem	pointer
m_axi_gmem_AWCACHE	out	4	m_axi	gmem	pointer
m_axi_gmem_AWPROT	out	3	m_axi	gmem	pointer
m_axi_gmem_AWQOS	out	4	m_axi	gmem	pointer
m_axi_gmem_AWREGION	out	4	m_axi	gmem	pointer
m_axi_gmem_AWUSER	out	1	m_axi	gmem	pointer
m_axi_gmem_WVALID	out	1	m_axi	gmem	pointer
m_axi_gmem_WREADY	in	1	m_axi	gmem	pointer
m_axi_gmem_WDATA	out	32	m_axi	gmem	pointer
m_axi_gmem_WSTRB	out	4	m_axi	gmem	pointer
m_axi_gmem_WLAST	out	1	m_axi	gmem	pointer
m_axi_gmem_WID	out	1	m_axi	gmem	pointer
m_axi_gmem_WUSER	out	1	m_axi	gmem	pointer
m_axi_gmem_ARVALID	out	1	m_axi	gmem	pointer
m_axi_gmem_ARREADY	in	1	m_axi	gmem	pointer
m_axi_gmem_ARADDR	out	64	m_axi	gmem	pointer
m_axi_gmem_ARID	out	1	m_axi	gmem	pointer
m_axi_gmem_ARLEN	out	8	m_axi	gmem	pointer
m_axi_gmem_ARSIZE	out	3	m_axi	gmem	pointer
m_axi_gmem_ARBURST	out	2	m_axi	gmem	pointer
m_axi_gmem_ARLOCK	out	2	m_axi	gmem	pointer
m_axi_gmem_ARCACHE	out	4	m_axi	gmem	pointer
m_axi_gmem_ARPROT	out	3	m_axi	gmem	pointer
m_axi_gmem_ARQOS	out	4	m_axi	gmem	pointer
m_axi_gmem_ARREGION	out	4	m_axi	gmem	pointer
m_axi_gmem_ARUSER	out	1	m_axi	gmem	pointer
m_axi_gmem_RVALID	in	1	m_axi	gmem	pointer
m_axi_gmem_RREADY	out	1	m_axi	gmem	pointer
m_axi_gmem_RDATA	in	32	m_axi	gmem	pointer
m_axi_gmem_RLAST	in	1	m_axi	gmem	pointer
m_axi_gmem RID	in	1	m_axi	gmem	pointer
m_axi_gmem_RUSER	in	1	m_axi	gmem	pointer
m_axi_gmem_RRESP	in	2	m_axi	gmem	pointer
m_axi_gmem_BVALID	in	1	m_axi	gmem	pointer
m_axi_gmem_BREADY	out	1	m_axi	gmem	pointer
m_axi_gmem_BRESP	in	2	m_axi	gmem	pointer
m_axi_gmem_BID	in	1	m_axi	gmem	pointer

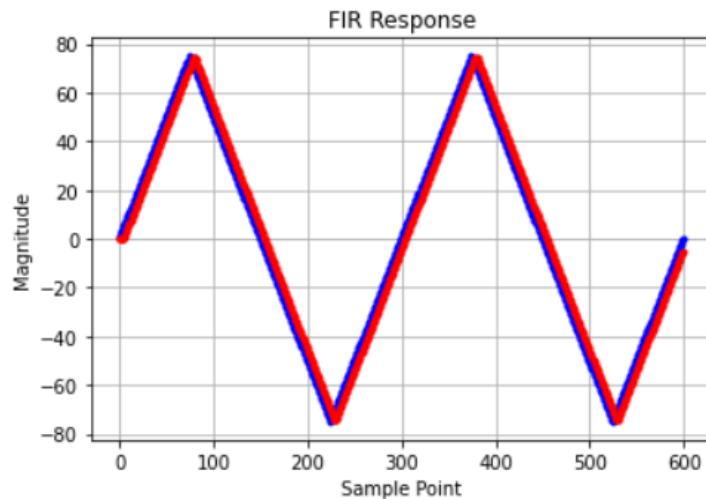
m_axi_gmem_BUSER	in	1	m_axi	gmem	pointer
+	-----+	+-----+	-----+	-----+	-----+

- Co-simulation transcript/waveform

Report time : Thu 05 Oct 2023 07:27:51 AM EDT.									
Solution : solution1.									
Simulation tool : xsim.									
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+									
Latency(Clock Cycles) Interval(Clock Cycles) Total Execution Time									
+ RTL + Status +-----+-----+-----+-----+-----+-----+-----+-----+-----+									
min avg max min avg max									
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+									
VHDL NA		NA NA		NA NA		NA NA		NA NA	
Verilog Pass		943 943		943 943		NA NA		NA NA	
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+									

- Jupyter Notebook execution result

```
Entry: /usr/local/share/pynq-venv/lib/python3.8/site-packages/ipykernel_launcher.py
System argument(s): 3
Start of "/usr/local/share/pynq-venv/lib/python3.8/site-packages/ipykernel_launcher.py"
Kernel execution time: 0.00026488304138183594 s
```



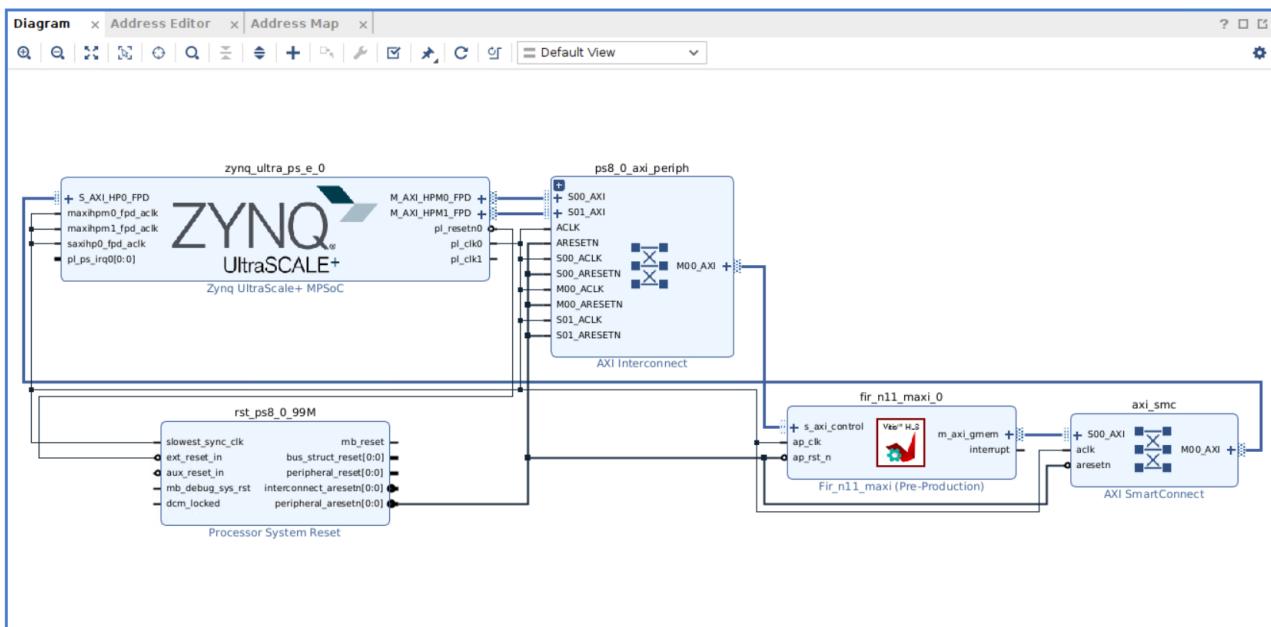
```
=====

```

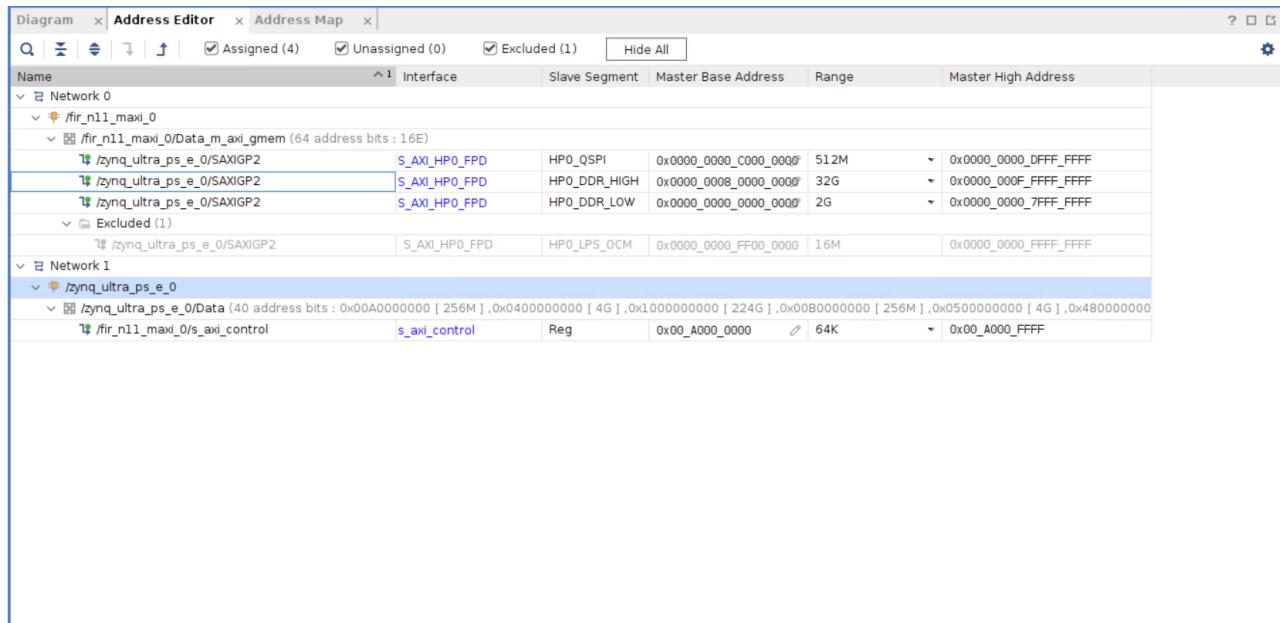
```
Exit process
```

[FIRN11MAXI] Screen dump (Other)

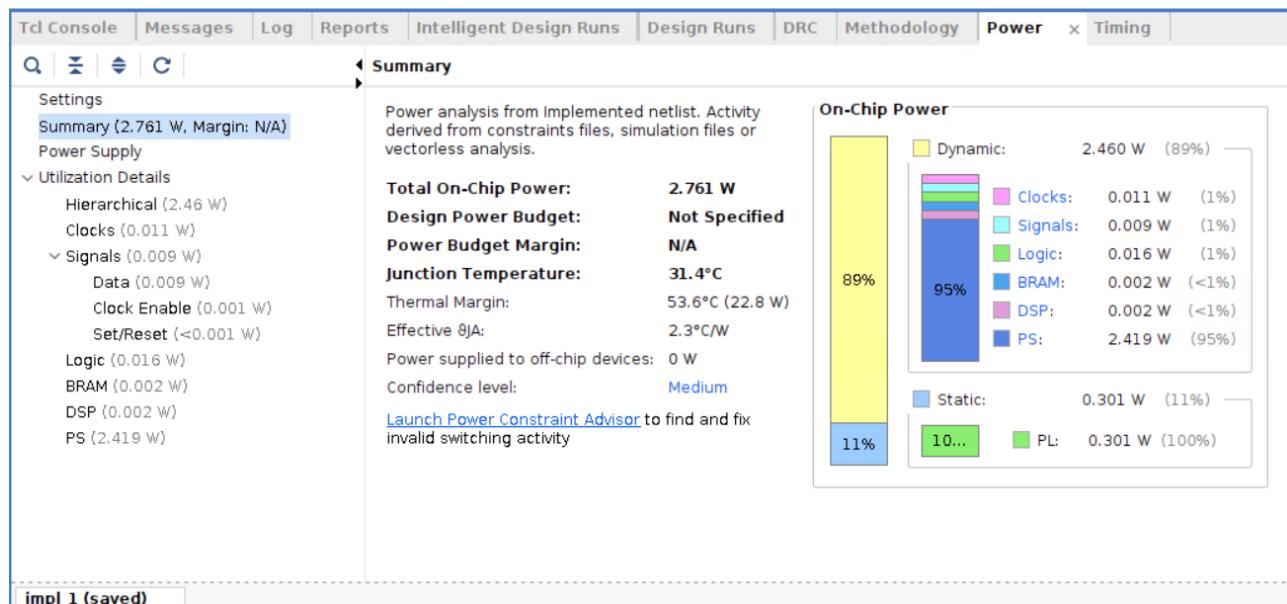
- Block Design



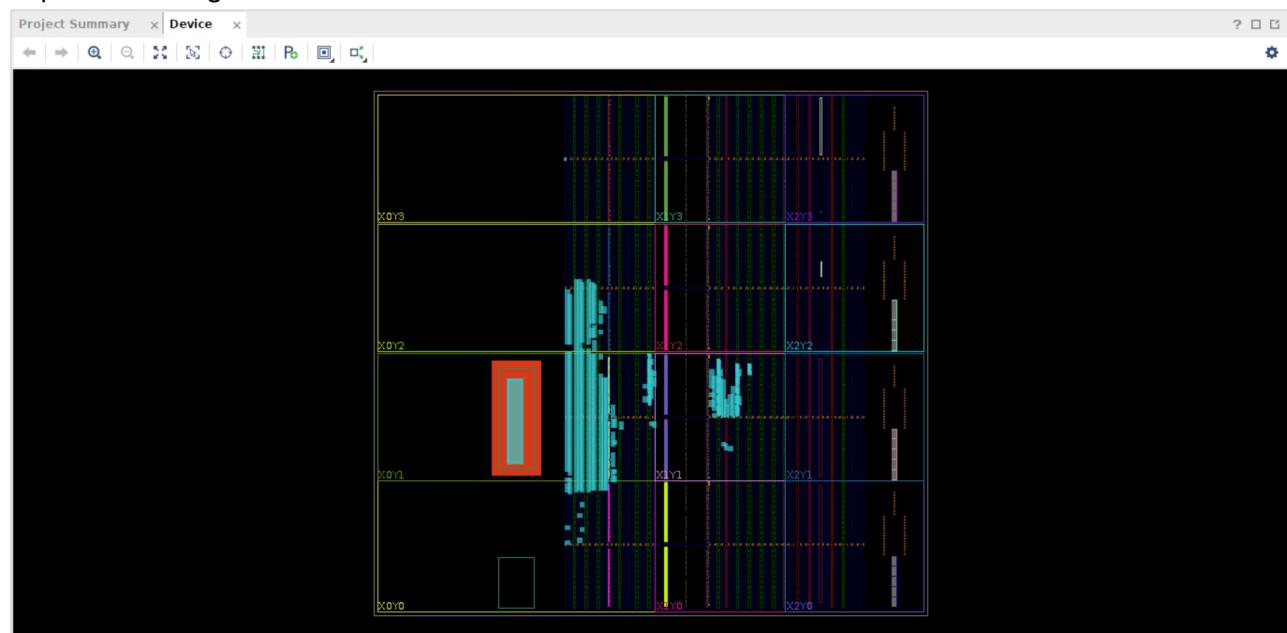
- Memory map



- Power



- Implement Design



[FIRN11Stream] FIR Stream Interface

- Performance

C Synthesis

Synthesis Summary Report of 'fir_n11_strm'

General Information

Date: Thu Oct 5 08:36:43 2023
Version: 2022.1 (Build 3526262 on Mon Apr 18 15:47:01 MDT 2022)
Project: lab2_Stream

Solution: solution1 (Vivado IP Flow Target)
Product family: zynqplus
Target device: xck26-sfvc784-2LV-c

Timing Estimate

Target	Estimated	Uncertainty
10.00 ns	6.290 ns	2.70 ns

Performance & Resource Estimates

Modules & Loops	Issue Type	Violation Type	Distance	Slack	Latency(cycles)	Latency(ns)	Iteration Latency	Interval	Trip Count	Pipelined	BRAM	DSP	FF	LUT	URAM
↳ fir_n11_strm	-	-	-	-	-	-	-	-	-	no	0	33	952	1082	0
↳ fir_n11_strm_Pipeline_XFER_LOOP	⌚ Violation	-	-	-	-	-	-	-	-	no	0	33	762	825	0
↳ XFER_LOOP	⌚ Violation	Resource Limitation	-	-	-	-	-	12	11	yes	-	-	-	-	-

Console

```
Vitis HLS Console
// ...
INFO: [RTGEN 206-500] Setting interface mode on port 'fir_n11_strm/pstrmOutput_v_glbp_V' to 'axis' (register, both mode).
INFO: [RTGEN 206-500] Setting interface mode on port 'fir_n11_strm/pstrmOutput_v_glbv_V' to 'axis' (register, both mode).
INFO: [RTGEN 206-500] Setting interface mode on port 'fir_n11_strm/pstrmOutput_v_glbw_V' to 'axis' (register, both mode).
INFO: [RTGEN 206-500] Setting interface mode on port 'fir_n11_strm/pstrmOutput_v_id_V' to 'axis' (register, both mode).
INFO: [RTGEN 206-500] Setting interface mode on port 'fir_n11_strm/pstrmOutput_v_dest_V' to 'axis' (register, both mode).
INFO: [RTGEN 206-500] Setting interface mode on port 'fir_n11_strm/an32Conf' to 's_axilite & ap_memory'.
INFO: [RTGEN 206-500] Setting interface mode on port 'fir_n11_strm/regXferLang' to 's_axilite & ap_none'.
INFO: [RTGEN 206-500] Setting interface mode on function 'fir_n11_strm' to 's_axilite & ap_ctrl_hs'.
INFO: [RTGEN 206-100] Bundling port 'regXferLang' 'an32Conf' and 'return' to AXI-Lite port control.
INFO: [RTGEN 206-100] Finished creating RTL model for 'fir_n11_strm'.
INFO: [HLS 200-111] Finished Creating RTL model: CPU user time: 0.37 seconds. CPU system time: 0 seconds. Elapsed time: 0.42 seconds; current allocated memory: 524.000 MB.
INFO: [HLS 200-111] Finished Generating all RTL models: CPU user time: 0.34 seconds. CPU system time: 0 seconds. Elapsed time: 0.36 seconds; current allocated memory: 527.742 MB.
INFO: [HLS 200-111] Finished Updating report files: CPU user time: 0.38 seconds. CPU system time: 0 seconds. Elapsed time: 0.39 seconds; current allocated memory: 534.426 MB.
INFO: [VHDL 208-304] Generating VHDL RTL for fir_n11_strm.
INFO: [VHDL 208-304] Generating VHDL RTL for fir_n11_strm.
INFO: [HLS 200-780] **** Loop Constraint Status: All loop constraints were NOT satisfied.
INFO: [HLS 200-780] **** Estimated Fmax: 158.98 Mb
INFO: [HLS 200-111] Finished Command csynth_design CPU user time: 8.46 seconds. CPU system time: 1.84 seconds. Elapsed time: 13.16 seconds; current allocated memory: -444.652 MB.
INFO: [HLS 200-112] Total CPU user time: 10.42 seconds. Total CPU system time: 4.97 seconds. Total elapsed time: 16.53 seconds; peak allocated memory: 979.273 MB.
Finished C synthesis.
```

Co-Simulation

Co-simulation Report for 'fir_n11_strm'

General Information

Date: Thu 05 Oct 2023 08:39:28 AM EDT
Version: 2022.1 (Build 3526262 on Mon Apr 18 15:47:01 MDT 2022)
Project: lab2_Stream
Status: Pass

Cosim Options

Tool: Vivado XSIM
Dump Trace: all
RTL: Verilog

Performance Estimates

Modules & Loops	Avg II	Max II	Min II	Avg Latency	Max Latency	Min Latency
↳ fir_n11_strm	6603	6603	6603	-	-	-
↳ fir_n11_strm_Pipeline_XFER_LOOP	6600	6600	6600	-	-	-
↳ XFER_LOOP	6601	6601	6601	-	-	-

Console

```
// ...
// Intra-Transaction Progress: Measured Latency / Latency Estimation * 100%
// ...
// RTL Simulation : "Inter-Transaction Progress" [*Intra-Transaction Progress*] @ "Simulation Time"
// ...
// RTL Simulation : 0 / 1 [ns] @ *125000*
// RTL Simulation : 1 / 1 [ns] @ *6785000*
// ...
// finish called at time : 67915 ns : File '/home/ubuntu/lab/course-lab_2/lab2_Stream/solution1/sim/verilog/fir_n11_strm.autob.v' Line 458
## quit
INFO: [Common 17-206] Exiting xsim at Thu Oct 5 08:39:27 2023...
INFO: [COSIM 212-916] Starting C post checking ...
>> Start test!
>> Comparing against output data...
>> Test passed!
...
INFO: [COSIM 212-1000] *** C/RTL co-simulation finished: PASS ***
INFO: [COSIM 212-1000] *** Transaction progress is measurable only when transaction number is greater than 1 in RTL simulation. Otherwise, they will be marked as all NA. If user wants to calculate them, please make sure there are a
INFO: [HLS 200-111] Finished Command cosim_design CPU user time: 23.52 seconds. CPU system time: 6.23 seconds. Elapsed time: 31.57 seconds; current allocated memory: 9.879 MB.
INFO: [HLS 200-112] Total CPU user time: 25.7 seconds. Total CPU system time: 8.98 seconds. Total elapsed time: 34.63 seconds; peak allocated memory: 472.430 MB.
Finished C/RTL co-simulation.
```

csynth.rpt

+ Performance & Resource Estimates:												
PS: '+' for module; 'o' for loop; '*' for dataflow +-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+ Modules Issue Latency Latency Iteration Trip & Loops Type (cycles) (ns) Latency Interval Count Pipelined BRAM DSP FF LUT URAM +-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+												
+ fir_n11_strm	- 1.01 - - - - - no - 33 (2%) 952 (~0%) 1082 (~0%) -											
+ fir_n11_strm_Pipeline_XFER_LOOP	- 1.01 - - - - - no - 33 (2%) 762 (~0%) 825 (~0%) -											
+ o XFER_LOOP	II 7.30 - - 12 11 - yes - - - - - -											

```
fir_n11_strm_csynth.rpt

= Performance Estimates

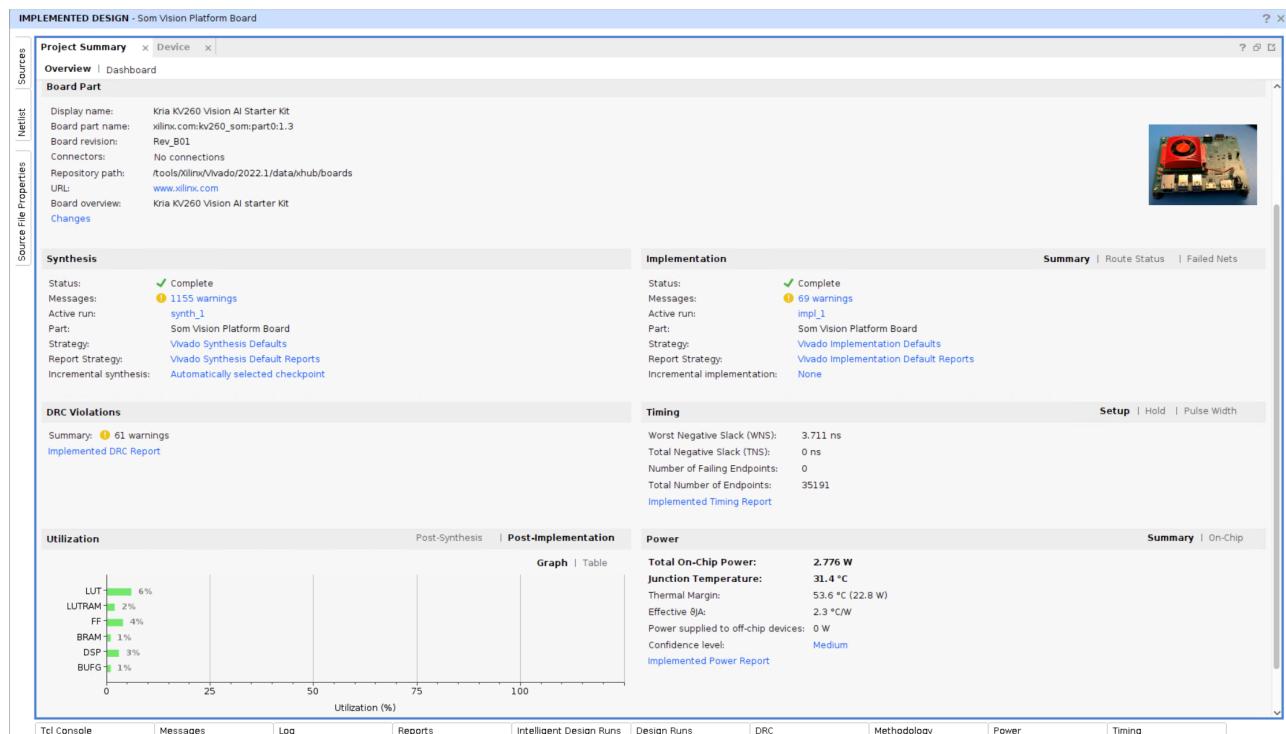
+ Timing:
  * Summary:
    +-----+-----+-----+-----+
    | Clock | Target | Estimated| Uncertainty|
    +-----+-----+-----+-----+
    | ap_clk | 10.00 ns| 6.290 ns| 2.70 ns|
    +-----+-----+-----+-----+

+ Latency:
  * Summary:
    +-----+-----+-----+-----+-----+-----+
    | Latency (cycles) | Latency (absolute) | Interval | Pipeline|
    | min | max | min | max | min | max | Type |
    +-----+-----+-----+-----+-----+-----+
    | ? | ? | ? | ? | ? | no |
    +-----+-----+-----+-----+-----+-----+

+ Detail:
  * Instance:
    +-----+-----+-----+-----+-----+-----+-----+-----+
    | | | | Latency (cycles) | Latency (absolute) | Interval | Pipeline| |
    | | | | min | max | min | max | Type |
    | | Instance | Module | ? | ? | ? | ? | no |
    +-----+-----+-----+-----+-----+-----+-----+
    | grp_fir_n11_strm_Pipeline_XFER_LOOP_fu_112 | fir_n11_strm_Pipeline_XFER_LOOP | ? | ? | ? | ? | no |
    +-----+-----+-----+-----+-----+-----+-----+-----+

  * Loop:
  N/A
```

- Utilization



- Interface

csynth.rpt

= HW Interfaces											
* S_AXILITE Interfaces											
+-----+-----+-----+-----+-----+											
Interface	Data Width	Address Width	Offset	Register							
+-----+-----+-----+-----+-----+											
s_axi_control 32 7 64 0											
+-----+-----+-----+-----+-----+											
* S_AXILITE Registers											
+-----+-----+-----+-----+-----+-----+-----+											
Interface	Register	Offset	Width	Access	Description	Bit Fields					
+-----+-----+-----+-----+-----+-----+-----+											
s_axi_control CTRL 0x00 32 RW Control signals 0=AP_START 1=AP_DONE 2=AP_IDLE 3=AP_READY 7=AUTO_RESTART 9=INTERRUPT											
s_axi_control GIER 0x04 32 RW Global Interrupt Enable Register 0=Enable											
s_axi_control IP_IER 0x08 32 RW IP Interrupt Enable Register 0=CHAN0_INT_EN 1=CHAN1_INT_EN											
s_axi_control IP_ISR 0x0C 32 RW IP Interrupt Status Register 0=CHAN0_INT_ST 1=CHAN1_INT_ST											
s_axi_control regXferleng 0x10 32 W Data signal of regXferleng											
+-----+-----+-----+-----+-----+-----+-----+											
* AXIS											
+-----+-----+-----+-----+-----+-----+-----+											
Interface	Register Mode	TDATA	TDEST	TID	TKEEP	TLAST TREADY TSTRB TUSER TVALID					
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+											
pstrmInput both 32 1 1 4 1 1 4 1 1											
pstrmOutput both 32 1 1 4 1 1 4 1 1											
+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+-----+											
* TOP LEVEL CONTROL											
+-----+-----+-----+											
Interface	Type	Ports									
+-----+-----+-----+											
ap_clk clock ap_clk											
ap_rst_n reset ap_rst_n											
interrupt interrupt interrupt											
ap_ctrl ap_ctrl_hs											
+-----+-----+-----+											

fir_n11_maxi_csynth.rpt

= Interface

* Summary:

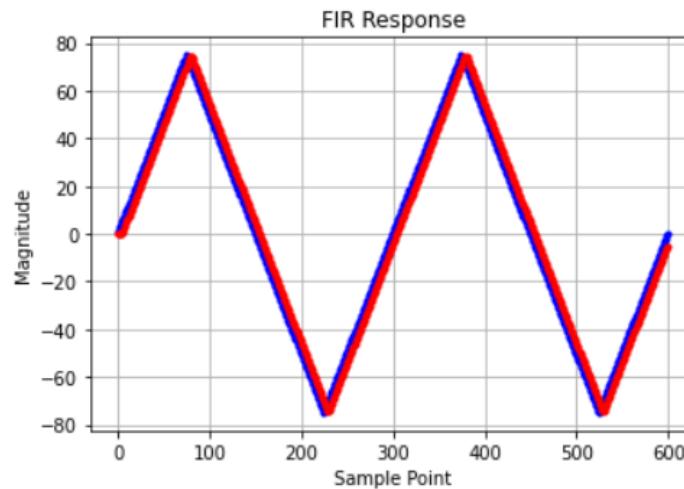
RTL Ports	Dir	Bits	Protocol	Source Object	C Type
s_axi_control_AWVALID	in	1	s_axi	control	array
s_axi_control_AWREADY	out	1	s_axi	control	array
s_axi_control_AWADDR	in	7	s_axi	control	array
s_axi_control_WVALID	in	1	s_axi	control	array
s_axi_control_WREADY	out	1	s_axi	control	array
s_axi_control_WDATA	in	32	s_axi	control	array
s_axi_control_WSTRB	in	4	s_axi	control	array
s_axi_control_ARVALID	in	1	s_axi	control	array
s_axi_control_ARREADY	out	1	s_axi	control	array
s_axi_control_ARADDR	in	7	s_axi	control	array
s_axi_control_RVALID	out	1	s_axi	control	array
s_axi_control_RREADY	in	1	s_axi	control	array
s_axi_control_RDATA	out	32	s_axi	control	array
s_axi_control_RRESP	out	2	s_axi	control	array
s_axi_control_BVALID	out	1	s_axi	control	array
s_axi_control_BREADY	in	1	s_axi	control	array
s_axi_control_BRESP	out	2	s_axi	control	array
ap_clk	in	1	ap_ctrl_hs	fir_n11_strm	return value
ap_rst_n	in	1	ap_ctrl_hs	fir_n11_strm	return value
interrupt	out	1	ap_ctrl_hs	fir_n11_strm	return value
pstrmInput_TDATA	in	32	axis	pstrmInput_V_data_V	pointer
pstrmInput_TVALID	in	1	axis	pstrmInput_V_dest_V	pointer
pstrmInput_TREADY	out	1	axis	pstrmInput_V_dest_V	pointer
pstrmInput_TDEST	in	1	axis	pstrmInput_V_dest_V	pointer
pstrmInput_TKEEP	in	4	axis	pstrmInput_V_keep_V	pointer
pstrmInput_TSTRB	in	4	axis	pstrmInput_V_strb_V	pointer
pstrmInput_TUSER	in	1	axis	pstrmInput_V_user_V	pointer
pstrmInput_TLAST	in	1	axis	pstrmInput_V_last_V	pointer
pstrmInput_TID	in	1	axis	pstrmInput_V_id_V	pointer
pstrmOutput_TDATA	out	32	axis	pstrmOutput_V_data_V	pointer
pstrmOutput_TVALID	out	1	axis	pstrmOutput_V_dest_V	pointer
pstrmOutput_TREADY	in	1	axis	pstrmOutput_V_dest_V	pointer
pstrmOutput_TDEST	out	1	axis	pstrmOutput_V_dest_V	pointer
pstrmOutput_TKEEP	out	4	axis	pstrmOutput_V_keep_V	pointer
pstrmOutput_TSTRB	out	4	axis	pstrmOutput_V_strb_V	pointer
pstrmOutput_TUSER	out	1	axis	pstrmOutput_V_user_V	pointer
pstrmOutput_TLAST	out	1	axis	pstrmOutput_V_last_V	pointer
pstrmOutput_TID	out	1	axis	pstrmOutput_V_id_V	pointer

- Co-simulation transcript/waveform

Latency(Clock Cycles)										Interval(Clock Cycles)			Total Execution Time		
RTL	Status	min	avg	max	min	avg	max	(Clock Cycles)							
VHDL	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA				
Verilog	Pass	6771	6771	6771	NA	NA	NA	NA	NA	NA	6771				

- Jupyter Notebook execution result

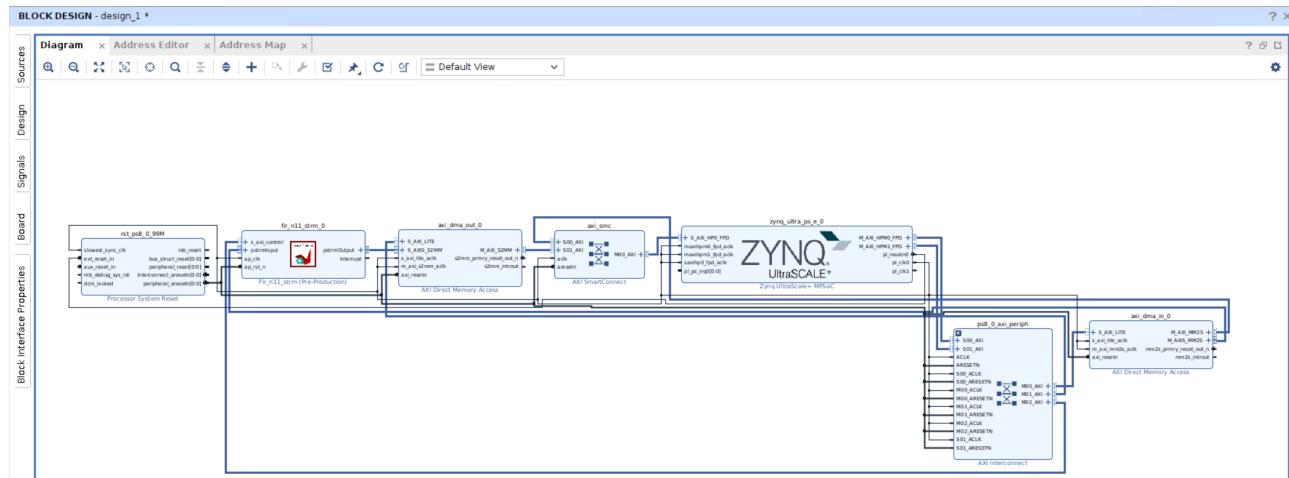
```
Entry: /usr/local/share/pynq-venv/lib/python3.8/site-packages/ipykernel_launcher.py
System argument(s): 3
Start of "/usr/local/share/pynq-venv/lib/python3.8/site-packages/ipykernel_launcher.py"
Kernel execution time: 0.0008745193481445312 s
```



```
=====
Exit process
```

[FIRN11Stream] Screen dump (Other)

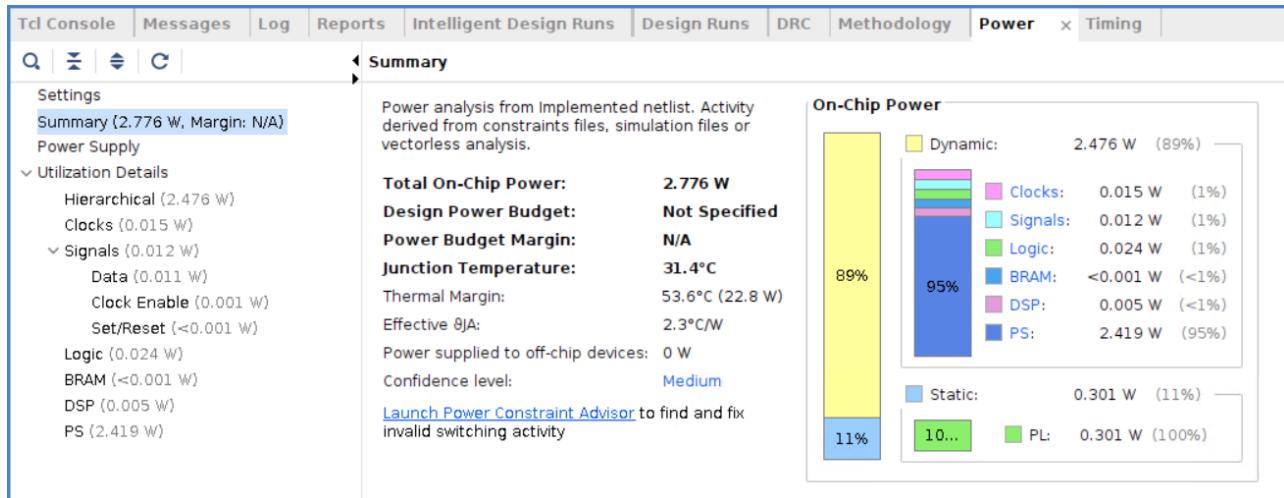
- Block Design



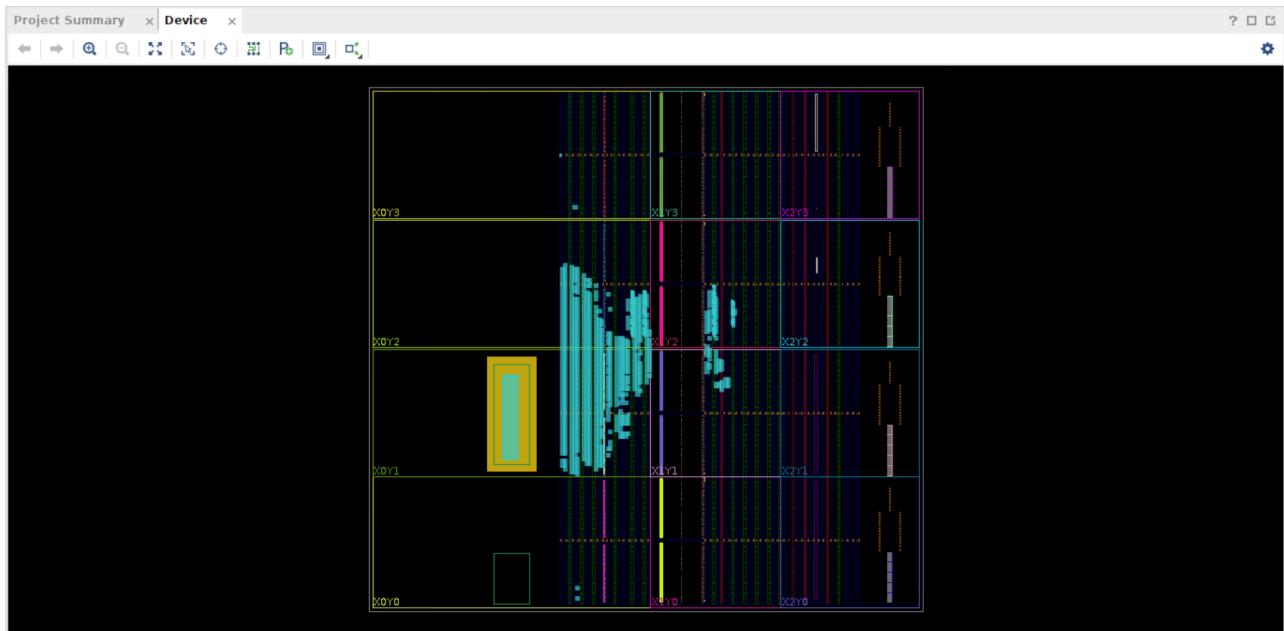
- Memory map

Address Editor						
Name	Interface	Slave Segment	Master Base Address	Range	Master High Address	
Network 0						
/axi_dma_in_0						
/zynq_ultra_ps_e_0/SAXIGP2	S_AXI_HPO_FPD	HP0_DDR_LOW	0x0000_0000	2G	0x7FFF_FFFF	
/zynq_ultra_ps_e_0/SAXIGP2	S_AXI_HPO_FPD	HP0_QSPI	0xC000_0000	512M	0xDFFF_FFFF	
Excluded (2)						
/zynq_ultra_ps_e_0/SAXIGP2	S_AXI_HPO_FPD	HP0_DDR_HIGH				
/zynq_ultra_ps_e_0/SAXIGP2	S_AXI_HPO_FPD	HP0_LPS_OCM	0xFF00_0000	16M	0xFFFF_FFFF	
/axi_dma_out_0						
/axi_dma_out_0/Data_S2MM						
/zynq_ultra_ps_e_0/SAXIGP2	S_AXI_HPO_FPD	HP0_DDR_LOW	0x0000_0000	2G	0x7FFF_FFFF	
/zynq_ultra_ps_e_0/SAXIGP2	S_AXI_HPO_FPD	HP0_QSPI	0xC000_0000	512M	0xDFFF_FFFF	
Excluded (2)						
/zynq_ultra_ps_e_0/SAXIGP2	S_AXI_HPO_FPD	HP0_DDR_HIGH				
/zynq_ultra_ps_e_0/SAXIGP2	S_AXI_HPO_FPD	HP0_LPS_OCM	0xFF00_0000	16M	0xFFFF_FFFF	
Network 1						
/zynq_ultra_ps_e_0						
/zynq_ultra_ps_e_0/Data						
/zynq_ultra_ps_e_0/S_AXI_LITE	S_AXI_LITE	Reg	0x00_A000_0000	64K	0x00_A000_FFFF	
/zynq_ultra_ps_e_0/S_AXI_LITE	S_AXI_LITE	Reg	0x00_A001_0000	64K	0x00_A001_FFFF	
/fir_n11_strm_0/s_axi_control	s_axi_control	Reg	0x00_A002_0000	64K	0x00_A002_FFFF	

- Power



- Implement Design



 Note

名詞解釋

- **ap_ctrl_chain**: dataflow pipelining
 - 允許多個功能在硬體中同時進行，以實現高效率的資料流處理
- **ap_ctrl_hs**: 要做 Co-Simulation top module 的 block level protocol 必須是 "hand-shake"
 - 一種機制，由 host function 去 start kernel function
- **ap_ctrl_none**: kernel啟動為 "data-driven"
 - 不需要 host trigger，只要有 data buffer 就會自動開始

觀念補充

1. Co-Simulation 的 **depth** 是模擬器參數，需要被明確指定。選擇一個過小或不指定 depth 可能會導致模擬不正確。
 - 值得注意的是，**depth** 並不直接代表硬體的buffer，而是與模擬器的操作有關
 - **FIFO depth** 要足夠容納所有要測試的 data 量

Provide sufficient FIFO depth to avoid stall or deadlock

 - • Depth declared for the interface is too small. Create Deadlock
2. 選擇適當演算法，能減省 hardware resource

Troubleshooting

- 實驗過程中，設定 **depth** 非600(設定128)，會在 Co-Simulation 時產生錯誤，如附圖所示：

```
>> Start test!
ERROR: System received a signal named SIGSEGV and the program has to stop immediately!
This signal was generated when a program tries to read or write outside the memory that is allocated for it, or to write memory that can only be read.
Possible cause of this problem may be: 1) the depth setting of pointer type argument is much larger than it needed; 2)insufficient depth of array argument; 3)null pointer etc.
Current execution stopped during CodeState = DELETE_CHAR_BUFFERS.
You can search CodeState variable name in apath*.cpp file under ./sim/wrapc dir to locate the position.

ERROR: [COSIM 212-360] Aborting co-simulation: C TB simulation failed.
ERROR: [COSIM 212-320] C TB testing failed, stop generating test vectors. Please check C TB or re-run cosim.
ERROR: [COSIM 212-5] *** C/RTL co-simulation file generation failed. ***
ERROR: [COSIM 212-4] *** C/RTL co-simulation finished: FAIL ***
INFO: [HLS 200-111] Finished Command cosim_design CPU user time: 6.87 seconds. CPU system time: 1.74 seconds. Elapsed time: 8.79 seconds; current allocated memory: 9.398 MB.
command 'ap_source' returned error code
while executing
"source /home/ubuntu/lab/course-lab_2/lab2-axi/lab2-AXI/solution1/cosim.tcl"
invoked from within
"hs::main /home/ubuntu/lab/course-lab_2/lab2-axi/lab2-AXI/solution1/cosim.tcl"
("uplevel" body line 1)
invoked from within
"uplevel 1 hs::main {*}$newargs"
(procedure "hs_proc" line 16)
invoked from within
```



後續更多資訊會補充於以下HackMD

- <https://hackmd.io/@Sheng08/HkzeBuDyp>



- []