TPS7A470x 36V，1A，4μV$_{RMS}$，射频 (RF) 低压降 (LDO) 电压稳压器

1 特性

- 输入电压范围：+3V 至 +36V
- 输出电压噪声：
  4μV$_{RMS}$(10Hz，100Hz)
- 电源纹波抑制：
  - 82dB (100Hz)
  - ≥ 55dB (10Hz，10MHz)
- 两个输出电压模式：
  - ANY-OUT™ 版本（借助印刷电路板 (PCB) 布局布线的用户可调输出）：
    - 无需外部反馈电阻器或者前馈电容器
    - 输出电压范围：+1.4V 至 +20.5V
  - 可调版本（仅适用于 TPS7A4701）：
    - 输出电压范围：+1.4V 至 +34V
- 输出电流：1A
- 压降电压：1A 时为 307mV
- 与 CMOS 逻辑电平兼容的启用引脚
- 内置固定电流限制和
  热关断
- 采用高性能散热封装：5mm × 5mm 四方扁平无引线 (QFN)
- 工作温度范围：
  –40°C 至 125°C

2 应用

- 压控振荡器 (VCO)
- 频率合成器
- 测试和测量
- 仪器仪表、医疗和音频
- RX，TX，和 PA 电路
- 用于运算放大器，
  数模转换器 (DAC)，模数转换器 (ADC)，和其它高精度模拟电路的电源轨
- 后置 DC/DC 转换器稳压和
  纹波滤除
- 基站和电信基础设施
- +12V 和 +24V 工业用总线

3 说明

TPS7A47 是一款正电压 (+36V) 超低噪声 (4μV$_{RMS}$) 低压降线性稳压器 (LDO) 系列产品，能够提供 1A 负载。

用户可通过印刷电路板 (PCB) 布局布线来编程设定 TPS7A4700 输出电压（最高 20.5V），无需外部电阻器或前馈电容器，从而减少了元件总数量。

配置 TPS7A4701 输出电压时，用户可通过 PCB 布局编程设定（高达 20.5V）或使用外部反馈电阻器调节（高达 34V）。

TPS7A47 由双极型技术设计而成，主要用于高准确度、高精度仪器仪表应用。在此类应用中，规整的电压轨对于系统性能的最大化至关重要。 这种设计使其成为功率运算放大器，模数转换器(ADC)，数模转换器 (DAC) 及其它关键应用（诸如医疗、射频 (RF) 和测试测量应用）中高性能模拟电路的最佳选择。

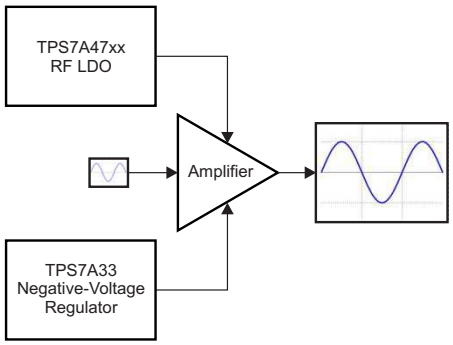
此外，TPS7A47 线性稳压器也非常适合于后置 DC/DC 转换器稳压。 通过滤除 dc/dc 开关转换所固有的输出电压纹波，可确保在灵敏仪器仪表、测试和测量、音频和 RF 应用中将系统性能最大化。

对于需要正向和负向低噪声电源轨的应用，请考虑 TI 的TPS7A33负向高电压、超低噪声线性稳压器系列产品。

器件信息(1)

部件号	封装	封装尺寸（标称值）
TPS7A470x	VQFN (20)	5mm x 5mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。



目录

4 修订历史记录

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (January 2014) to Revision F **Page**

- 已添加 *处理额定值表*、*特性描述*部分、*器件功能模式*、*应用和实施*部分、*电源相关建议*部分、*布局*部分、*器件和文档支持*部分以及*机械、封装和可订购信息*部分 ... 1
- 重新编写了*特性*列表中的第九个要点 ... 1
- Changed polarity of op amp shown on right side of the functional block diagram ... 12
- Reworded second paragraph in *Soft-Start And Inrush Current* section ... 13
- Revised *Capacitor Recommendations* section ... 16
- Changed paragraph 2 of *Dropout Voltage (V_{DO})* section for clarity ... 17
- Revised paragraph 1 of *Startup* section ... 17
- Rewrote paragraph 1 of *Power-Supply Rejection Ratio (PSRR)* section to eliminate confusion ... 18
- Changed paragraph 1 of *Power Supply Recommendations* section ... 20
- Changed paragraph 1 and paragraph 4 of *Power Dissipation (P_D)* section ... 20
- Revised paragraph 2 of *Layout Guidelines* section ... 21
- Changed second paragraph of *Thermal Protection* section ... 22

Changes from Revision D (December 2013) to Revision E **Page**

- 标题页的三个实例中输出电压噪声值从 4.17μV 改为 4μV ... 1
- 更改了*说明*部分中的第二段和第三段 ... 1
- Added "Thermal Pad" to pin configuration drawing ... 4
- Changed EN pin description ... 4
- Changed SENSE/FB pin to be for TPS7A4701 only ... 5
- Added new row to Pin Descriptions table for SENSE pin (for TPS7A4700 only) ... 5
- Added new row to Pin Descriptions table for thermal pad ... 5
- Added V_{REF} parameter ... 7
- Added TPS7A4701 device to test conditions for V_{NR} parameter ... 7

- Added Feedback Pin Current parameter to Electrical Characteristics 7
- Deleted Dropout Voltage vs Output Current graph 8
- Added EN pin to Functional Block Diagram 12
- Added sentence to ANY-OUT Programmable Output Voltage section to clarify ANY-OUT is for both devices 13
- Changed last two paragraphs of *Adjustable Operation* section 14
- Added "TPS7A4701 Only" to *Adjustable Operation* section title 14
- Deleted equation in Figure 23 14
- Changed Equation 3 14

Changes from Revision C (July 2013) to Revision D **Page**

- 将数据表状态从生产结构更改为生产数据 1
- 已将 TPS7A4701 静电放电 (ESD) 额定值从 > 1kV 更改为 2.5kV 1
- Changed noise reduction pin voltage parameter to show both devices 7
- Added text clarifying V_{REF} typical value to last paragraph on page 14

Changes from Revision B (April 2013) to Revision C **Page**

- 从数据表中删除了 TPS7A4702 预览器件 1

Changes from Revision A (July 2012) to Revision B **Page**

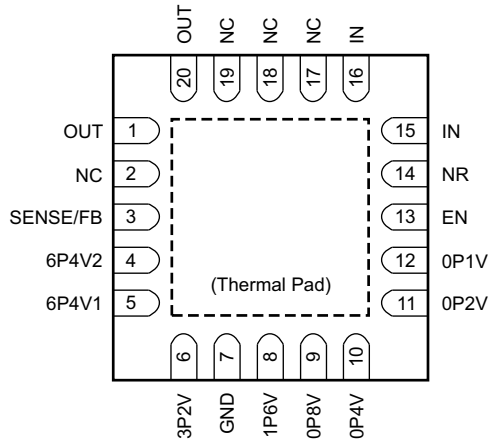
- 已将 TPS7A47 改为 TPS7A4700 1
- 已将 TPS7A4701 和 TPS7A4702 预览器件添加到数据表中 1
- 更改了标题页图表 1
- Added FB to SENSE pin to Functional Block Diagram 12
- Added new paragraph after Table 1 14
- Added new Table 2 14
- Added *Adjustable Operation* section 14

Changes from Original (June 2012) to Revision A **Page**

- 已移动到全生产数据（在整个文档中进行更改） 1

5 Pin Configuration and Functions

RGW Package
5-mm × 5-mm VQFN-20
(Top View)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
0P1V	12	I	When connected to GND, this pin adds 0.1 V to the nominal output voltage of the regulator. Do not connect any voltage other than GND to this pin. If not used, leave this pin floating.
0P2V	11	I	When connected to GND, this pin adds 0.2 V to the nominal output voltage of the regulator. Do not connect any voltage other than GND to this pin. If not used, leave this pin floating.
0P4V	10	I	When connected to GND, this pin adds 0.4 V to the nominal output voltage of the regulator. Do not connect any voltage other than GND to this pin. If not used, leave this pin floating.
0P8V	9	I	When connected to GND, this pin adds 0.8 V to the nominal output voltage of the regulator. Do not connect any voltage other than GND to this pin. If not used, leave this pin floating.
1P6V	8	I	When connected to GND, this pin adds 1.6 V to the nominal output voltage of the regulator. Do not connect any voltage other than GND to this pin. If not used, leave this pin floating.
3P2V	6	I	When connected to GND, this pin adds 3.2 V to the nominal output voltage of the regulator. Do not connect any voltage other than GND to this pin. If not used, leave this pin floating.
6P4V1	5	I	When connected to GND, this pin adds 6.4 V to the nominal output voltage of the regulator. Do not connect any voltage other than GND to this pin. If not used, leave this pin floating.
6P4V2	4	I	When connected to GND, this pin adds 6.4 V to the nominal output voltage of the regulator. Do not connect any voltage other than GND to this pin. If not used, leave this pin floating.
EN	13	I	Enable pin. The device is enabled when the voltage on this pin exceeds the maximum enable voltage, $V_{EN(HI)}$. If enable is not required, tie EN to IN.
GND	7	—	Ground
IN	15, 16	I	Input supply. A capacitor greater than or equal to 1 µF must be tied from this pin to ground to assure stability. A 10-µF capacitor is recommended to be connected from IN to GND (as close to the device as possible) to reduce circuit sensitivity to printed circuit board (PCB) layout, especially when long input traces or high source impedances are encountered.
NC	2, 17-19	—	This pin can be left open or tied to any voltage between GND and IN.
NR	14	—	Noise reduction pin. When a capacitor is connected from this pin to GND, RMS noise can be reduced to very low levels. A capacitor greater than or equal to 10 nF must be tied from this pin to ground to assure stability. A 1-µF capacitor is recommended to be connected from NR to GND (as close to the device as possible) to maximize ac performance and minimize noise.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
OUT	1, 20	O	Regulator output. A capacitor greater than or equal to 10 µF must be tied from this pin to ground to assure stability. A 47-µF ceramic output capacitor is highly recommended to be connected from OUT to GND (as close to the device as possible) to maximize ac performance.
SENSE/FB	3	I	Control-loop error amplifier input (TPS7A4701 only). This is the SENSE pin if the device output voltage is programmed using ANY-OUT (no external feedback resistors). This pin must be connected to OUT. Connect this pin to the point of load to maximize accuracy. This is the FB pin if the device output voltage is set using external resistors. See the *Adjustable Operation* section for more details.
SENSE	3	I	Control-loop error amplifier input (TPS7A4700 only). This is the SENSE pin of the device and must be connected to OUT. Connect this pin to the point of load to maximize accuracy.
Thermal Pad		—	Connect the thermal pad to a large-area ground plane. The thermal pad is internally connected to GND.

6 Specifications

6.1 Absolute Maximum Ratings

Over junction temperature range, unless otherwise noted.(1)

		MIN	MAX	UNIT
Voltage(2)	IN pin to GND pin	–0.4	+36	V
	EN pin to GND pin	–0.4	+36	V
	EN pin to IN pin	–36	+0.4	V
	OUT pin to GND pin	–0.4	+36	V
	NR pin to GND pin	–0.4	+36	V
	SENSE/FB pin to GND pin	–0.4	+36	V
	0P1V pin to GND pin	–0.4	+36	V
	0P2V pin to GND pin	–0.4	+36	V
	0P4V pin to GND pin	–0.4	+36	V
	0P8V pin to GND pin	–0.4	+36	V
	1P6V pin to GND pin	–0.4	+36	V
	3P2V pin to GND pin	–0.4	+36	V
	6P4V1 pin to GND pin	–0.4	+36	V
	6P4V2 pin to GND pin	–0.4	+36	V
Current	Peak output	Internally limited		
Temperature	Operating virtual junction, T_J	–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability..
(2) All voltages are with respect to network ground terminal.

6.2 Handling Ratings

				MIN	MAX	UNIT
T_{stg}	Storage temperature range			–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	TPS7A4700	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	–1000	1000	V
			Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	–500	500	
		TPS7A4701	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	–2500	2500	V
			Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	–500	500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over junction temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
V_I	3.0		35.0	V
V_O	1.4		34.0	V
V_{EN}	0		V_{IN}	V
I_O	0		1.0	A

6.4 Thermal Information

THERMAL METRIC(1)		TPS7A47xx RGW 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	27	
$R_{\theta JB}$	Junction-to-board thermal resistance	11.9	
ψ_{JT}	Junction-to-top characterization parameter	0.3	
ψ_{JB}	Junction-to-board characterization parameter	11.9	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.7	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

At –40°C ≤ T_J ≤ 125°C; $V_I = V_{O(nom)}$ + 1.0 V or V_I = 3.0 V (whichever is greater); $V_{EN} = V_I$; I_O = 0 mA; C_{IN} =10 µF; C_{OUT} = 10 µF; C_{NR} = 10 nF; SENSE/FB tied to OUT; and 0P1V, 0P2V, 0P4V, 0P8V, 1P6V, 3P2V, 6P4V1, 6P4V2 pins OPEN, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_I	Input voltage range			3		35	V
V_{UVLO}	Under-voltage lockout threshold	V_I rising			2.67		V
		V_I falling			2.5		V
$V_{(REF)}$	Reference voltage	$V_{(REF)} = V_{(FB)}$, TPS7A4701 only			1.4		V
$V_{UVLO(HYS)}$	Under-voltage lockout hysteresis				177		mV
V_{NR}	Noise reduction pin voltage	TPS7A4700, TPS7A4701 using ANY-OUT option			V_{OUT}		V
		TPS7A4701 in adjustable mode only			1.4		V
V_O	Output voltage range	$V_I \geq V_{O(nom)}$ + 1.0 V or 3 V (whichever is greater), C_{OUT} = 20 µF	TPS7A4700, TPS7A4701 using ANY-OUT option	1.4		20.5	V
			TPS7A4701 using adjustable option	1.4		34	V
	Nominal accuracy	T_J = 25°C, C_{OUT} = 20 µF		–1.0		1.0	$\%V_O$
	Overall accuracy	$V_{O(nom)}$ + 1.0 V ≤ V_I ≤ 35 V, 0 mA ≤ I_O ≤ 1 A, C_{OUT} = 20 µF		–2.5		2.5	$\%V_O$
$\Delta V_{O(\Delta VI)}$	Line regulation	$V_{O(nom)}$ + 1.0 V ≤ V_I ≤ 35 V			0.092		$\%V_O$
$\Delta V_{O(\Delta IO)}$	Load regulation	0 mA ≤ I_O ≤ 1 A			0.3		$\%V_O$
$V_{(DO)}$	Dropout voltage	V_I = 95% $V_{O(nom)}$, I_O = 0.5 A			216		mV
		V_I = 95% $V_{O(nom)}$, I_O = 1 A			307	450	mV
$I_{(CL)}$	Current limit	V_O = 90% $V_{O(nom)}$		1	1.26		A
$I_{(GND)}$	Ground pin current	I_O = 0 mA			0.58	1.0	mA
		I_O = 1 A			6.1		mA
$I_{(EN)}$	Enable pin current	$V_{EN} = V_I$			0.78	2	µA
		$V_I = V_{EN}$ = 35 V			0.81	2	µA
$I_{(SHDN)}$	Shutdown supply current	V_{EN} = 0.4 V			2.55	8	µA
		V_{EN} = 0.4 V, V_I = 35 V			3.04	60	µA
$V_{+EN(HI)}$	Enable high-level voltage			2.0		V_I	V
$V_{+EN(LO)}$	Enable low-level voltage			0.0		0.4	V
$I_{(FB)}$	Feedback pin current				350		nA
PSRR	Power-supply rejection ratio	V_I = 16 V, $V_{O(nom)}$ = 15 V, C_{OUT} = 50 µF, I_O = 500 mA, C_{NR} = 1 µF, f = 1 kHz			78		dB
V_n	Output noise voltage	V_I = 3 V, $V_{O(nom)}$ = 1.4 V, C_{OUT} = 50 µF, C_{NR} = 1 µF, BW = 10 Hz to 100 kHz			4.17		μV_{RMS}
		V_{IN} = 6 V, $V_{O(nom)}$ = 5 V, C_{OUT} = 50 µF, C_{NR} = 1 µF, BW = 10 Hz to 100 kHz			4.67		μV_{RMS}
T_{sd}	Thermal shutdown temperature	Shutdown, temperature increasing			170		°C
		Reset, temperature decreasing			150		°C
T_J	Operating junction temperature			–40		125	°C

6.6 Typical Characteristics

At –40°C ≤ T_J ≤ 125°C; V_I = $V_{O(nom)}$ + 1.0 V or V_I = 3.0 V (whichever is greater); V_{EN} = V_I; I_O = 0 mA; C_{IN} =10 µF; C_{OUT} = 10 µF; C_{NR} = 1 µF; SENSE/FB tied to OUT; and 0P1V, 0P2V, 0P4V, 0P8V, 1P6V, 3P2V, 6P4V1, 6P4V2 pins OPEN, unless otherwise noted.

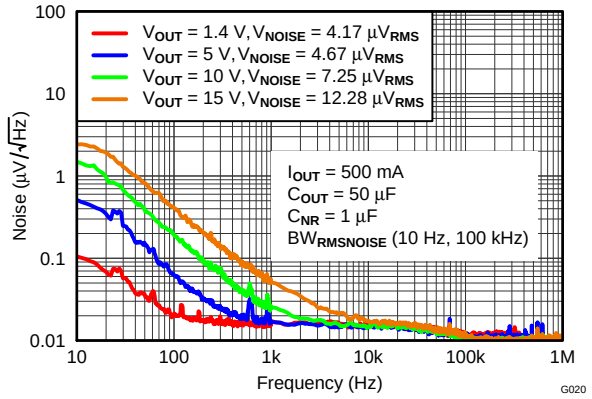


Figure 1. Noise vs Output Voltage

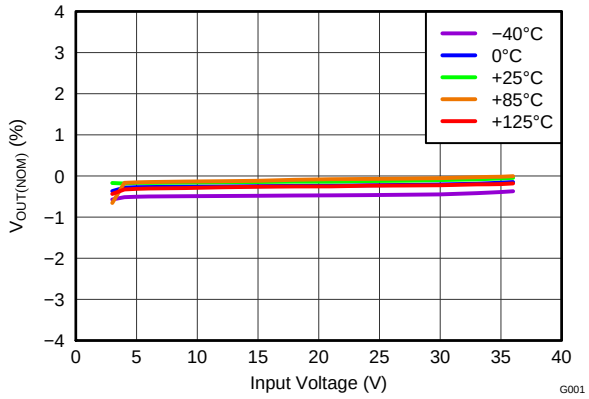


Figure 2. Line Regulation

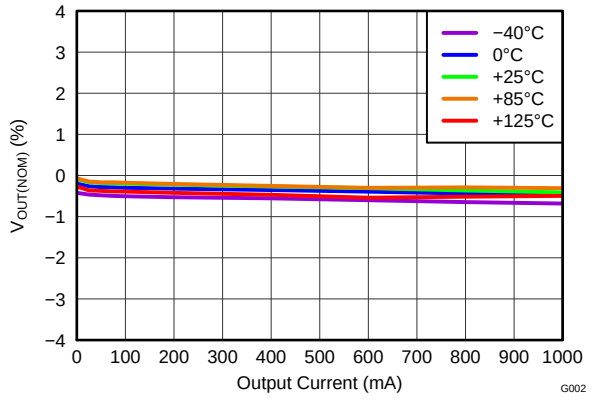


Figure 3. Load Regulation

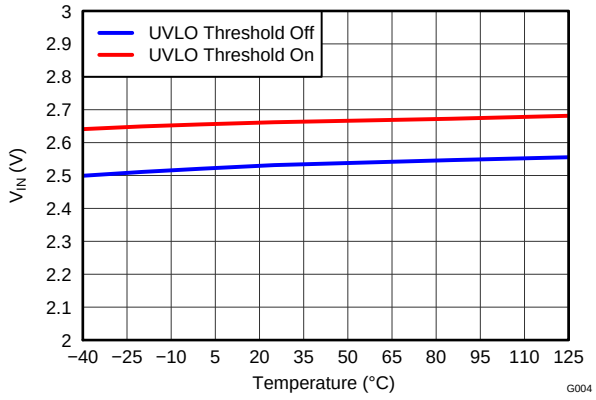


Figure 4. UVLO Threshold vs Temperature

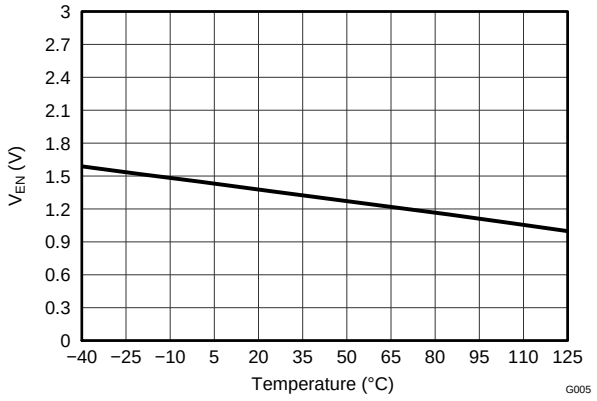


Figure 5. Enable Voltage Threshold vs Temperature

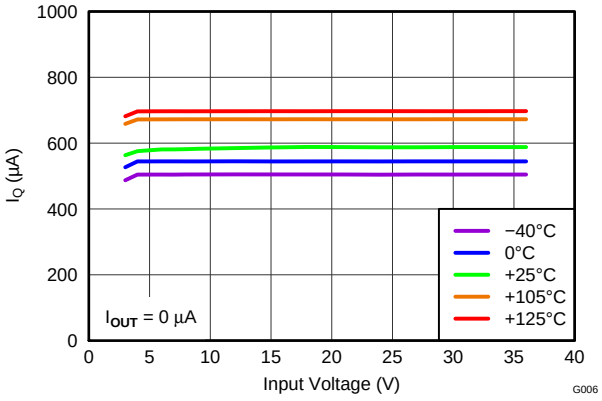


Figure 6. Quiescent Current vs Input Voltage

Typical Characteristics (continued)

At –40°C ≤ T_J ≤ 125°C; $V_I = V_{O(nom)}$ + 1.0 V or V_I = 3.0 V (whichever is greater); $V_{EN} = V_I$; I_O = 0 mA; C_{IN} =10 µF; C_{OUT} = 10 µF; C_{NR} = 1 µF; SENSE/FB tied to OUT; and 0P1V, 0P2V, 0P4V, 0P8V, 1P6V, 3P2V, 6P4V1, 6P4V2 pins OPEN, unless otherwise noted.

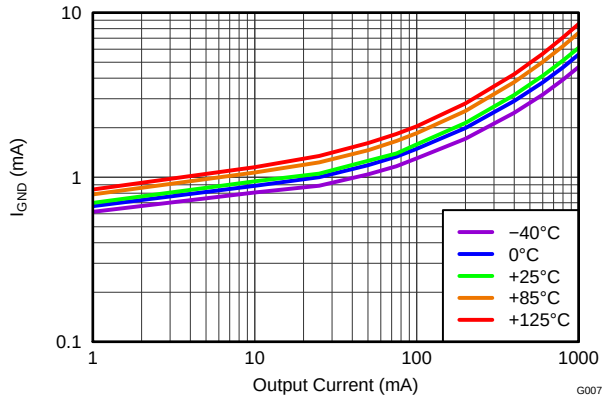


Figure 7. Ground Current vs Output Current

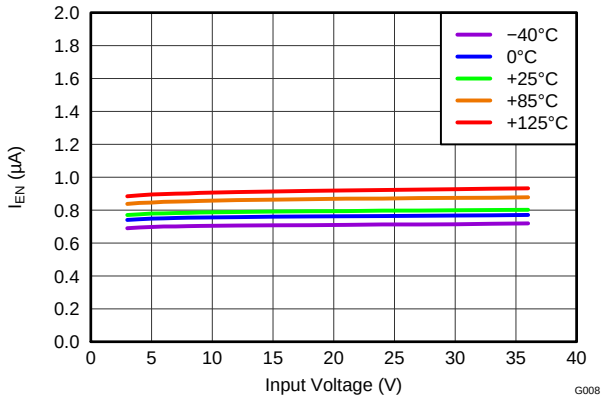


Figure 8. Enable Current vs Input Voltage

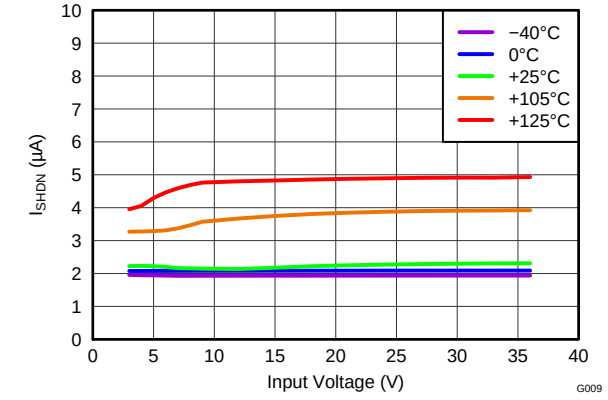


Figure 9. Shutdown Current vs Input Voltage

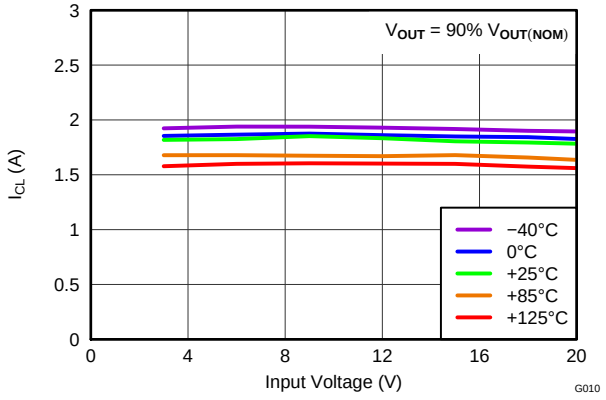


Figure 10. Current Limit vs Input Voltage

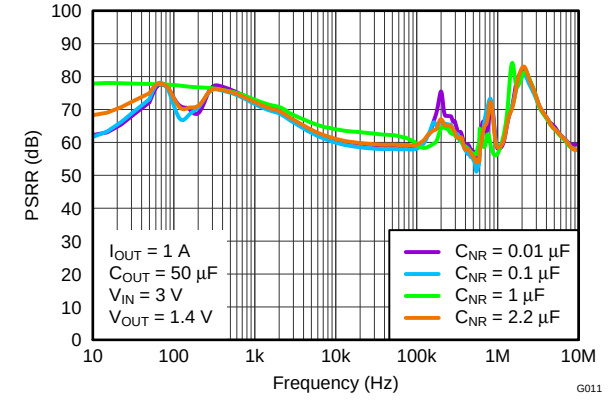


Figure 11. Power-Supply Rejection Ratio vs C_{NR}

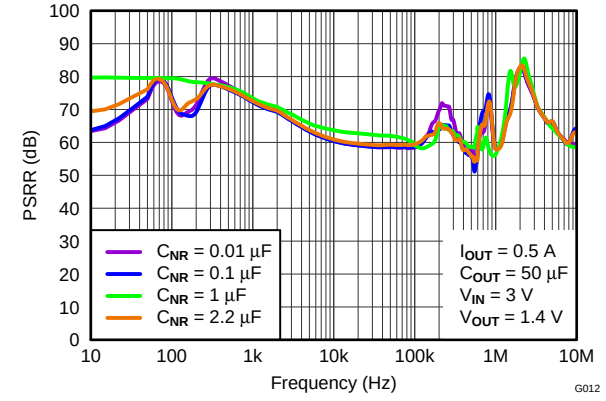


Figure 12. Power-Supply Rejection Ratio vs C_{NR}

Typical Characteristics (continued)

At –40°C ≤ T_J ≤ 125°C; V_I = $V_{O(nom)}$ + 1.0 V or V_I = 3.0 V (whichever is greater); V_{EN} = V_I; I_O = 0 mA; C_{IN} =10 µF; C_{OUT} = 10 µF; C_{NR} = 1 µF; SENSE/FB tied to OUT; and 0P1V, 0P2V, 0P4V, 0P8V, 1P6V, 3P2V, 6P4V1, 6P4V2 pins OPEN, unless otherwise noted.

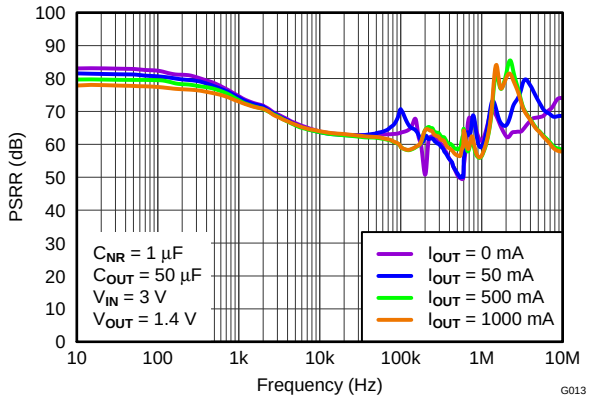


Figure 13. Power-Supply Rejection Ratio vs I_O

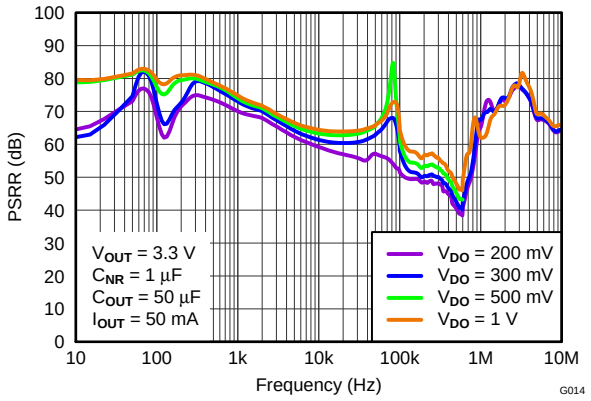


Figure 14. Power-Supply Rejection Ratio vs Dropout

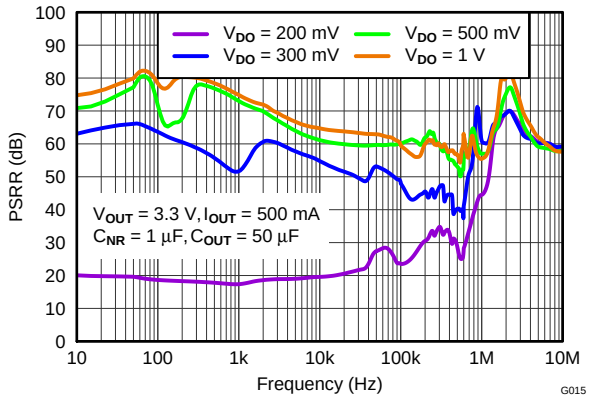


Figure 15. Power-Supply Rejection Ratio vs Dropout

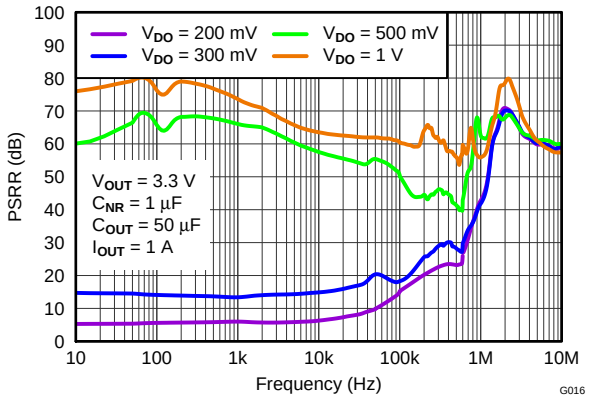


Figure 16. Power-Supply Rejection Ratio vs Dropout

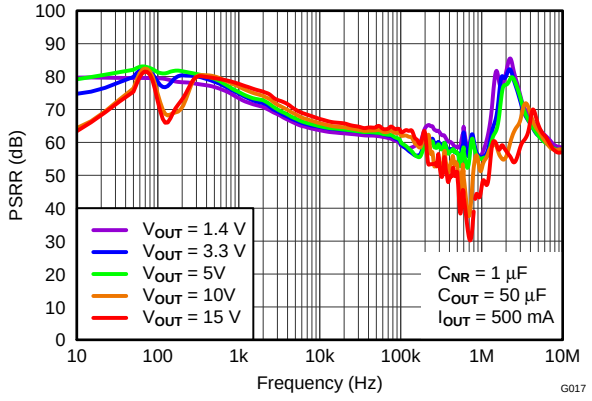


Figure 17. Power-Supply Rejection Ratio vs Output Voltage

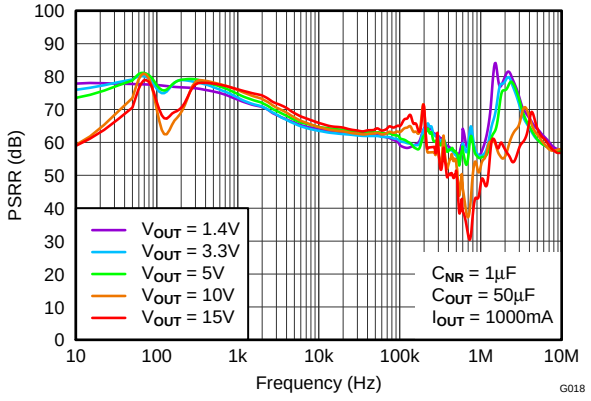


Figure 18. Power-Supply Rejection Ratio vs Output Voltage

Typical Characteristics (continued)

At –40°C ≤ T_J ≤ 125°C; V_I = $V_{O(nom)}$ + 1.0 V or V_I = 3.0 V (whichever is greater); V_{EN} = V_I; I_O = 0 mA; C_{IN} =10 µF; C_{OUT} = 10 µF; C_{NR} = 1 µF; SENSE/FB tied to OUT; and 0P1V, 0P2V, 0P4V, 0P8V, 1P6V, 3P2V, 6P4V1, 6P4V2 pins OPEN, unless otherwise noted.

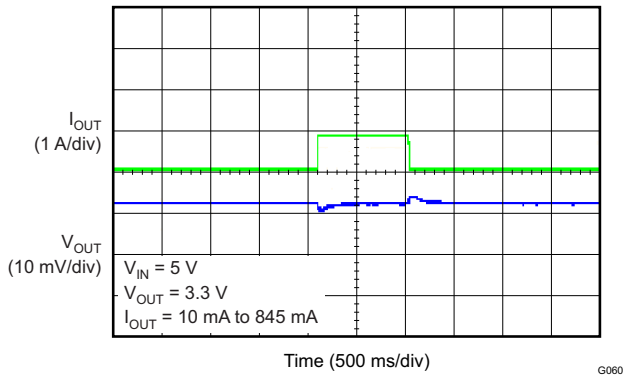


Figure 19. Load Transient

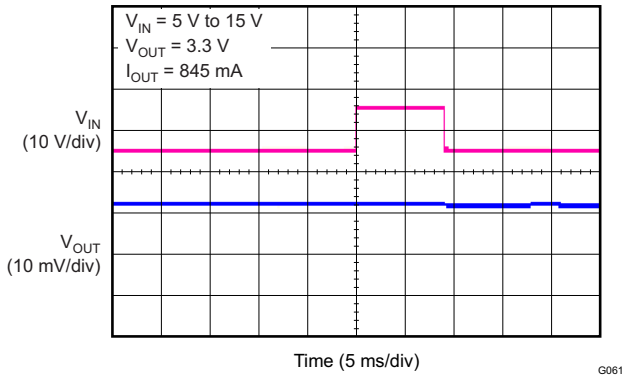


Figure 20. Line Transient

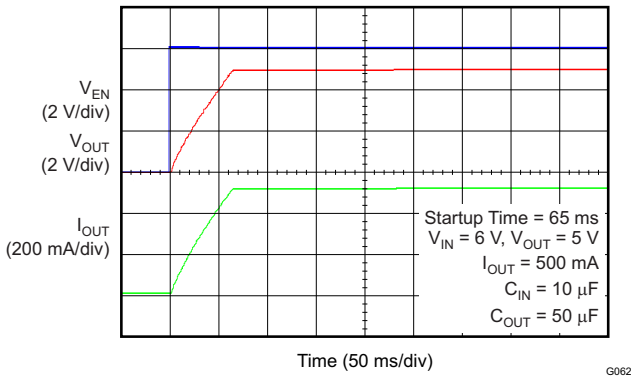


Figure 21. Startup

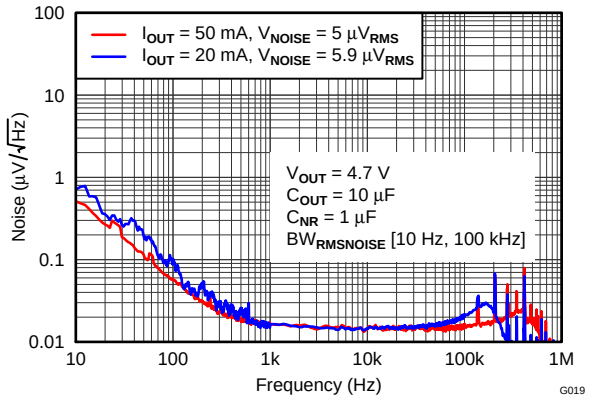


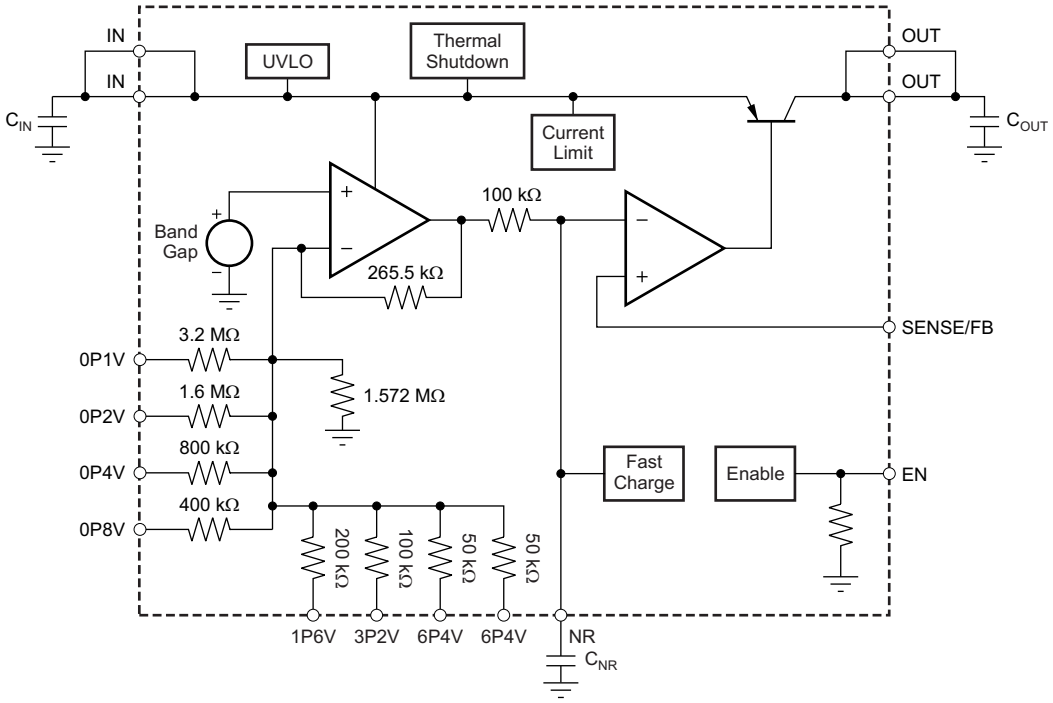
Figure 22. Noise vs Output Current

7 Detailed Description

7.1 Overview

The TPS7A4700 and TPS7A4701 (TPS7A470x) are positive voltage (+36 V), ultralow-noise (4 μV_{RMS}) LDOs capable of sourcing a 1-A load. The TPS7A470x is designed with bipolar technology primarily for high-accuracy, high-precision instrumentation applications where clean voltage rails are critical to maximize system performance. This feature makes the device ideal for powering operational amplifiers, analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and other high-performance analog circuitry.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Internal Current Limit (I_{CL})

The internal current limit circuit is used to protect the LDO against high-load current faults or shorting events. The LDO is not designed to operate at a steady-state current limit. During a current-limit event, the LDO sources constant current. Therefore, the output voltage falls while load impedance decreases. Note also that when a current limit occurs while the resulting output voltage is low, excessive power is dissipated across the LDO, which results in a thermal shutdown of the output.

7.3.2 Enable (EN) And Under-Voltage Lockout (UVLO)

The TPS7A470x only turns on when both EN and UVLO are above the respective voltage thresholds. The UVLO circuit monitors input voltage (V_I) to prevent device turn-on before V_I rises above the lockout voltage. The UVLO circuit also causes a shutdown when V_I falls below lockout. The EN signal allows independent logic-level turn-on and shutdown of the LDO when the input voltage is present. EN can be connected directly to V_I if independent turn-on is not needed.

Feature Description (continued)

7.3.3 Soft-Start And Inrush Current

Soft-start refers to the ramp-up characteristic of the output voltage during LDO turn-on after EN and UVLO have achieved threshold voltage. The noise reduction capacitor serves a dual purpose of both governing output noise reduction and programming the soft-start ramp during turn-on.

Inrush current is defined as the current through the LDO from IN to OUT during the time of the turn-on ramp up. Inrush current then consists primarily of the sum of load and charge current to the output capacitor. Inrush current can be estimated by Equation 1:

$$I_{OUT(t)} = \left[\frac{C_{OUT} \times dV_{OUT}(t)}{dt}\right] + \left[\frac{V_{OUT}(t)}{R_{LOAD}}\right] \quad (1)$$

where:

- $V_{OUT}(t)$ is the instantaneous output voltage of the turn-on ramp,
- $dV_{OUT}(t)/dt$ is the slope of the V_O ramp, and
- R_{LOAD} is the resistive load impedance

7.4 Device Functional Modes

The TPS7A470x has the following functional modes:

1. **Enabled:** When EN goes above $V_{+EN(HI)}$, the device is enabled.
2. **Disabled:** When EN goes below $V_{+EN(LO)}$, the device is disabled. During this time, OUT is high impedance, and the current into IN does not exceed $I_{(SHDN)}$.

7.5 Programming

7.5.1 ANY-OUT Programmable Output Voltage

Both devices can be used in ANY-OUT mode. For ANY-OUT operation, the TPS7A4700 and TPS7A4701 do not use external resistors to set the output voltage, but use device pins 4, 5, 6, 8, 9, 10, 11, and 12 to program the regulated output voltage. Each pin is either connected to ground (active) or is left open (floating). The ANY-OUT programming is set by Equation 2 as the sum of the internal reference voltage ($V_{(REF)}$ = 1.4 V) plus the accumulated sum of the respective voltages assigned to each active pin; that is, 100 mV (pin 12), 200 mV (pin 11), 400 mV (pin 10), 800 mV (pin 9), 1.6 V (pin 8), 3.2 V (pin 6), 6.4 V (pin 5), or 6.4 V (pin 4). Table 1 summarizes these voltage values associated with each active pin setting for reference. By leaving all program pins open, or floating, the output is thereby programmed to the minimum possible output voltage equal to $V_{(REF)}$.

$$V_{OUT} = V_{REF} + (\Sigma \text{ ANY-OUT Pins to Ground}) \quad (2)$$

Table 1. ANY-OUT Programmable Output Voltage

ANY-OUT PROGRAM PINS (Active Low)	ADDITIVE OUTPUT VOLTAGE LEVEL
Pin 4 (6P4V2)	6.4 V
Pin 5 (6P4V1)	6.4 V
Pin 6 (3P2)	3.2 V
Pin 8 (1P6)	1.6 V
Pin 9 (0P8)	800 mV
Pin 10 (0P4)	400 mV
Pin 11 (0P2)	200 mV
Pin 12 (0P1)	100 mV

Table 2 shows a list of the most common output voltages and the corresponding pin settings. The voltage setting pins have a binary weight; therefore, the output voltage can be programmed to any value from 1.4 V to 20.5 V in 100-mV steps.

Table 2. Common Output Voltages and Corresponding Pin Settings

V_O (V)	PIN NAMES AND VOLTAGE PER PIN							
	0P1V 100 mV	0P2V 200 mV	0P4V 400 mV	0P8V 800 mV	1P6V 1.6 V	3P2V 3.2 V	6P4V1 6.4 V	6P4V2 6.4 V
1.4	Open	Open	Open	Open	Open	Open	Open	Open
1.5	GND	Open	Open	Open	Open	Open	Open	Open
1.8	Open	Open	GND	Open	Open	Open	Open	Open
2.5	GND	GND	Open	GND	Open	Open	Open	Open
3	Open	Open	Open	Open	GND	Open	Open	Open
3.3	GND	GND	Open	Open	GND	Open	Open	Open
4.5	GND	GND	GND	GND	GND	Open	Open	Open
5	Open	Open	GND	Open	Open	GND	Open	Open
10	Open	GND	GND	Open	GND	Open	GND	Open
12	Open	GND	Open	GND	Open	GND	GND	Open
15	Open	Open	Open	GND	Open	Open	GND	GND
18	Open	GND	GND	Open	Open	GND	GND	GND
20.5	GND	GND	GND	GND	GND	GND	GND	GND

7.5.2 Adjustable Operation (TPS7A4701 Only)

The TPS7A4701 has an output voltage range of 1.4 V to 34 V. For adjustable operation, set the nominal output voltage of the device using two external resistors, as shown in Figure 23.

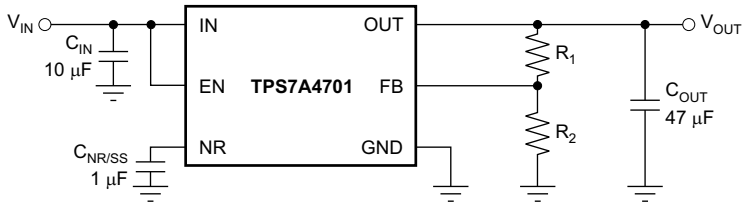


Figure 23. Adjustable Operation for Maximum AC Performance

R_1 and R_2 can be calculated for any output voltage within the operational range. The current through feedback resistor R_2 must be at least 5 µA to ensure stability. Additionally, the current into the FB pin ($I_{(FB)}$, typically 350 nA) creates an additional output voltage offset that depends on the resistance of R_1. For high-accuracy applications, select R_2 such that the current through R_2 is at least 35 µA to minimize any effects of $I_{(FB)}$ variation on the output voltage; 10 kΩ is recommended. R_1 can be calculated using Equation 3.

$$R_1 = \frac{V_{OUT} - V_{REF}}{I_{FB} + \frac{V_{REF}}{R_2}} \quad (3)$$

where

- V_{REF} = 1.4 V
- I_{FB} = 350 nA

Use 0.1% tolerance resistors to minimize the effects of resistor inaccuracy on the output voltage.

Table 3 shows the resistor combinations to achieve some standard rail voltages with commercially-available 1% tolerance resistors. The resulting output voltages yield a nominal error of < 0.5%.

Table 3. Suggested Resistors for Common Voltage Rails

V_{OUT}	R_1, Calculated	R_1, Closest 1% Value	R_2
1.4 V	0 Ω	0 Ω	∞
1.8 V	2.782 kΩ	2.8 kΩ	9.76 kΩ
3.3 V	13.213 kΩ	13.3 kΩ	9.76 kΩ
5 V	25.650 kΩ	25.5 kΩ	10 kΩ
12 V	77.032 kΩ	76.8 kΩ	10.2 kΩ
15 V	101.733 kΩ	102 kΩ	10.5 kΩ
18 V	118.276 kΩ	118 kΩ	10 kΩ
24 V	164.238 kΩ	165 kΩ	10.2 kΩ

To achieve higher nominal accuracy, two resistors can be used in the place of R_1. Select the two resistor values such that the sum results in a value as close as possible to the calculated R_1 value.

There are several alternative ways to set the output voltage. The program pins can be pulled low using external general-purpose input/output pins (GPIOs), or can be hardwired by the given layout of the printed circuit board (PCB) to set the ANY-OUT voltage. The TPS7A4701 evaluation module (EVM), available for purchase from the TI eStore, allows the output voltage to be programmed using jumpers.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS7A740x is a high-voltage, low-noise, 1-A LDO. Low-noise performance makes this LDO ideal for providing rail voltages to noise-sensitive loads, such as PLLs, oscillators, and high-speed ADCs.

8.2 Typical Application

Output voltage is set by grounding the appropriate control pins, as shown in Figure 24. When grounded, all control pins add a specific voltage on top of the internal reference voltage ($V_{(REF)}$ = 1.4 V). For example, when grounding pins 0P1V, 0P2V, and 1P6V, the voltage values 0.1 V, 0.2 V, and 1.6 V are added to the 1.4-V internal reference voltage for $V_{O(nom)}$ equal to 3.3 V, as described in the *Programming* section.

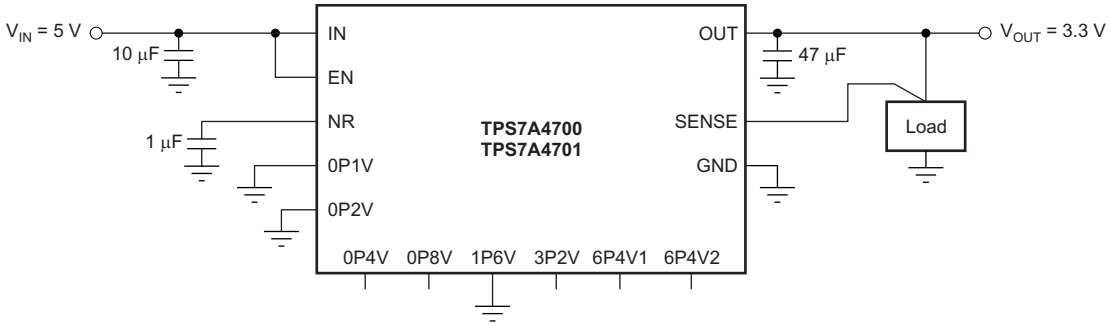


Figure 24. Typical Application, V_{OUT} = 3.3 V

8.2.1 Design Requirements

PARAMETER	DESIGN REQUIREMENT
Input Voltage	5.0 V, ±10%
Output Voltage	3.3 V, ±3%
Output Current	500 mA
Peak-to-Peak Noise, 10 Hz to 100 kHz	50 µVp-p

8.2.2 Detailed Design Procedure

8.2.2.1 Capacitor Recommendations

These LDOs are designed to be stable using low equivalent series resistance (ESR), ceramic capacitors at the input, output, and at the noise reduction pin (NR, pin 14). Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended here, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-, and COG-rated dielectric materials provide relatively good capacitive stability across temperature, but the use of Y5V-rated capacitors is discouraged precisely because the capacitance varies so widely. In all cases, ceramic capacitance varies a great deal with operating voltage and the design engineer must be aware of these characteristics. It is recommended to apply a 50% derating of the nominal capacitance in the design.

Attention must be given to the input capacitance to minimize transient input droop during load current steps because the TPS7A470x has a very fast load transient response. Large input capacitors are necessary for good transient load response, and have no detrimental influence on the stability of the device. Note, however, that using large ceramic input capacitances can also cause unwanted ringing at the output if the input capacitor, in combination with the wire lead inductance, creates a high-Q peaking effect during transients. For example, a 5-nH lead inductance and a 10-µF input capacitor form an LC filter with a resonance frequency of 712 kHz at the edge of the control loop bandwidth. Short, well-designed interconnect leads to the up-stream supply minimize this effect without adding damping. Damping of unwanted ringing can be accomplished by using a tantalum capacitor, with a few hundred milliohms of ESR, in parallel with the ceramic input capacitor.

8.2.2.1.1 Input and Output Capacitor Requirements

The TPS7A470x is designed and characterized for operation with ceramic capacitors of 10 µF or greater at the input and output. Optimal noise performance is characterized using a total output capacitor value of 50 µF. Note especially that input and output capacitances must be located as near as practical to the respective input and output pins.

8.2.2.1.2 Noise Reduction Capacitor (C_{NR})

The noise reduction capacitor, connected to the NR pin of the LDO, forms an RC filter for filtering out noise that might ordinarily be amplified by the control loop and appear on the output voltage. Larger capacitances, up to 1 µF, affect noise reduction at lower frequencies while also tending to further reduce noise at higher frequencies. Note that C_{NR} also serves a secondary purpose in programming the turn-on rise time of the output voltage and thereby controls the turn-on surge current.

8.2.2.2 Dropout Voltage (V_{DO})

Generally speaking, the dropout voltage often refers to the voltage difference between the input and output voltage ($V_{(DO)} = V_I – V_O$). However, in the *Electrical Characteristics* $V_{(DO)}$ is defined as the $V_I – V_O$ voltage at the rated current ($I_{(RATED)}$), where the main current pass-FET is fully on in the Ohmic region of operation and is characterized by the classic $R_{DS(on)}$ of the FET. $V_{(DO)}$ indirectly specifies a minimum input voltage above the nominal programmed output voltage at which the output voltage is expected to remain within its accuracy boundary. If the input falls below this $V_{(DO)}$ limit ($V_I < V_O + V_{(DO)}$), then the output voltage decreases in order to follow the input voltage.

Dropout voltage is always determined by the $R_{DS(on)}$ of the main pass-FET. Therefore, if the LDO operates below the rated current, the $V_{(DO)}$ is directly proportional to the output current and can be reduced by the same factor. The $R_{DS(on)}$ for the TPS7A470x can be calculated using Equation 4:

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \tag{4}$$

8.2.2.3 Output Voltage Accuracy

The output voltage accuracy specifies minimum and maximum output voltage error, relative to the expected nominal output voltage stated as a percent. This accuracy error typically includes the errors introduced by the internal reference and the load and line regulation across the full range of rated load and line operating conditions over temperature, unless otherwise specified by the *Electrical Characteristics*. Output voltage accuracy also accounts for all variations between manufacturing lots.

8.2.2.4 Startup

The startup time for the TPS7A470x depends on the output voltage and the capacitance of the C_{NR} capacitor. Equation 5 calculates the startup time for a typical device.

$$t_{SS} = 100{,}000 \bullet C_{NR} \bullet \ln\left(\frac{V_R + 5}{5}\right) \tag{5}$$

where

- C_{NR} = capacitance of the C_{NR} capacitor
- $V_R = V_O$ voltage if using the ANY-OUT configuration, or 1.4 V if using the adjustable configuration

8.2.2.5 AC Performance

AC performance of the LDO is typically understood to include power-supply rejection ratio, load step transient response, and output noise. These metrics are primarily a function of open-loop gain and bandwidth, phase margin, and reference noise.

8.2.2.5.1 Power-Supply Rejection Ratio (PSRR)

PSRR is a measure of how well the LDO control loop rejects ripple noise from the input source to make the dc output voltage as noise-free as possible across the frequency spectrum (usually 10 Hz to 10 MHz). Equation 6 gives the PSRR calculation as a function of frequency where input noise voltage [$V_{S(IN)}(f)$] and output noise voltage [$V_{S(OUT)}(f)$] are understood to be purely ac signals.

$$PSRR\ (dB) = 20\ Log_{10}\left(\frac{V_{S(IN)}(f)}{V_{S(OUT)}(f)}\right) \quad (6)$$

Noise that couples from the input to the internal reference voltage for the control loop is also a primary contributor to reduced PSRR magnitude and bandwidth. This reference noise is greatly filtered by the noise reduction capacitor at the NR pin of the LDO in combination with an internal filter resistor (R_{SS}) for optimal PSRR.

The LDO is often employed not only as a dc/dc regulator, but also to provide exceptionally clean power-supply voltages that are free of noise and ripple to power-sensitive system components. This usage is especially true for the TPS7A470x.

8.2.2.5.2 Load Step Transient Response

The load step transient response is the output voltage response by the LDO to a step change in load current whereby output voltage regulation is maintained. The worst-case response is characterized for a load step of 10 mA to 1 A (at 1 A per microsecond) and shows a classic, critically-damped response of a very stable system. The voltage response shows a small dip in the output voltage when charge is initially depleted from the output capacitor and then the output recovers as the control loop adjusts itself. The depth of the charge depletion immediately after the load step is directly proportional to the amount of output capacitance. However, to some extent, the speed of recovery is inversely proportional to that same output capacitance. In other words, larger output capacitances act to decrease any voltage dip or peak occurring during a load step but also decrease the control-loop bandwidth, thereby slowing response.

The worst-case, off-loading step characterization occurs when the current step transitions from 1 A to 0 mA. Initially, the LDO loop cannot respond fast enough to prevent a small increase in output voltage charge on the output capacitor. Because the LDO cannot sink charge current, the control loop must turn off the main pass-FET to wait for the charge to deplete, thus giving the off-load step its typical monotonic decay (which appears triangular in shape).

8.2.2.5.3 Noise

The TPS7A470x is designed, in particular, for system applications where minimizing noise on the power-supply rail is critical to system performance. This scenario is the case for phase-locked loop (PLL)-based clocking circuits for instance, where minimum phase noise is all important, or in-test and measurement systems where even small power-supply noise fluctuations can distort instantaneous measurement accuracy. Because the TPS7A470x is also designed for higher voltage industrial applications, the noise characteristic is well designed to minimize any increase as a function of the output voltage.

LDO noise is defined as the internally-generated intrinsic noise created by the semiconductor circuits alone. This noise is the sum of various types of noise (such as shot noise associated with current-through-pin junctions, thermal noise caused by thermal agitation of charge carriers, flicker or 1/f noise that is a property of resistors and dominates at lower frequencies as a function of 1/f, burst noise, and avalanche noise).

To calculate the LDO RMS output noise, a spectrum analyzer must first measure the spectral noise across the bandwidth of choice (typically 10 Hz to 100 kHz in units of $\mu V/\sqrt{Hz}$). The RMS noise is then calculated in the usual manner as the integrated square root of the squared spectral noise over the band, then averaged by the bandwidth.

8.2.3 Application Curves

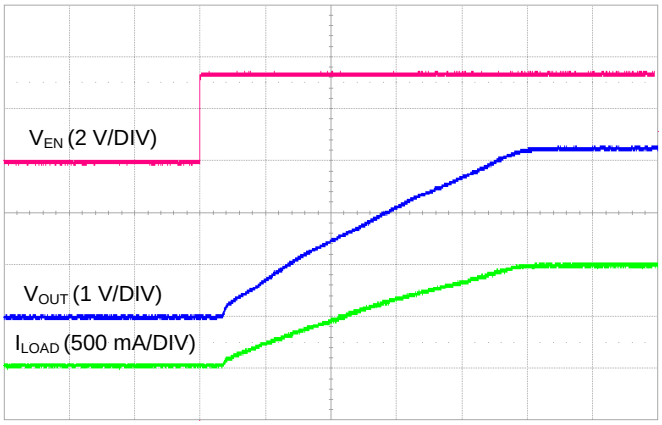


Figure 25. Startup with EN Pin rising (10 ms/DIV)

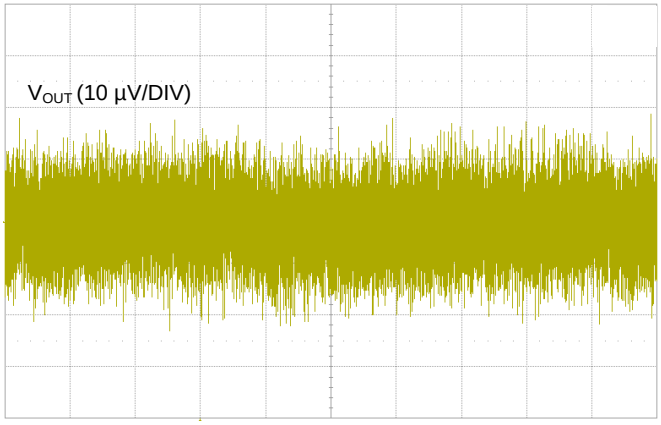


Figure 26. Output Noise Voltage, 10 Hz to 100 kHz (10 ms/DIV)

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range of 3 V to 35 V. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

9.1 Power Dissipation (P_D)

Power dissipation must be considered in the PCB design. In order to minimize risk of device operation above 125°C, use as much copper area as available for thermal dissipation. Do not locate other power-dissipating devices near the LDO.

Power dissipation in the regulator depends on the input to output voltage difference and load conditions. P_D can be calculated using Equation 7:

$$P_D = (V_{OUT} - V_{IN}) \times I_{OUT} \quad (7)$$

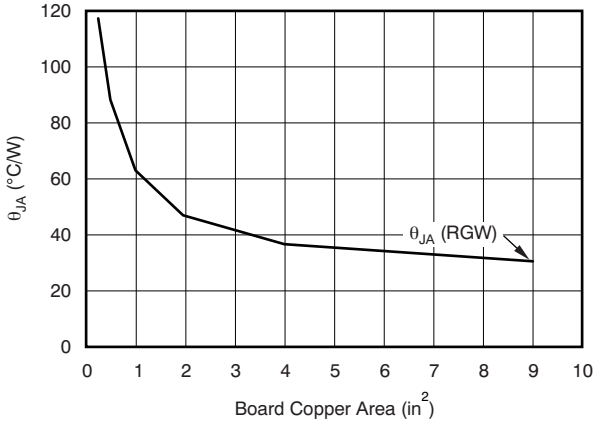
It is important to note that power dissipation can be minimized, and thus greater efficiency achieved, by proper selection of the system voltage rails. Proper selection allows the minimum input voltage necessary for output regulation to be obtained.

The primary heat conduction path for the QFN (RGW) package is through the thermal pad to the PCB. The thermal pad must be soldered to a copper pad area under the device. Thermal vias are recommended to improve the thermal conduction to other layers of the PCB.

The maximum power dissipation determines the maximum allowable junction temperature (T_J) for the device. Power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance (θ_{JA}) of the combined PCB and device package and the temperature of the ambient air (T_A), according to Equation 8.

$$T_J = T_A + (\theta_{JA} \times P_D) \quad (8)$$

Unfortunately, this thermal resistance (θ_{JA}) depends primarily on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the spreading planes. The θ_{JA} recorded in the *Thermal Information* table is determined by the JEDEC standard, PCB, and copper-spreading area and is to be used only as a relative measure of package thermal performance. Note that for a well-designed thermal layout, θ_{JA} is actually the sum of the QFN package junction-to-case (bottom) thermal resistance (θ_{JCbot}) plus the thermal resistance contribution by the PCB copper. By knowing θ_{JCbot}, the minimum amount of appropriate heat sinking can be used to estimate θ_{JA} with Figure 27. θ_{JCbot} can be found in the *Thermal Information* table.



NOTE: θ_{JA} value at a board size of 9-in^2 (that is, 3-in × 3-in) is a JEDEC standard.

Figure 27. Θ_{JA} vs Board Size

10 Layout

10.1 Layout Guidelines

For best overall performance, all circuit components are recommended to be located on the same side of the circuit board and as near as practical to the respective LDO pin connections. Ground return connections to the input and output capacitor, and to the LDO ground pin, must also be as close to each other as possible and connected by a wide, component-side, copper surface. The use of vias and long traces to create LDO circuit connections is strongly discouraged and negatively affects system performance. This grounding and layout scheme minimizes inductive parasitics and thereby reduces load-current transients, minimizes noise, and increases circuit stability.

A ground reference plane is also recommended. This reference plane serves to assure accuracy of the output voltage, shield noise, and behaves similar to a thermal plane to spread (or sink) heat from the LDO device when connected to the PowerPAD™. In most applications, this ground plane is necessary to meet thermal requirements.

Use the TPS7A4701 evaluation module (EVM), available for purchase from the TI eStore, as a reference for layout and application design.

10.2 Layout Example

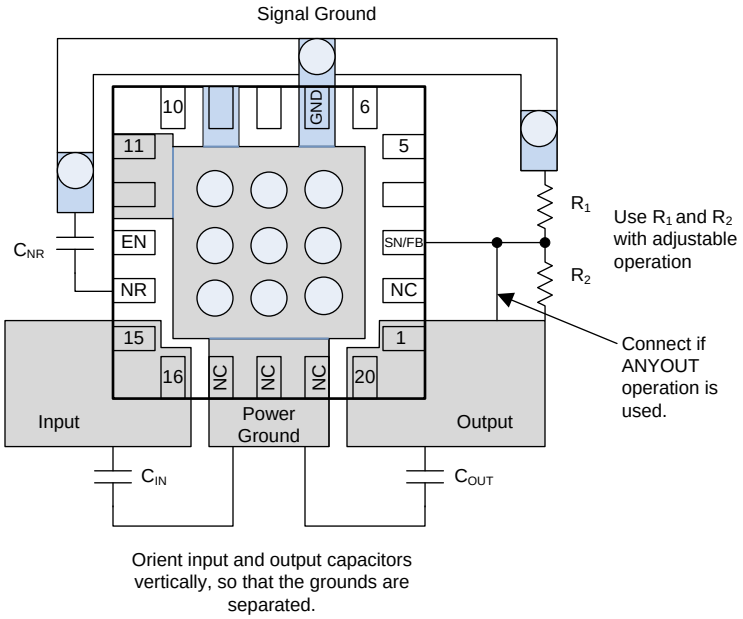


Figure 28. Layout Example

10.3 Thermal Protection

The TPS7A470x contains a thermal shutdown protection circuit to turn off the output current when excessive heat is dissipated in the LDO. Thermal shutdown occurs when the thermal junction temperature (T_J) of the main pass-FET exceeds 170°C (typical). Thermal shutdown hysteresis assures that the LDO again resets (turns on) when the temperature falls to 150°C (typical). Because the TPS7A470x is capable of supporting high input voltages, a great deal of power can be expected to be dissipated across the device at low output voltages, which causes a thermal shutdown. The thermal time-constant of the semiconductor die is fairly short, and thus the output oscillates on and off at a high rate when thermal shutdown is reached until power dissipation is reduced.

For reliable operation, the junction temperature must be limited to a maximum of 125°C. To estimate the thermal margin in a given layout, increase the ambient temperature until the thermal protection shutdown is triggered using worst-case load and highest input voltage conditions. For good reliability, thermal shutdown must be designed to occur at least 45°C above the maximum expected ambient temperature condition for the application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS7A470x is designed to protect against thermal overload conditions. The circuitry is not intended to replace proper heat sinking. Continuously running the TPS7A470x into thermal shutdown degrades device reliability.

10.4 Estimating Junction Temperature

JEDEC standards now recommend the use of PSI thermal metrics to estimate the junction temperatures of the LDO while in-circuit on a typical PCB board application. These metrics are not strictly speaking thermal resistances, but rather offer practical and relative means of estimating junction temperatures. These PSI metrics are determined to be significantly independent of copper-spreading area. The key thermal metrics (Ψ_{JT} and Ψ_{JB}) are given in the *Thermal Information* table and are used in accordance with Equation 9.

$$\Psi_{JT}: T_J = T_T + \Psi_{JT} \times P_D$$
$$\Psi_{JB}: T_J = T_B + \Psi_{JB} \times P_D$$

where:

- P_D is the power dissipated as explained in Equation 7,
- T_T is the temperature at the center-top of the device package, and
- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge (9)

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

相关文档如下（下载网站 www.ti.com.cn）：

- *《TPS7A47XXEVM-094 评估模块》*， 用户指南 SLVU741A
- *《使用前馈电容器和低压降稳压器的优缺点》*， 应用手册 SBVA042

11.2 相关链接

表 4 列出了快速访问链接。 范围包括技术文档、支持与社区资源、工具和软件，并且可以快速访问样片或购买链接。

表 4. 相关链接

部件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
TPS7A4700	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TPS7A4701	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

11.3 商标

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11.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.5 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

12 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A4700RGWR	ACTIVE	VQFN	RGW	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PXSQ	Samples
TPS7A4700RGWT	ACTIVE	VQFN	RGW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PXSQ	Samples
TPS7A4701RGWR	ACTIVE	VQFN	RGW	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7A4701	Samples
TPS7A4701RGWT	ACTIVE	VQFN	RGW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7A4701	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

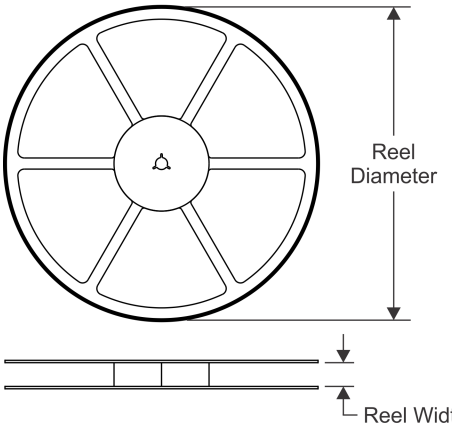
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

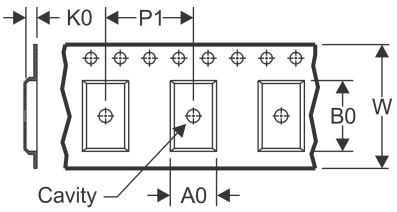
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

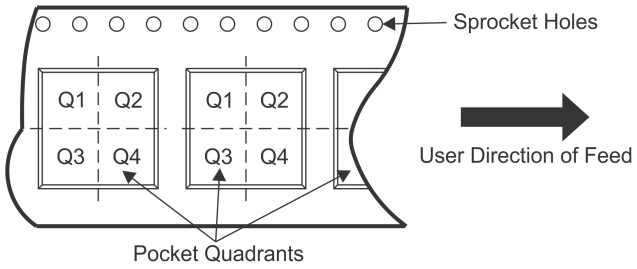


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

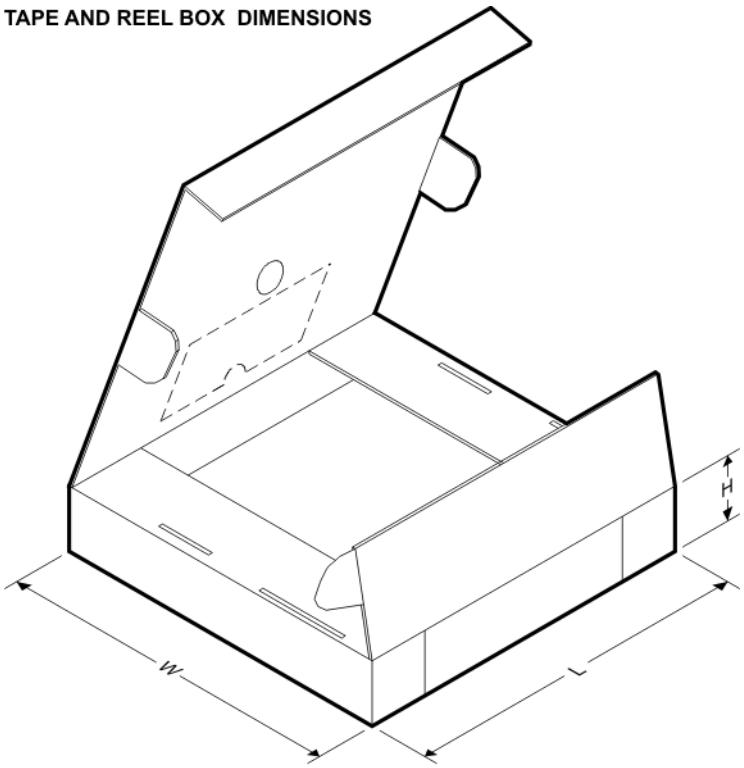
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A4700RGWR	VQFN	RGW	20	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TPS7A4700RGWT	VQFN	RGW	20	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TPS7A4701RGWR	VQFN	RGW	20	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TPS7A4701RGWT	VQFN	RGW	20	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

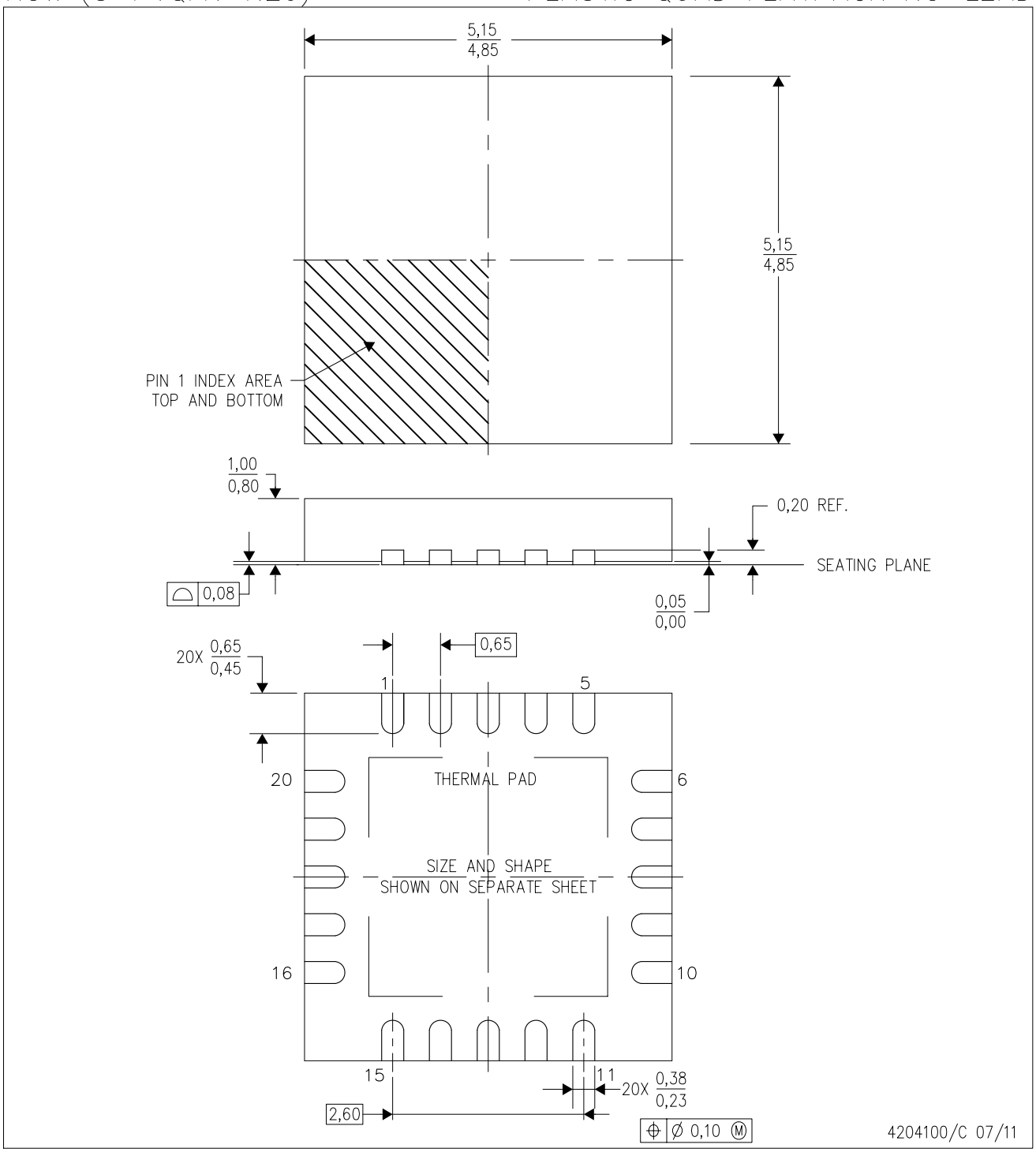
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A4700RGWR	VQFN	RGW	20	3000	367.0	367.0	35.0
TPS7A4700RGWT	VQFN	RGW	20	250	210.0	185.0	35.0
TPS7A4701RGWR	VQFN	RGW	20	3000	367.0	367.0	35.0
TPS7A4701RGWT	VQFN	RGW	20	250	210.0	185.0	35.0

RGW (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flat pack, No–leads (QFN) package configuration
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

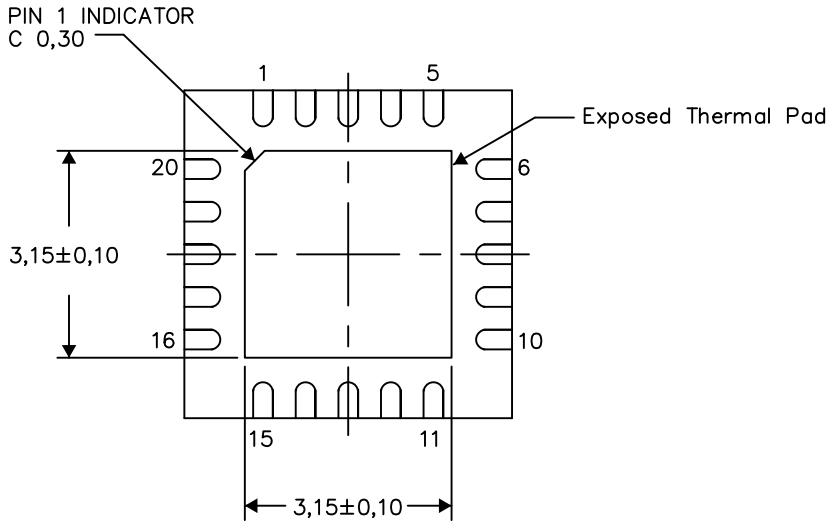
RGW (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



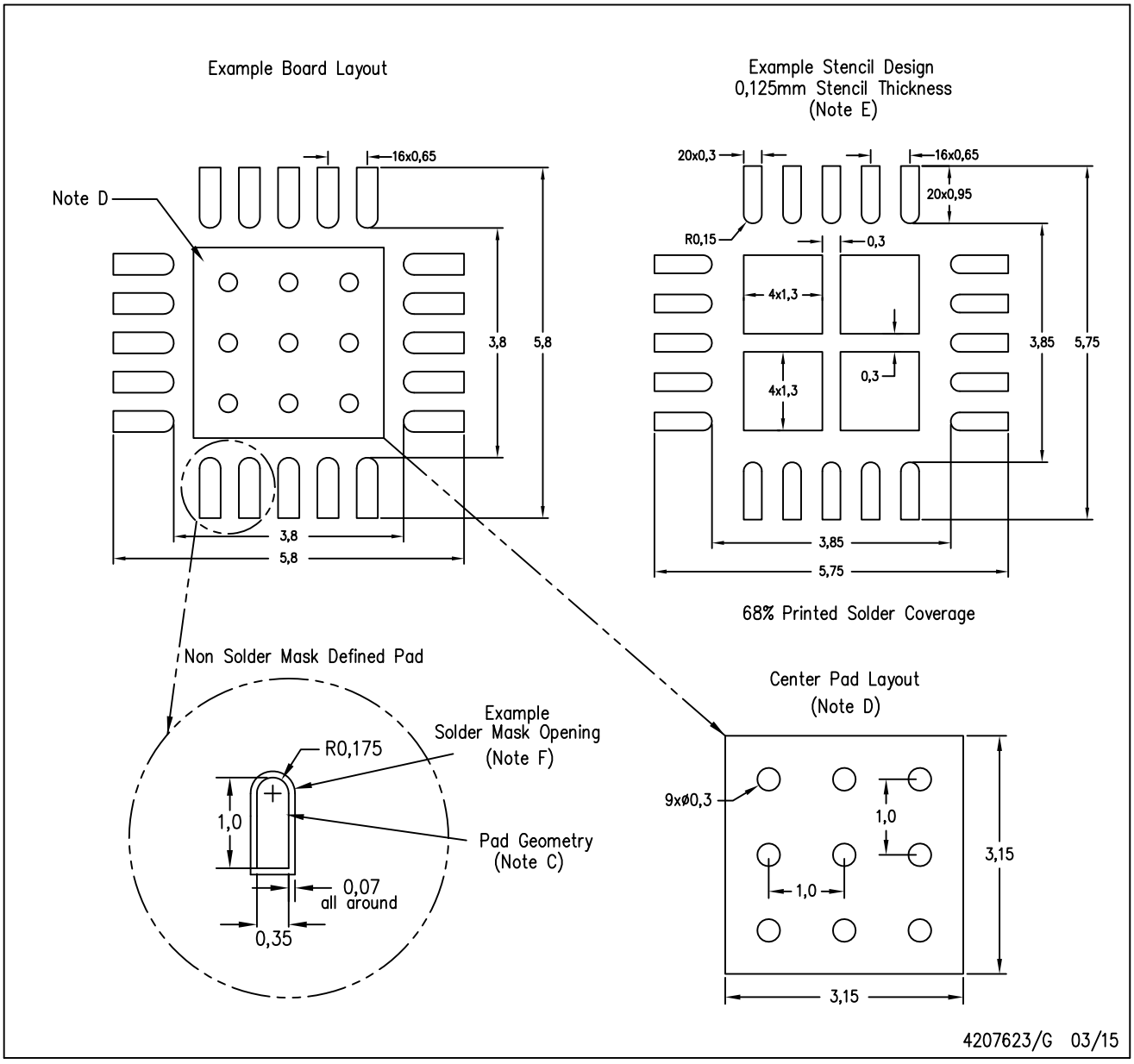
Bottom View

Exposed Thermal Pad Dimensions

4206352–2/M 06/15

NOTE: All linear dimensions are in millimeters

RGW (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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