

## Intel<sup>®</sup> MAX<sup>®</sup> 10

## INTEL® MAX® 10 FPGAS PRODUCT TABLE

PRODUCT LINE			10M02	10M04	10M08	10M16	10M25	10M40	10M50
LEs (K)			2	4	8	16	25	40	50
Block memory (Kb)			108	189	378	549	675	1,260	1,638
User flash memory¹ (KB)			12	16 – 156	32 – 172	32 – 296	32 – 400	64 – 736	64 – 736
18 x 18 multipliers			16	20	24	45	55	125	144
Phase-locked loops (PLLs) <sup>2</sup>			1, 2	1, 2	1, 2	1, 4	1, 4	1, 4	1, 4
Internal configuration			Single	Dual	Dual	Dual	Dual	Dual	Dual
Analog-to-digital converter (ADC), temperature sensing diode (TSD) <sup>3</sup>			-	1, 1	1, 1	1, 1	2, 1	2, 1	2, 1
External memory interface (EMIF)			Yes <sup>4</sup>	Yes <sup>4</sup>	Yes <sup>4</sup>	Yes⁵	Yes⁵	Yes⁵	Yes <sup>5</sup>
Package Options and I/O Pins: Feature Set Options, GPIO, True LVDS Transceiver/Receiver									
Dual Power Supply	V36 (D) <sup>6</sup>	WLCSP (3 mm, 0.4 mm pitch)	C, 27, 3/7	-	-	-	-	-	-
	V81 (D) <sup>7</sup>	WLCSP (4 mm, 0.4 mm pitch)	+	-	C/F, 56, 7/17	-	-	-	-
	F256 (D)	FBGA (17 mm, 1.0 mm pitch)	-	C/A, 178, 13/54					
	U324 (D)	UBGA (15 mm, 0.8 mm pitch)	C, 160, 9/47	C/A, 246, 15/81	C/A, 246, 15/81	C/A, 246, 15/81	-	-	-
	F484 (D)	FBGA (23 mm, 1.0 mm pitch)	-	-	C/A, 250, 15/83	C/A, 320, 22/116	C/A, 360, 24/136	C/A, 360, 24/136	C/A, 360, 24/136
	F672 (D)	FBGA (27 mm, 1.0 mm pitch)	-	-	-	-	-	C/A, 500, 30/192	C/A, 500, 30/192
Single Power Supply	E144 (S) <sup>6</sup>	EQFP (22 mm, 0.5 mm pitch)	C, 101, 7/27	C/A, 101, 10/27	C/A, 101, 10/27	C/A, 101, 10/27	C/A, 101, 10/27	C/A, 101, 10/28	C/A, 101, 10/28
	M153 (S)	MBGA (8 mm, 0.5 mm pitch) <sup>8</sup>	C, 112, 9/29	C/A, 112, 9/29	C/A, 112, 9/29	-	-	-	-
	U169 (S)	UBGA (11 mm, 0.8 mm pitch)	C, 130, 9/38	C/A, 130, 9/38	C/A, 130, 9/38	C/A, 130, 9/38	-	-	-
	U324 (S)	UBGA (15 mm, 0.8 mm pitch)	C, 246, 15/81	C/A, 246, 15/81	C/A, 246, 15/81	C/A, 246, 15/81			

## Notes

- 1. Additional user flash may be available, depending on configuration options.
- The number of PLLs available is dependent on the package option.
- 3. Availability of the ADC or TSD varies by package type. Smaller pin-count packages do not have access to the ADC hard IP.
- 4. SRAM only.
- 5. SRAM, DDR3 SDRAM, DDR2 SDRAM, or LPDDR2.
- 6. "D" = Dual power supply (1.2 V/2.5 V), "S" = Single power supply (3.3 V or 3.0 V).
- 7. V81 package does not support analog feature set. 10M08 V81 F devices support dual image with RSU.
- 8. "Easy PCB" utilizes 0.8 mm PCB design rules.
- 9. All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit www.altera.com.

C, 27, 3/7 Indicates feature set options, GPIO count, and LVDS transmitter or receiver count. Feature set options: C = Compact (single image), F = Flash (dual image with RSU), A = Analog (analog features block). Each has added premiums.

Indicates pin migration.

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