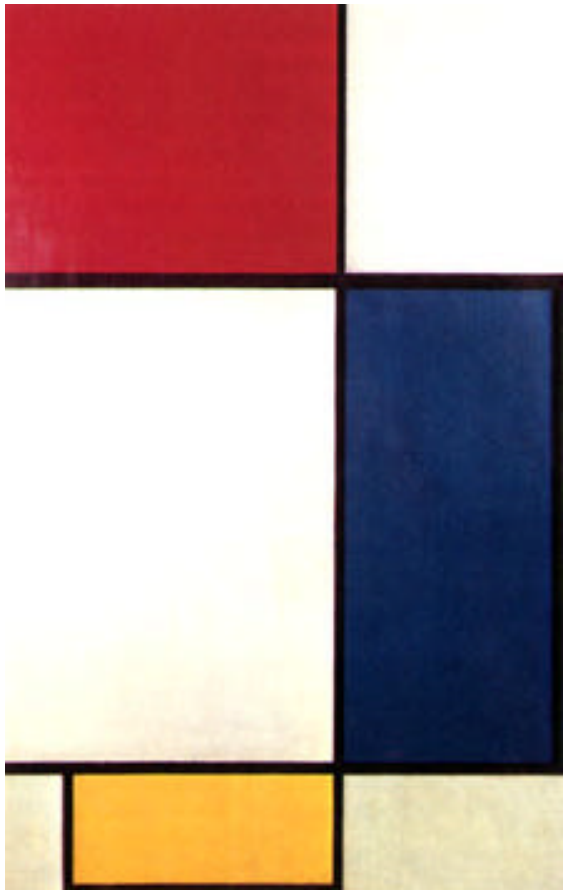
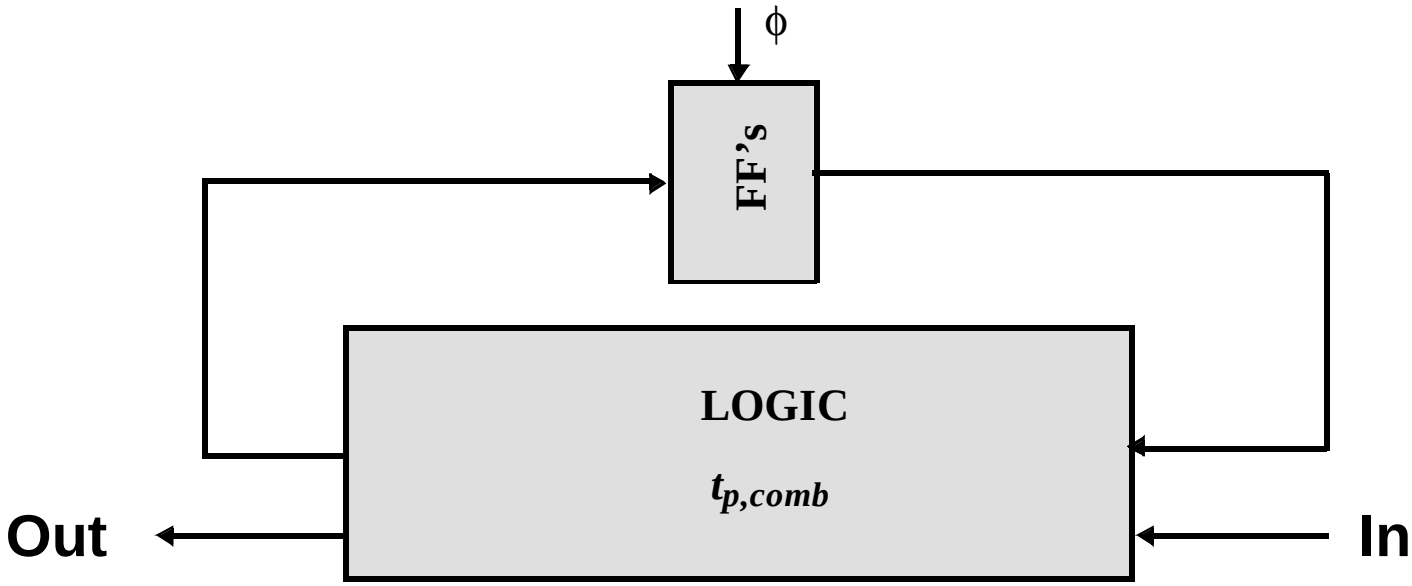
SEQUENTIAL LOGIC



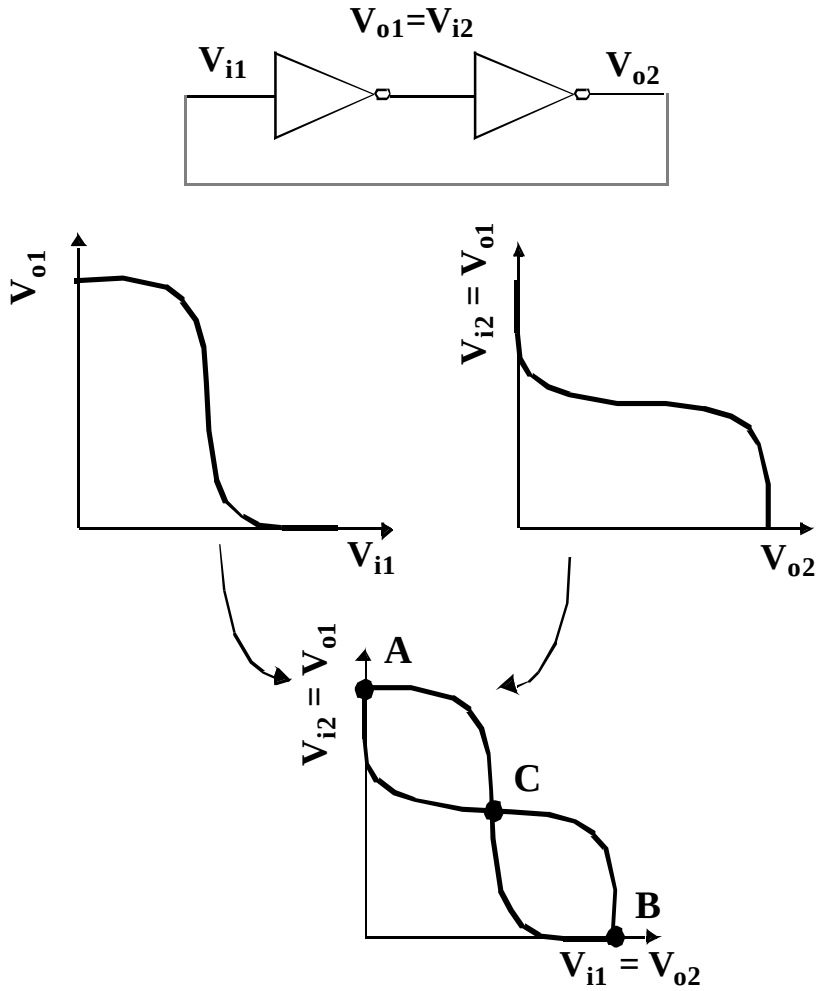
Sequential Logic



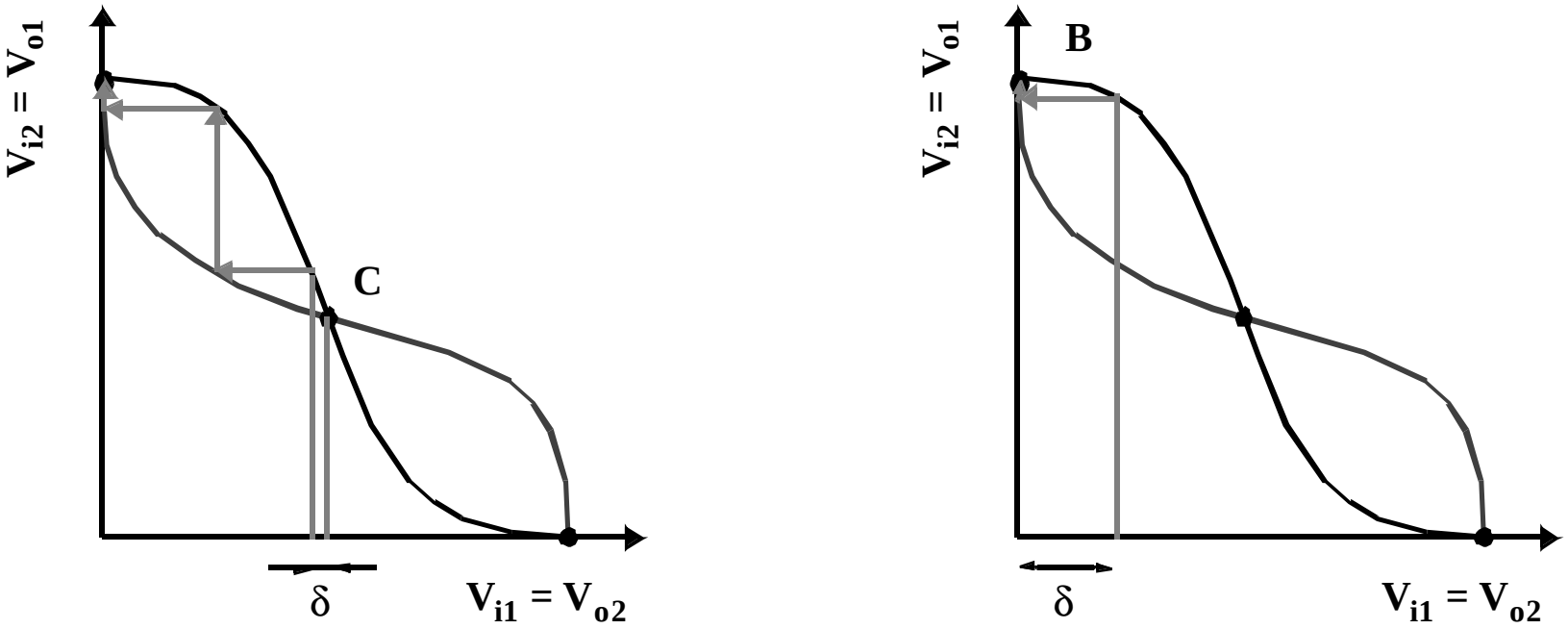
2 storage mechanisms

- **positive feedback**
- **charge-based**

Positive Feedback: Bi-Stability

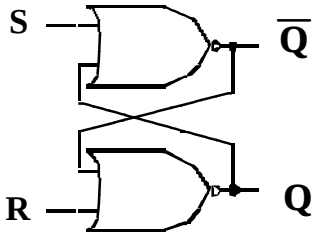


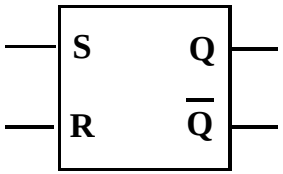
Meta-Stability



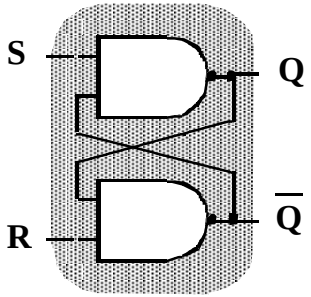
Gain should be larger than 1 in the transition region

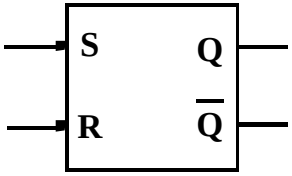
SR-Flip Flop





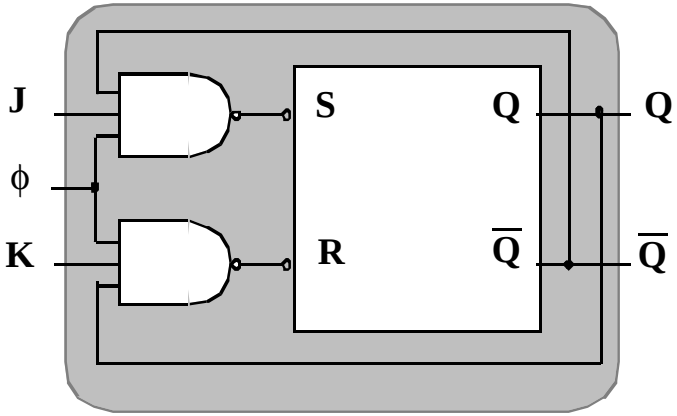
S	R	Q	$\overline{Q}$
0	0	Q	$\overline{Q}$
1	0	1	0
0	1	0	1
1	1	0	0



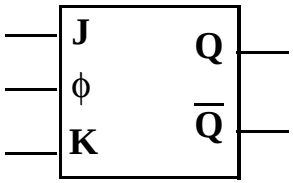


S	R	Q	$\overline{Q}$
1	1	Q	$\overline{Q}$
0	1	1	0
1	0	0	1
0	0	1	1

JK- Flip Flop



(a)

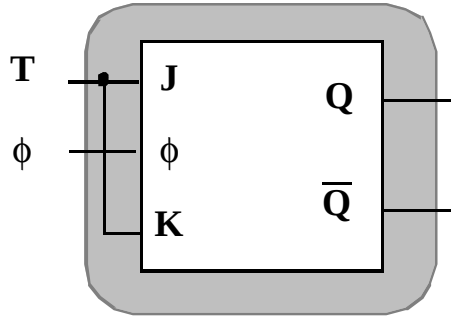


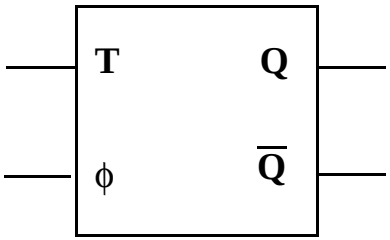
(b)

J_n	K_n	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

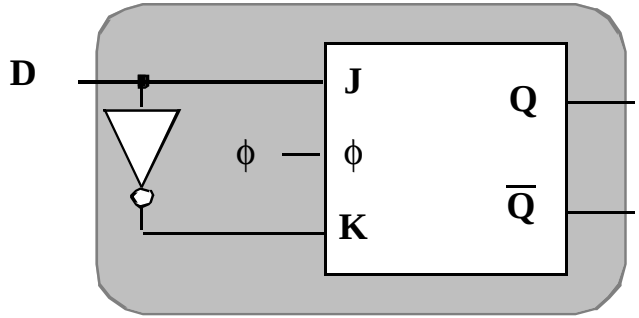
(c)

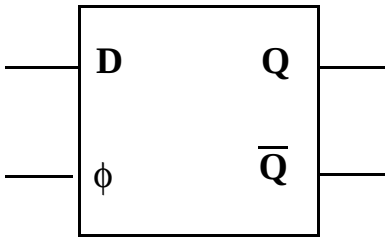
Other Flip-Flops





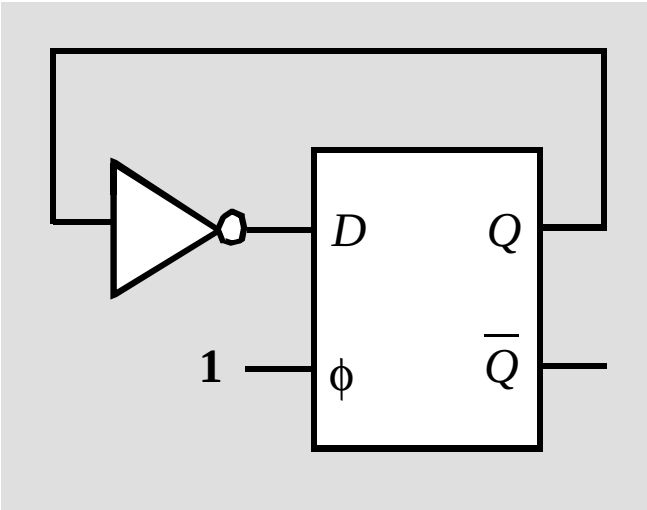
Toggle Flip-Flop

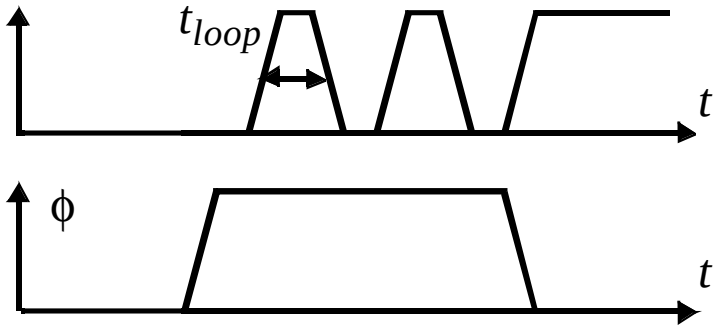




Delay Flip-Flop

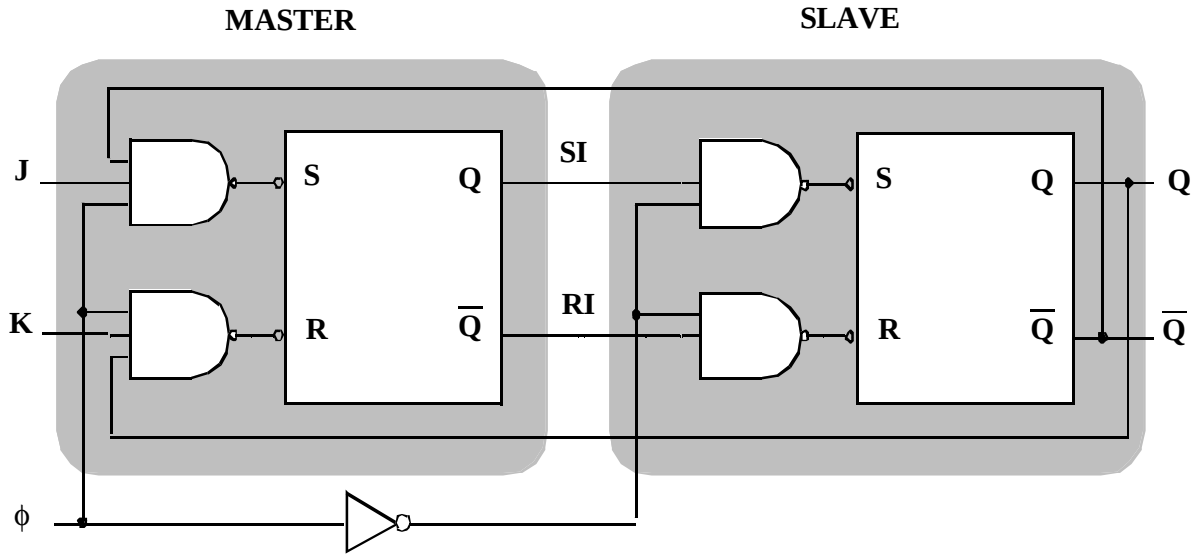
Race Problem

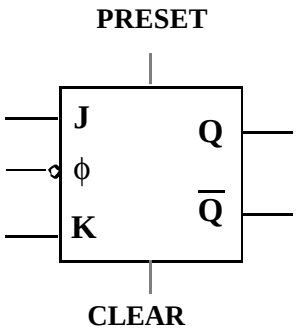




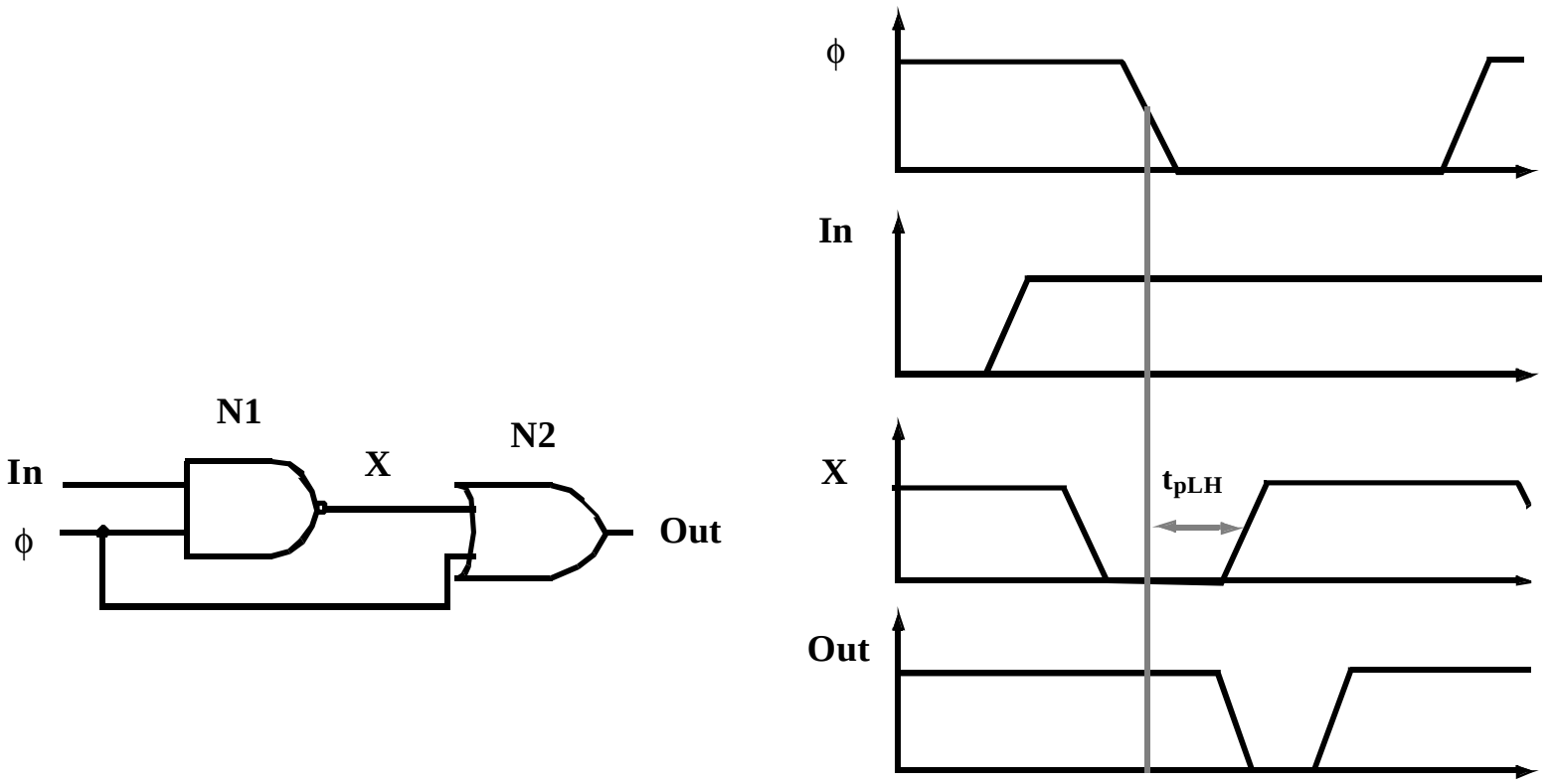
Signal can race around during ϕ = 1

Master-Slave Flip-Flop



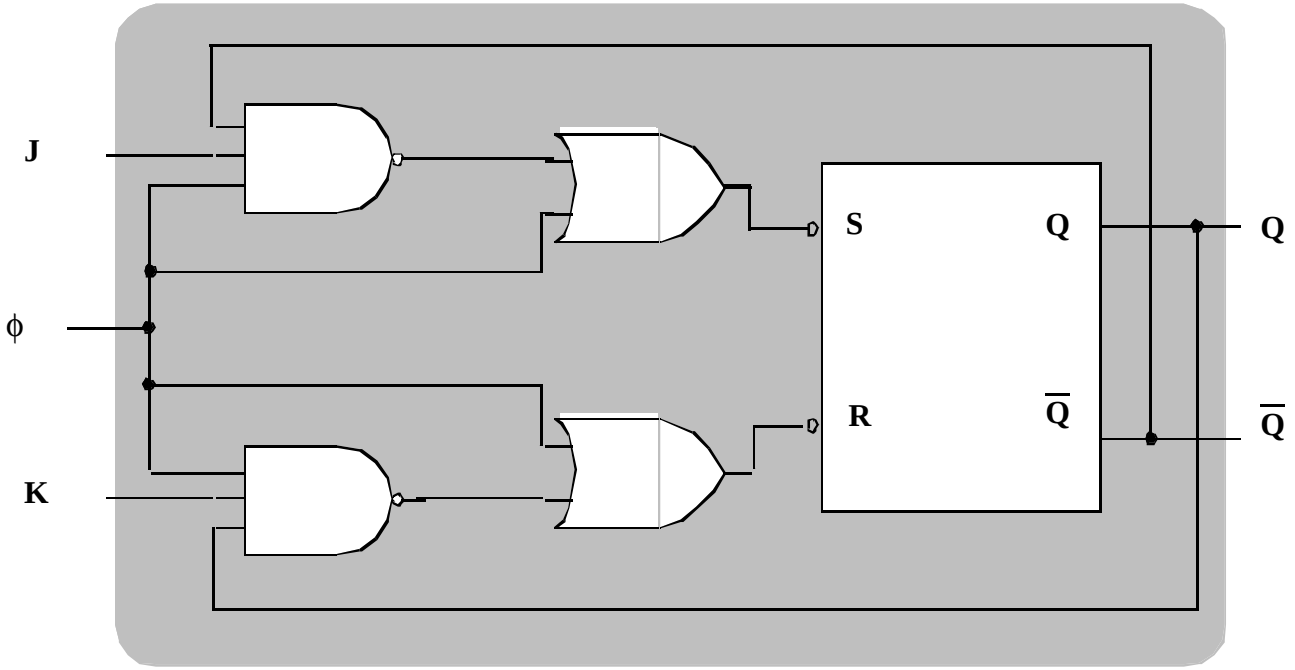


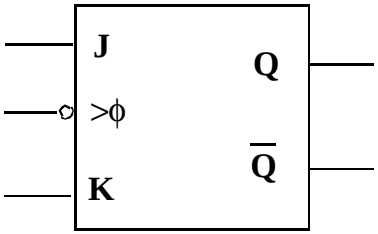
Propagation Delay Based Edge-Triggered



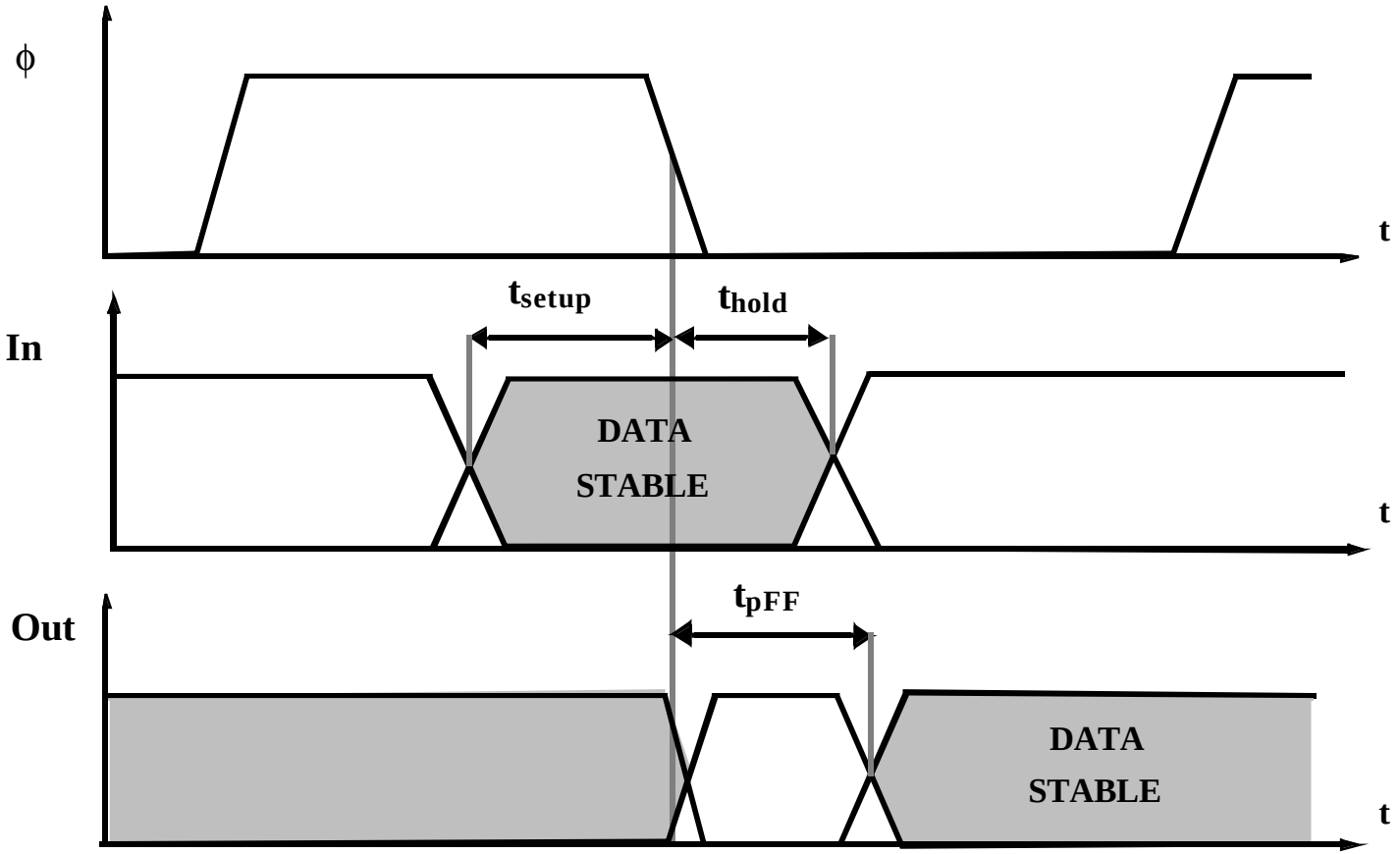
= Mono-Stable Multi-Vibrator

Edge Triggered Flip-Flop

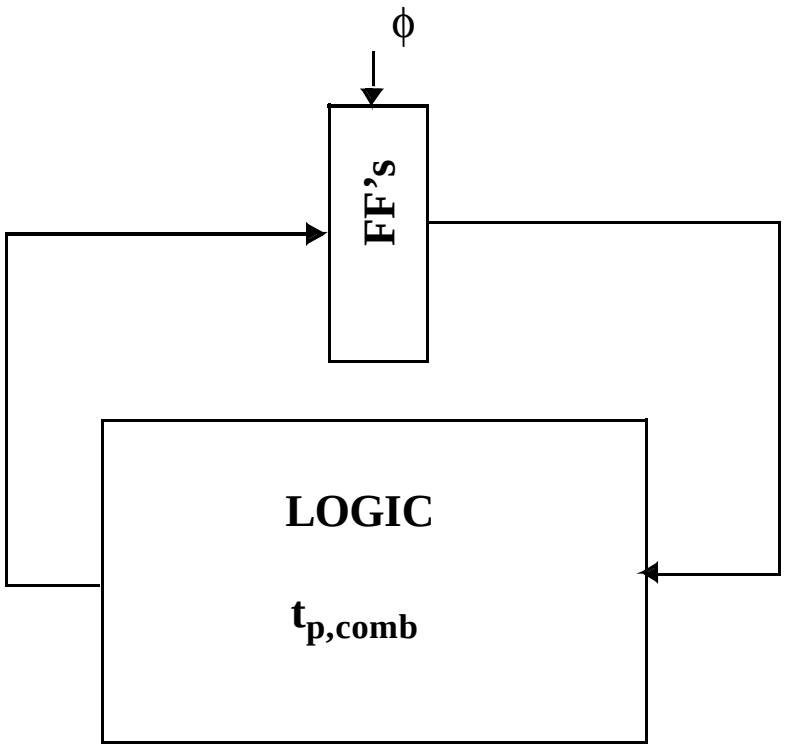




Flip-Flop: Timing Definitions

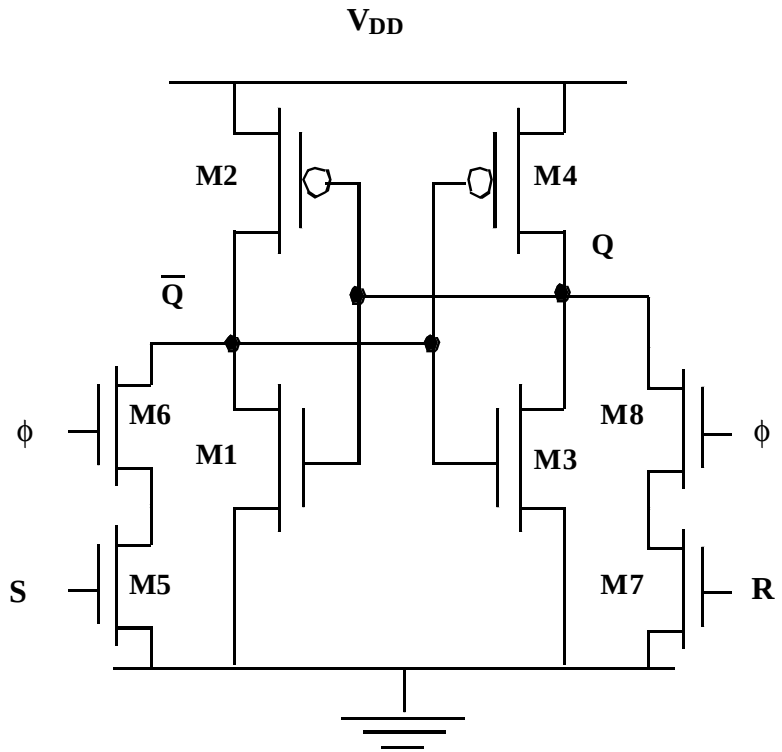


Maximum Clock Frequency

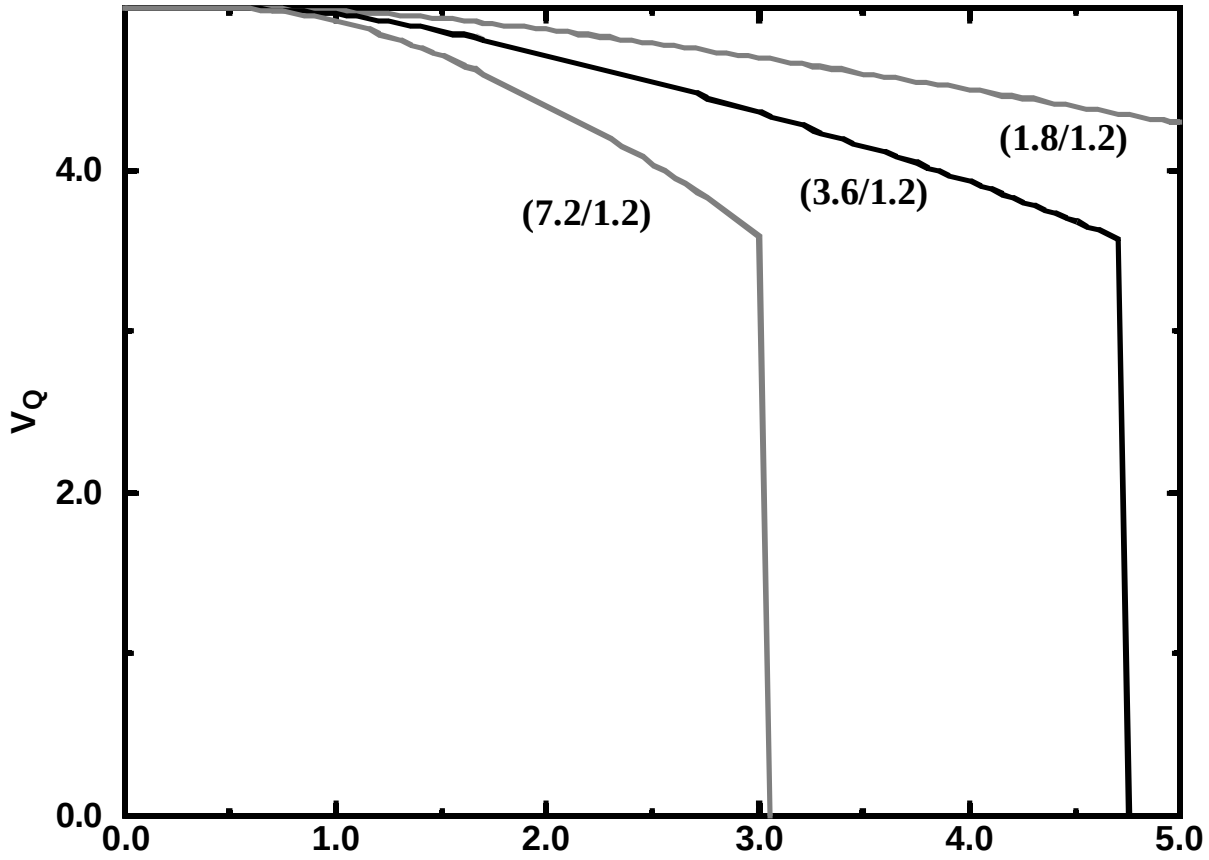


$$t_{pFF} + t_{p,comb} + t_{setup} < T$$

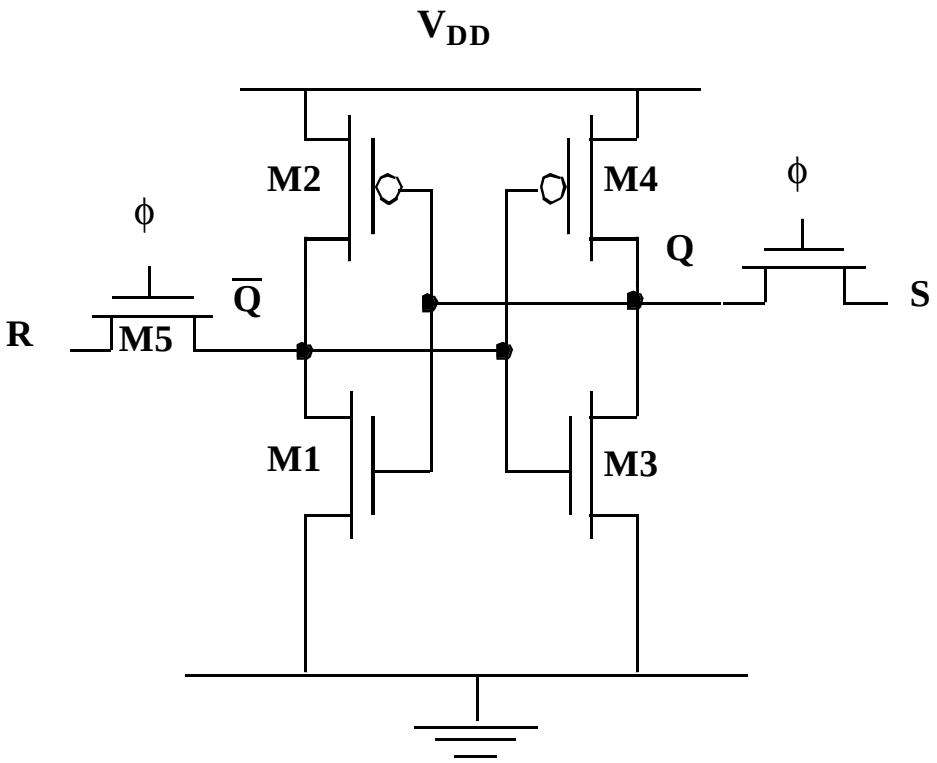
CMOS Clocked SR- FlipFlop



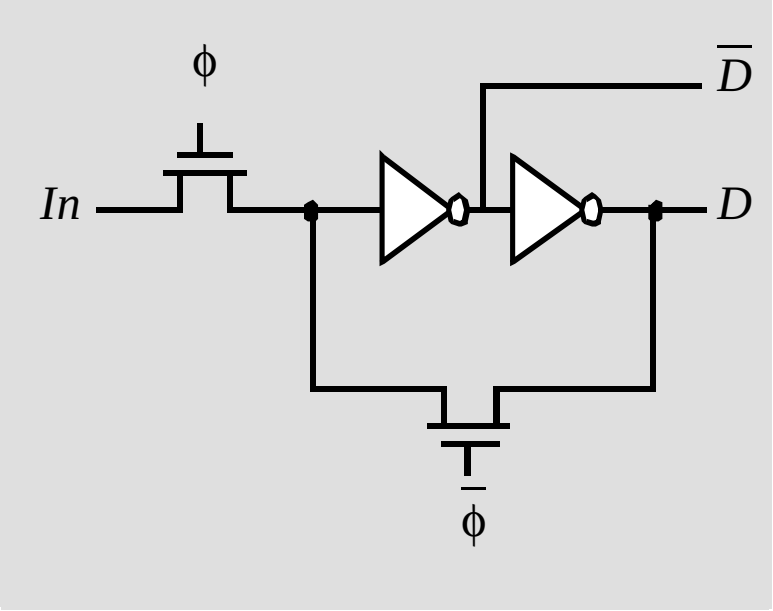
Flip-Flop: Transistor Sizing



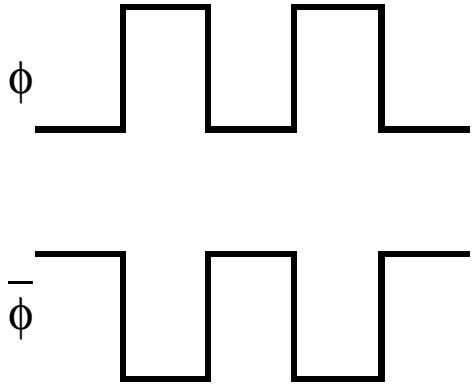
6 Transistor CMOS SR-Flip Flop



Charge-Based Storage



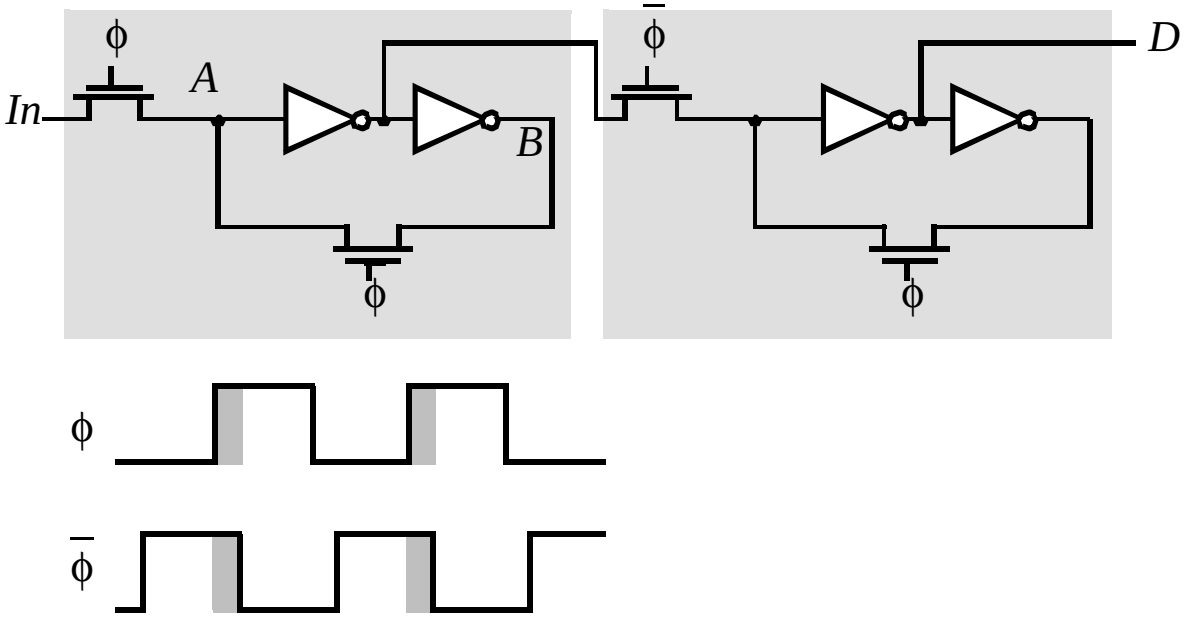
(a) Schematic diagram



(b) Non-overlapping clocks

Pseudo-static Latch

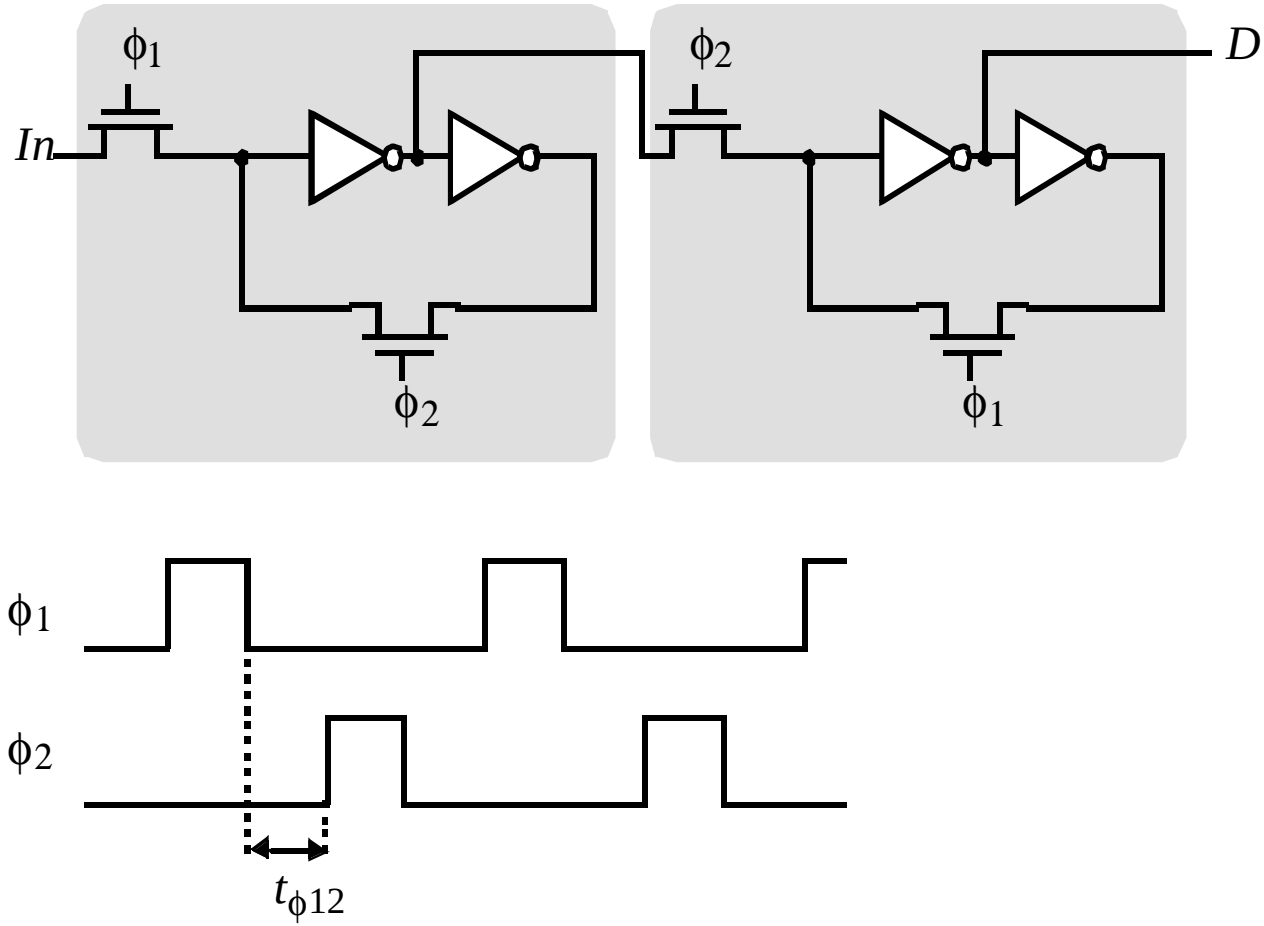
Master-Slave Flip-Flop



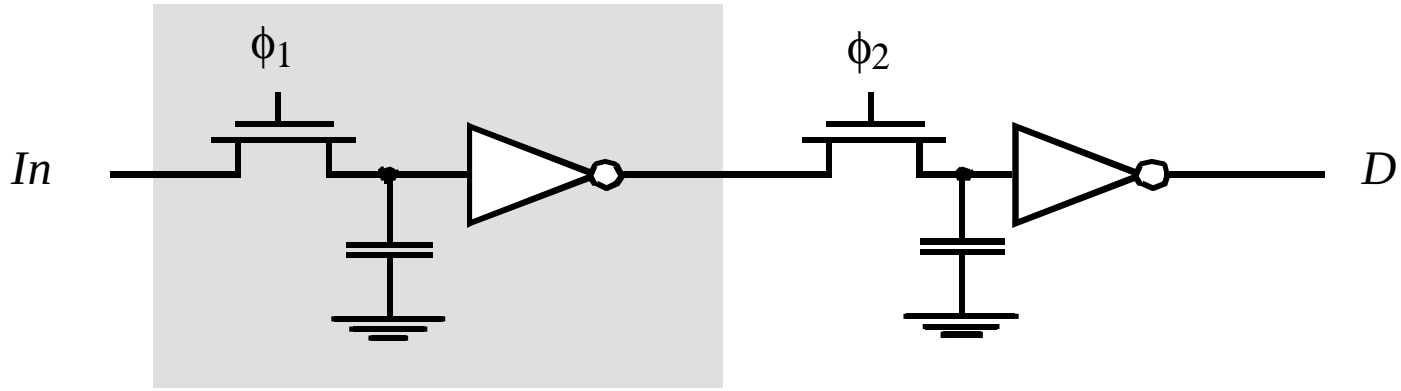
Overlapping Clocks Can Cause

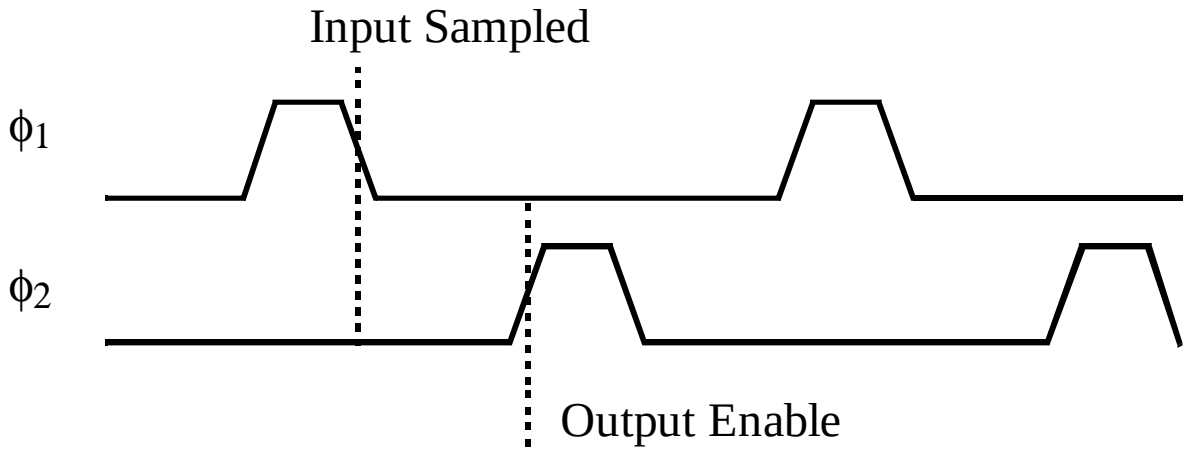
- **Race Conditions**
- **Undefined Signals**

2 phase non-overlapping clocks

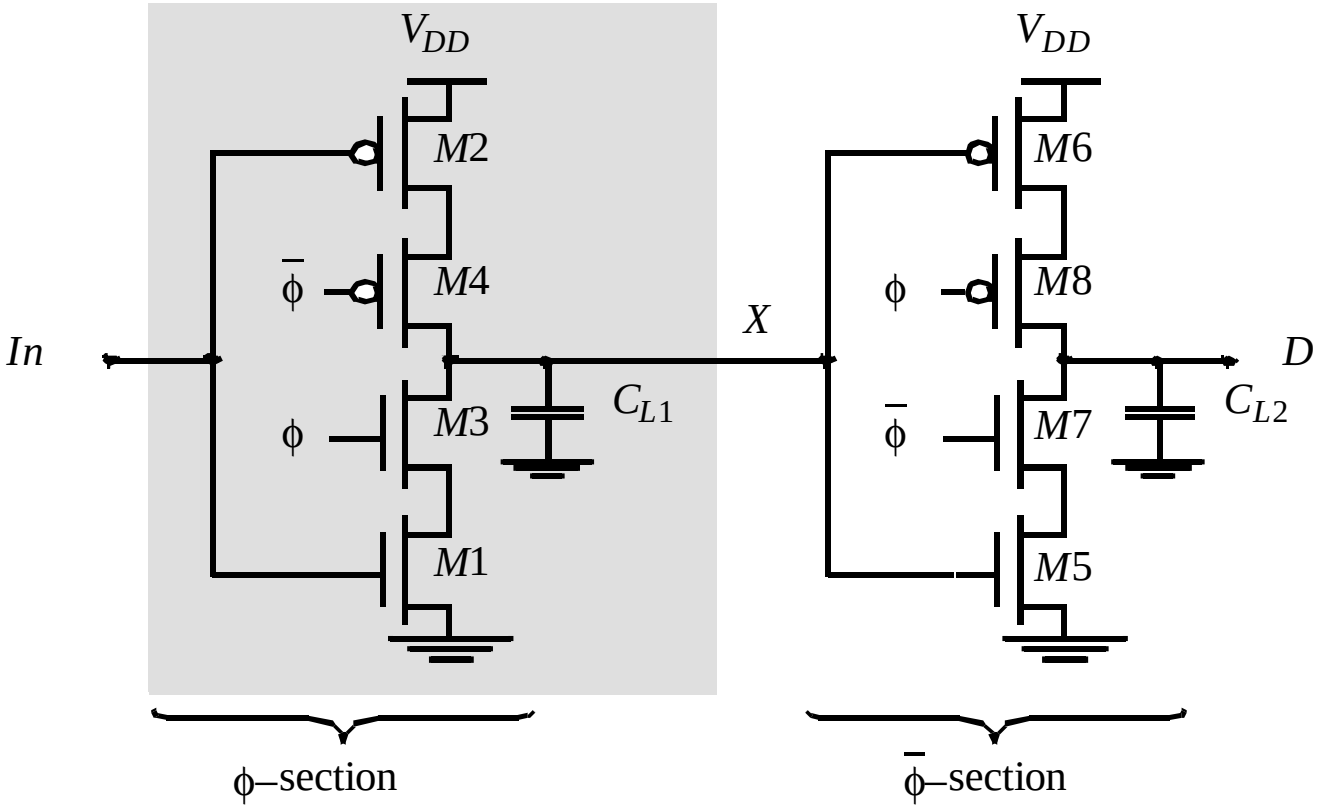


2-phase dynamic flip-flop



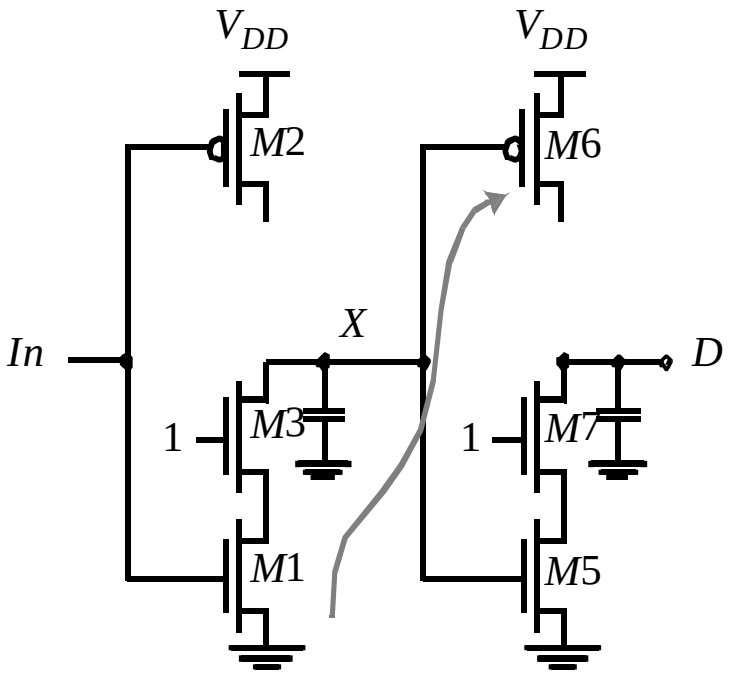


Flip-flop insensitive to clock overlap

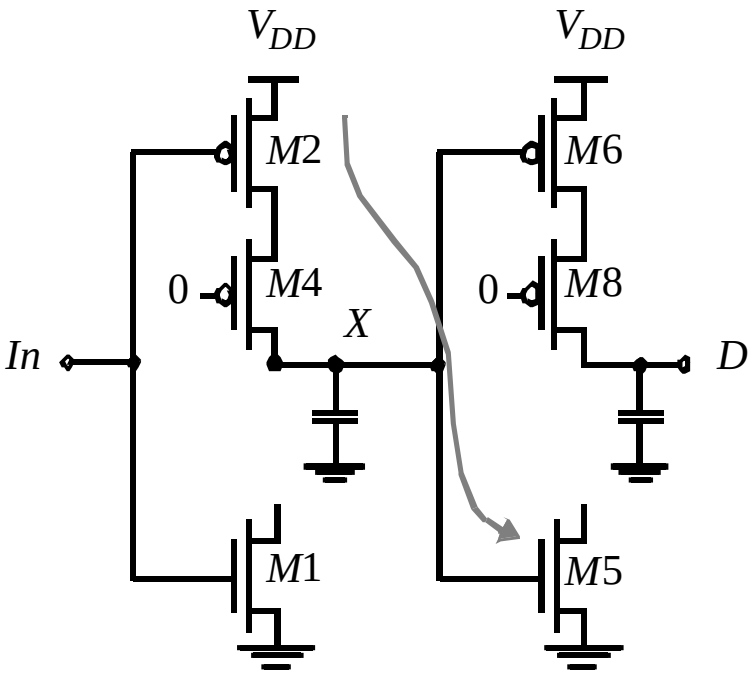


C²MOS LATCH

C²MOS avoids Race Conditions

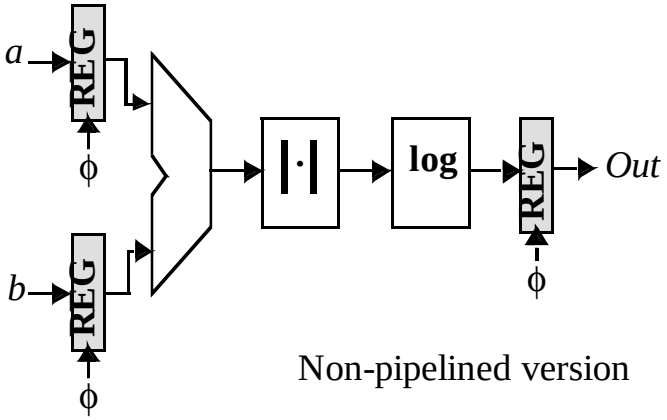


(a) (1-1) overlap

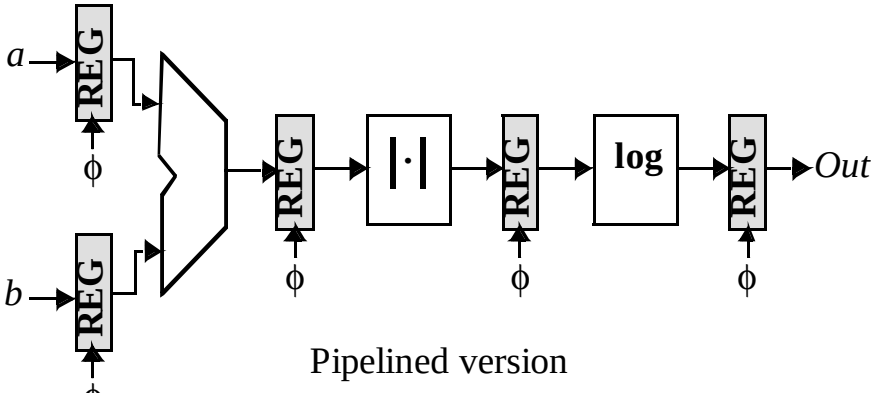


(b) (0-0) overlap

Pipelining



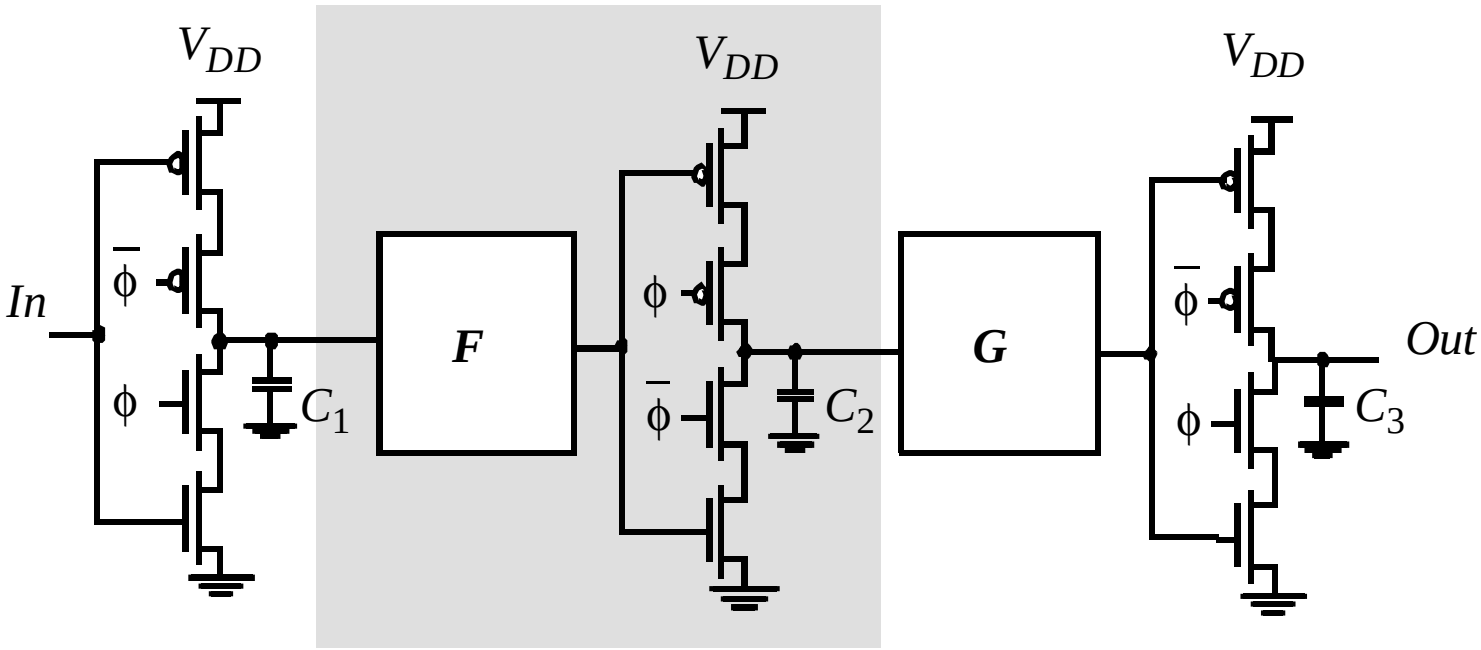
Non-pipelined version



Pipelined version

Clock Period	Adder	Absolute Value	Logarithm
1	$a_1 + b_1$		
2	$a_2 + b_2$	$\|a_1 + b_1\|$	
3	$a_3 + b_3$	$\|a_2 + b_2\|$	$\log(\|a_1 + b_1\|)$
4	$a_4 + b_4$	$\|a_3 + b_3\|$	$\log(\|a_2 + b_2\|)$
5	$a_5 + b_5$	$\|a_4 + b_4\|$	$\log(\|a_3 + b_3\|)$

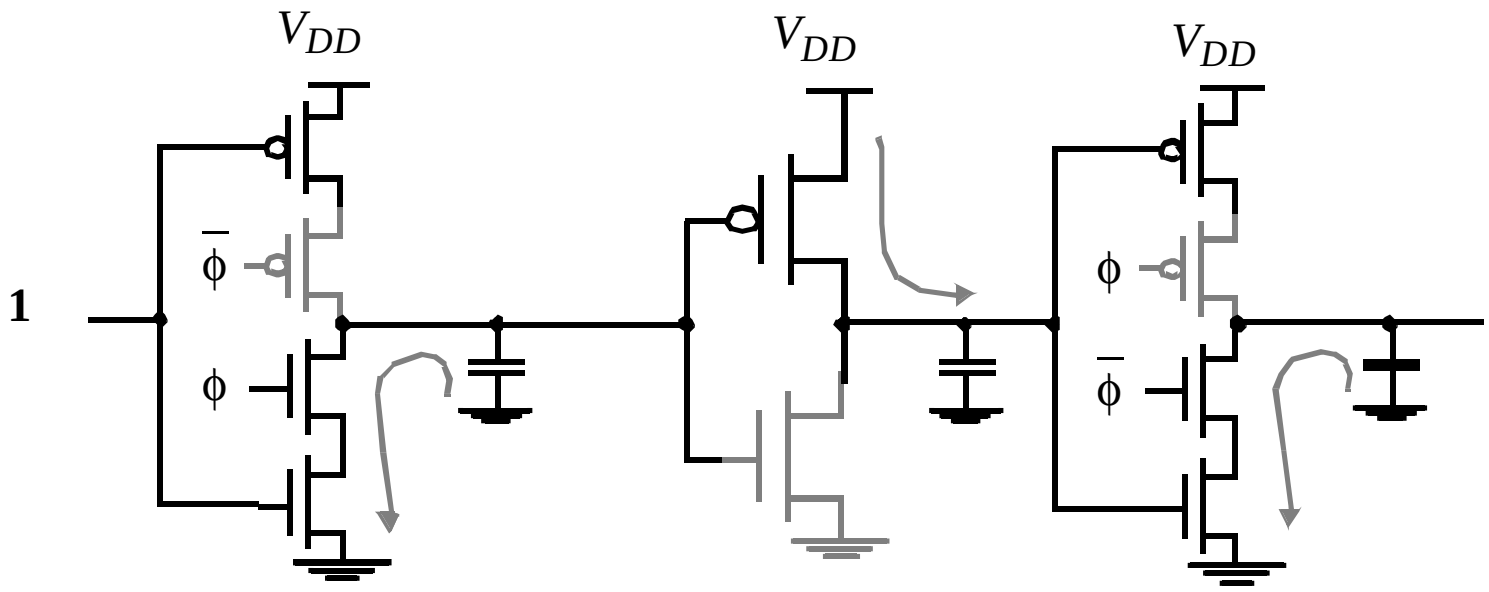
Pipelined Logic using C²MOS



NORA CMOS

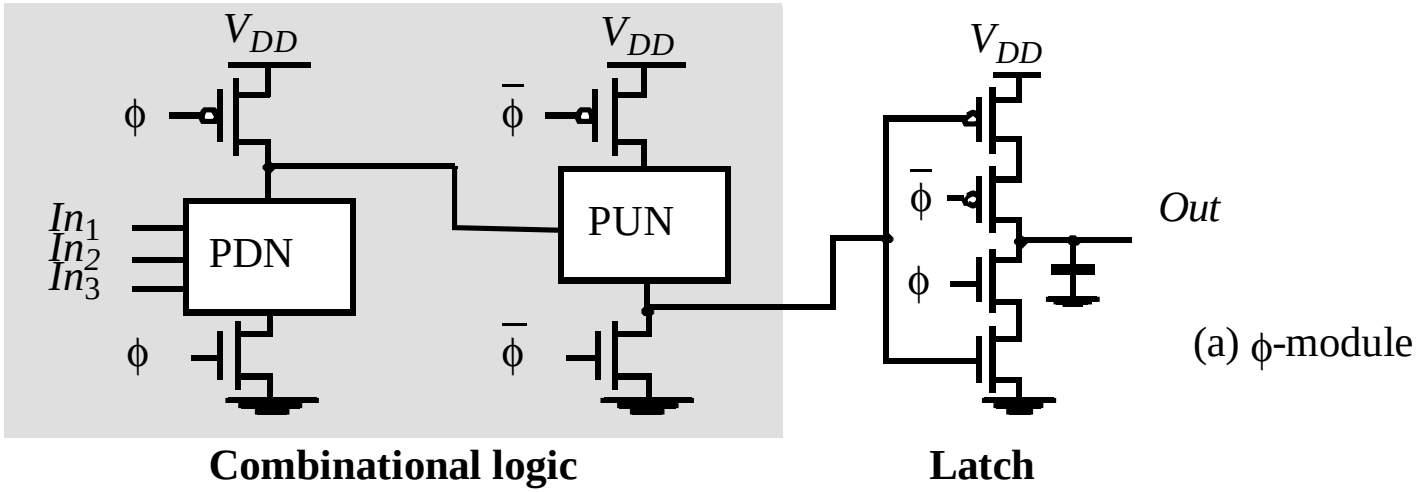
What are the constraints on F and G?

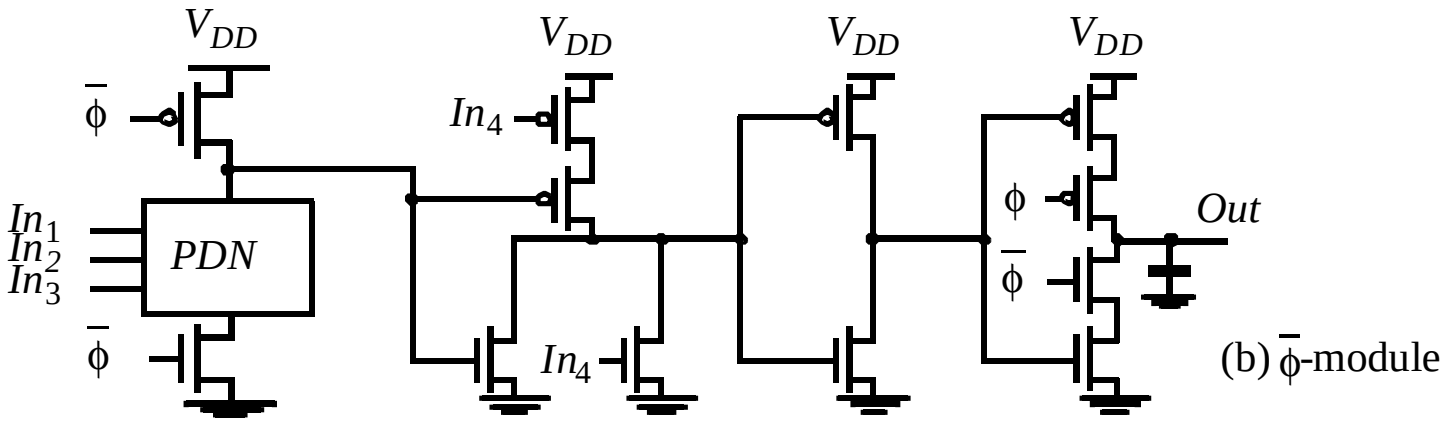
Example



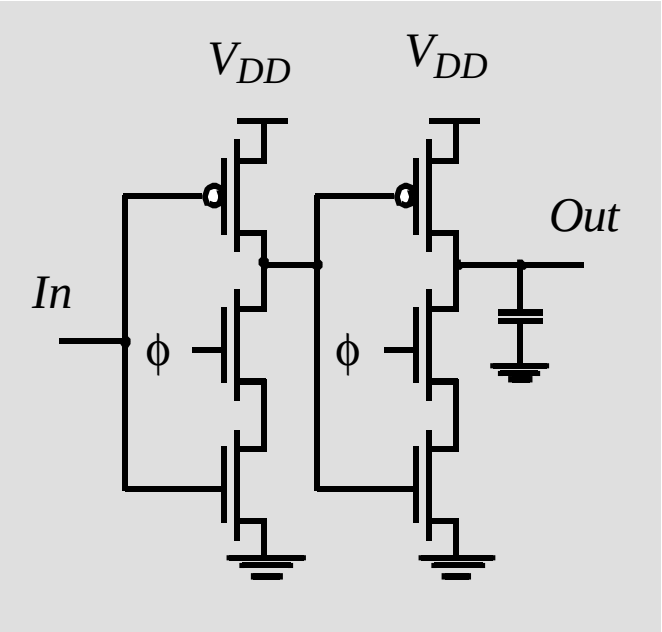
Number of a static inversions should be even

NORA CMOS Modules

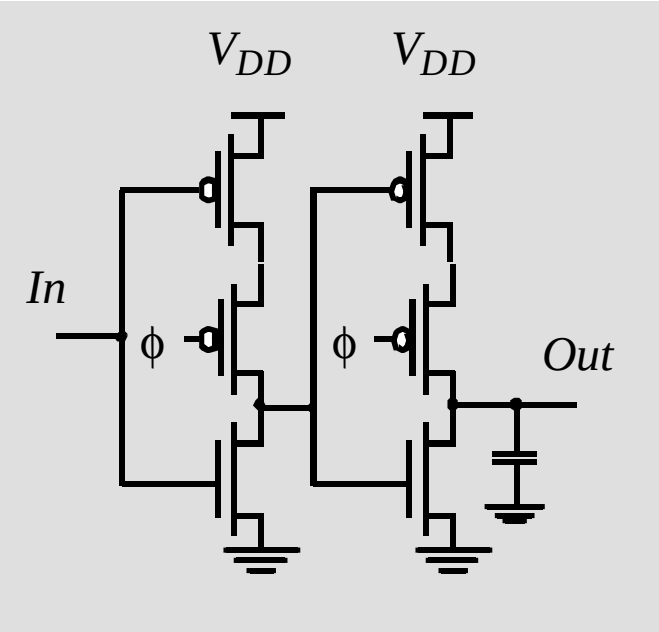




Doubled C²MOS Latches

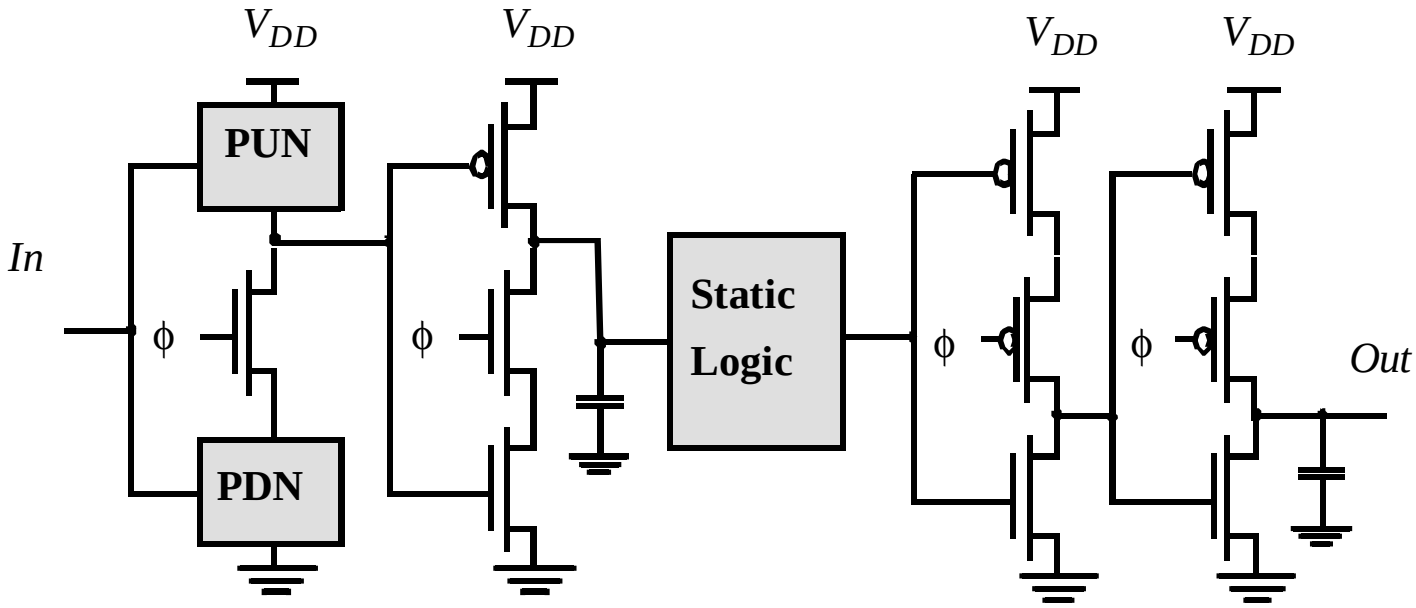


Doubled n-C²MOS latch



Doubled n-C²MOS latch

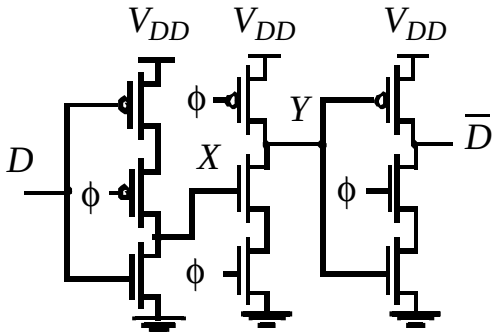
TSPC - True Single Phase Clock Logic



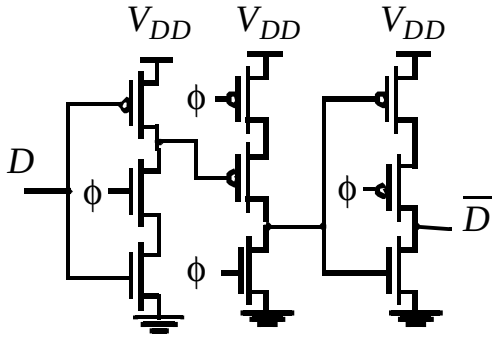
Including logic into the latch

Inserting logic between latches

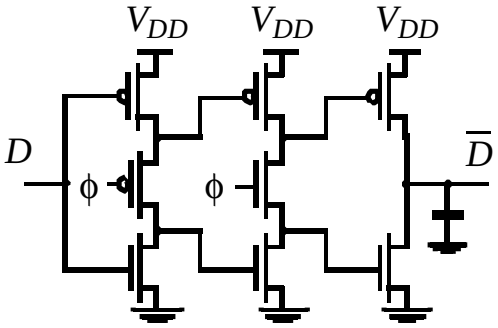
Master-Slave Flip-flops



(a) Positive edge-triggered *D* flip-flop

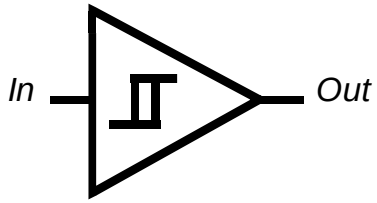


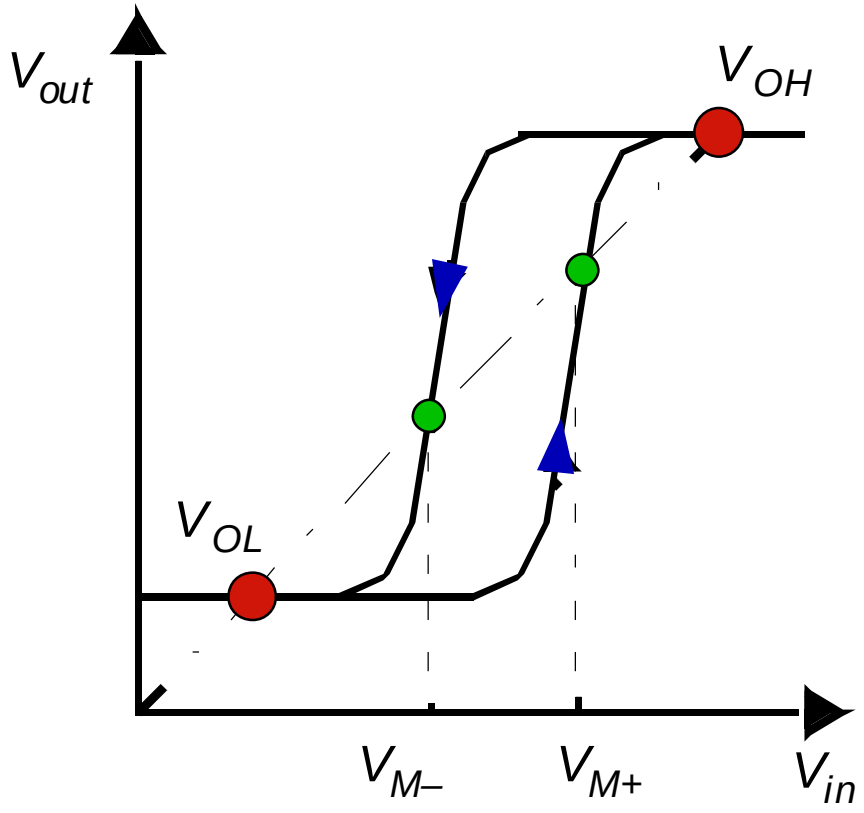
(b) Negative edge-triggered *D* flip-flop



(c) Positive edge-triggered *D* flip-flop using split-output latches

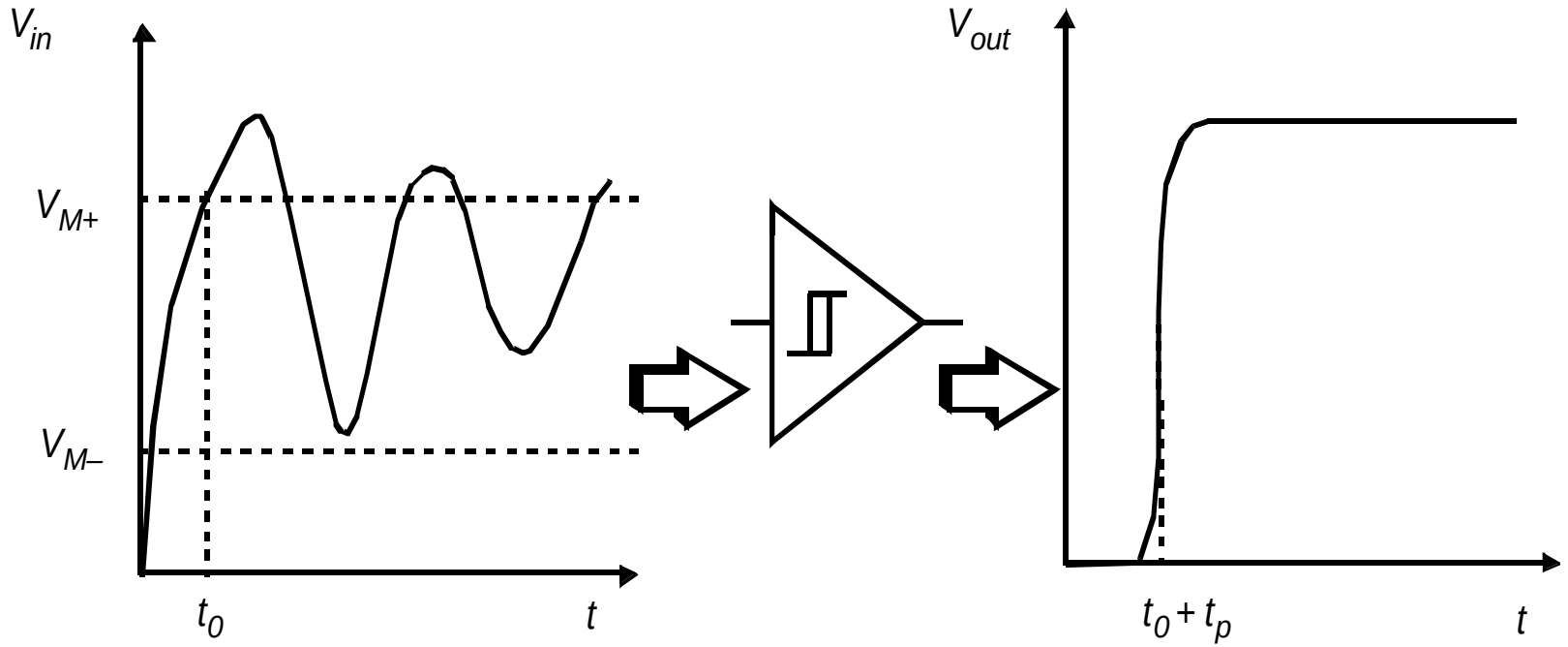
Schmitt Trigger



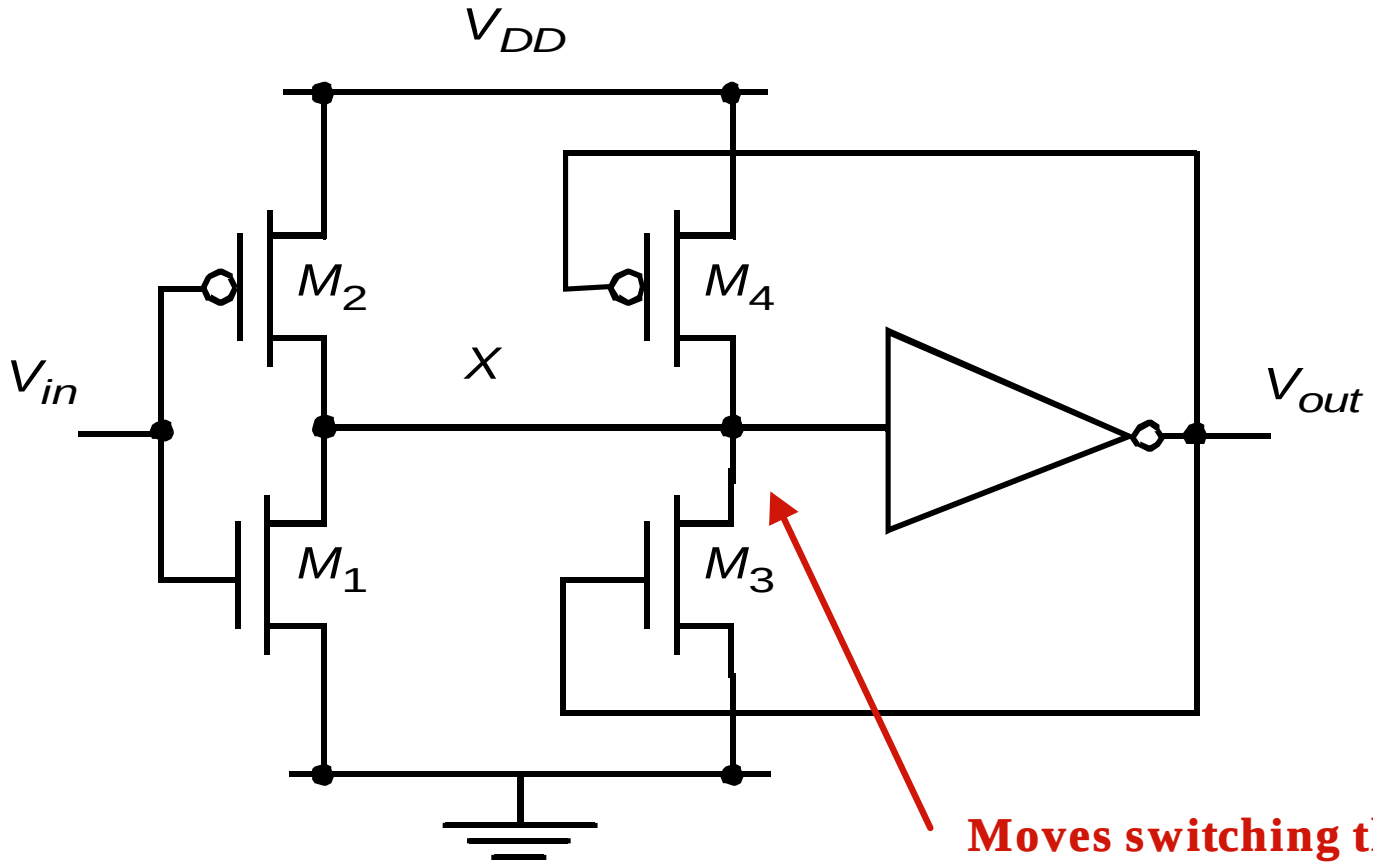


- **VTC with hysteresis**
- **Restores signal slopes**

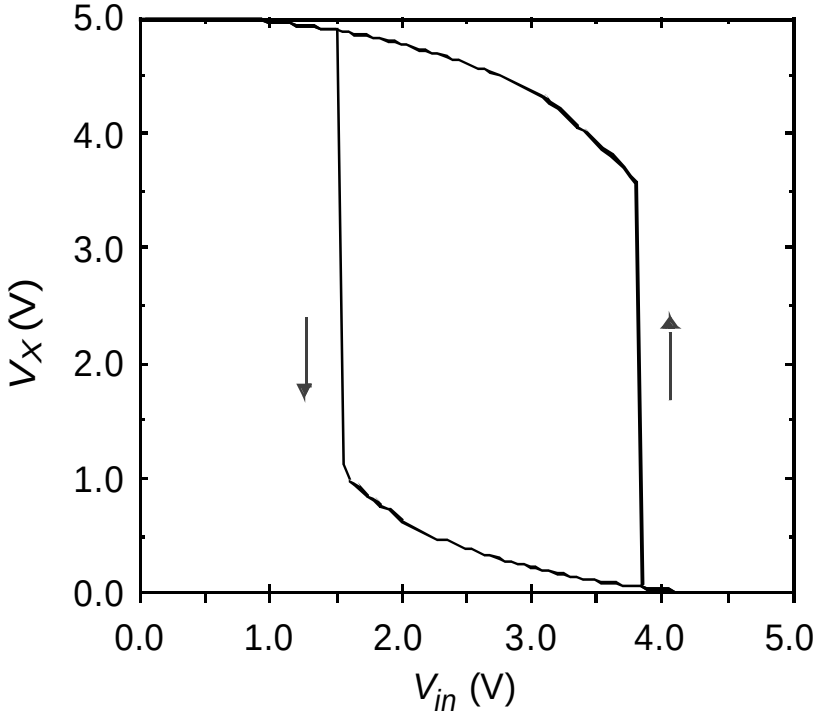
Noise Suppression using Schmitt Trigger

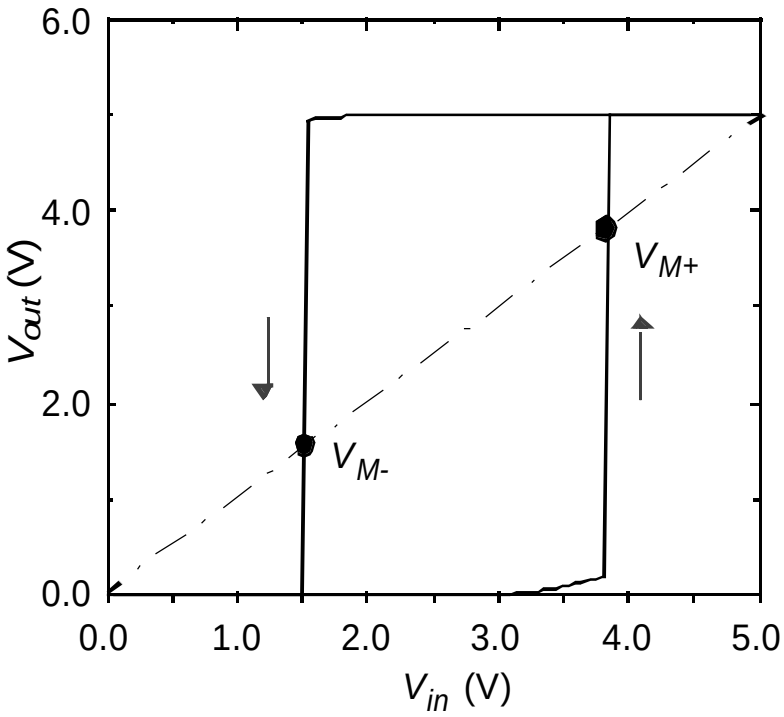


CMOS Schmitt Trigger

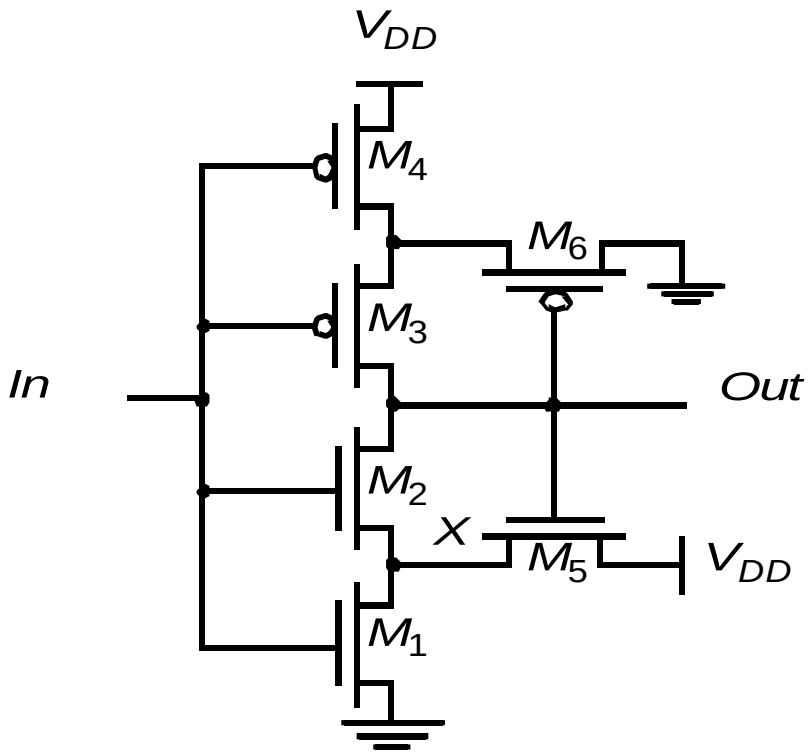


Schmitt Trigger Simulated VTC

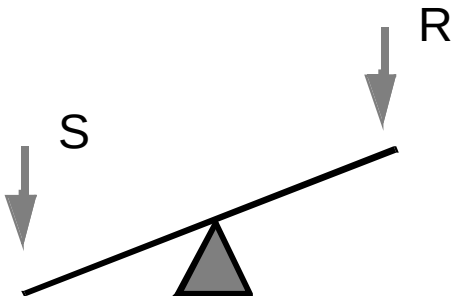




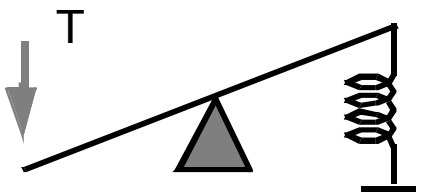
CMOS Schmitt Trigger (2)



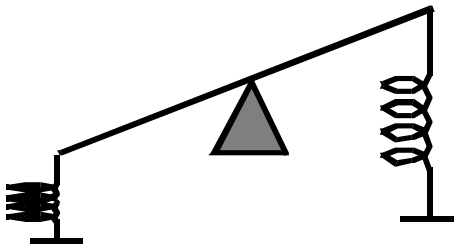
Multivibrator Circuits



Bistable Multivibrator
flip-flop, Schmitt Trigger

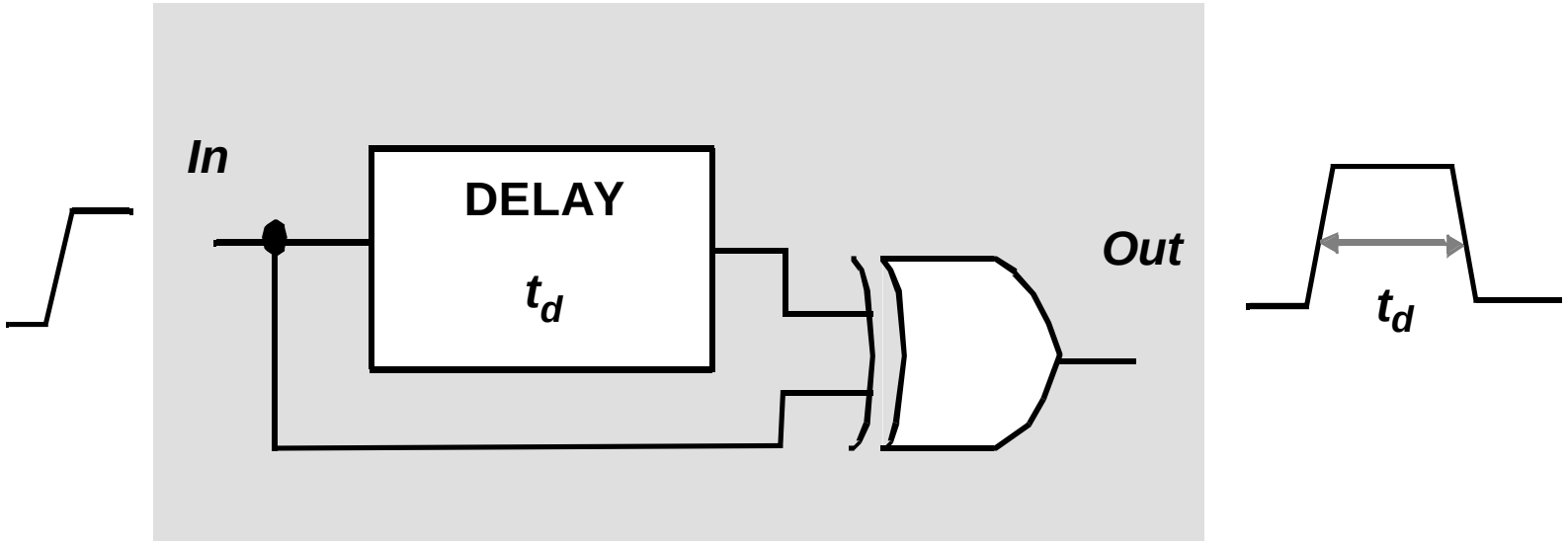


Monostable Multivibrator
one-shot

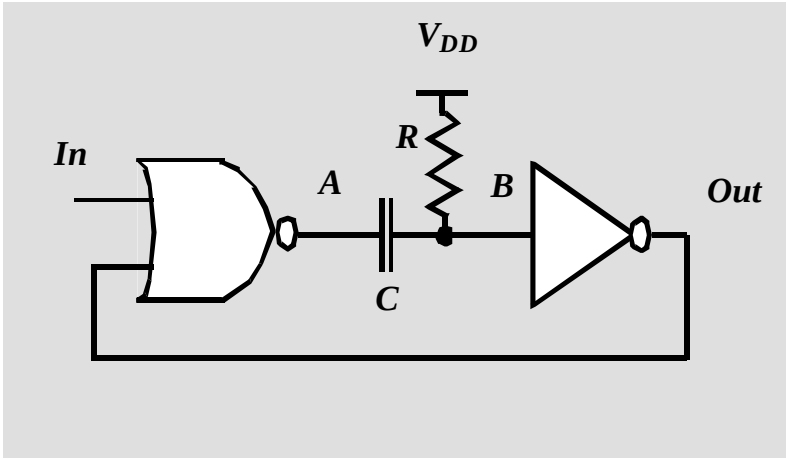


Astable Multivibrator
oscillator

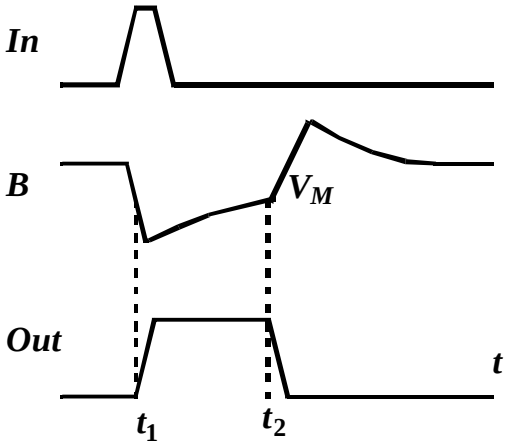
Transition-Triggered Monostable



Monostable Trigger (RC-based)

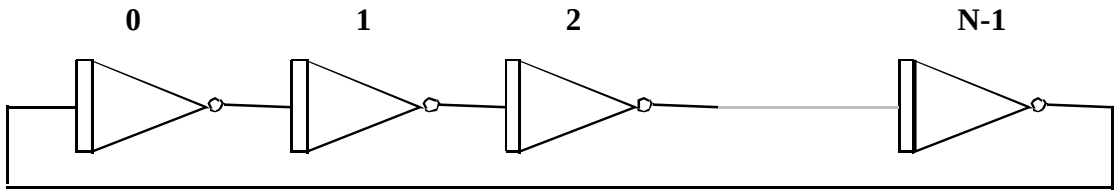


(a) Trigger circuit.

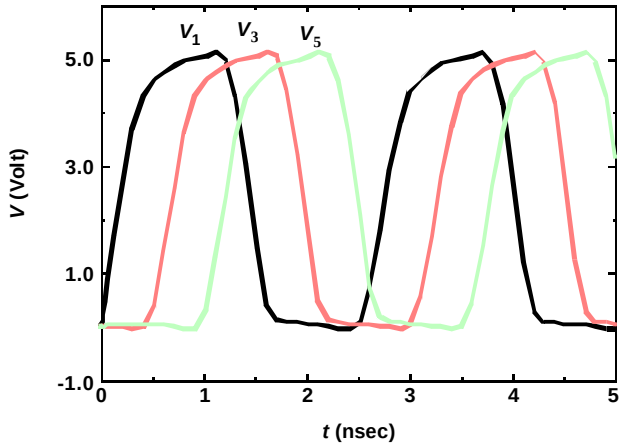


(b) Waveforms.

Astable Multivibrators (Oscillators)

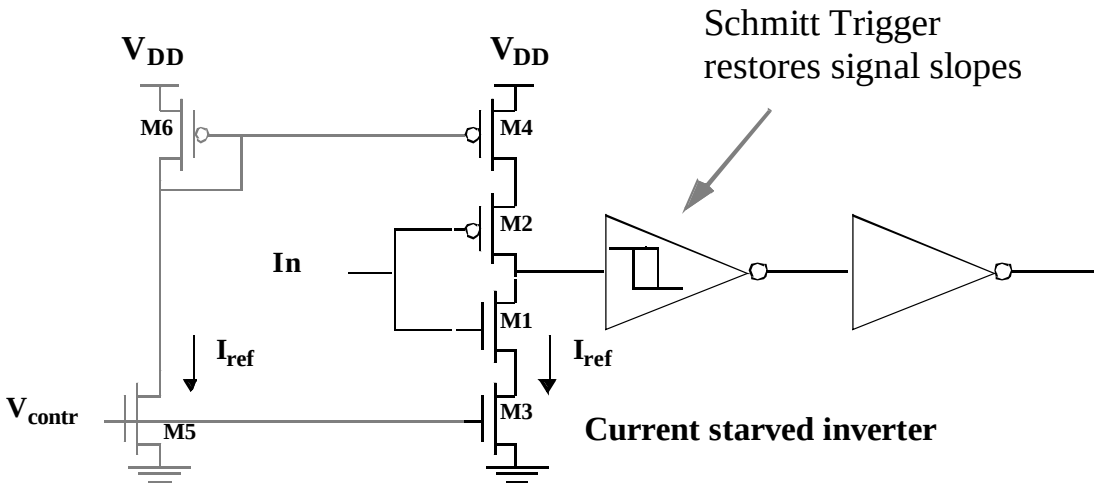


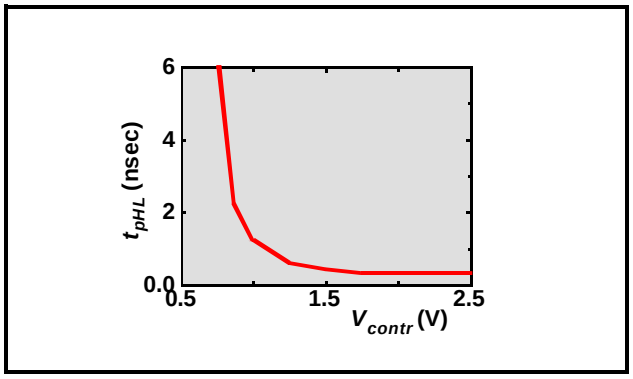
Ring Oscillator



simulated response of 5-stage oscillator

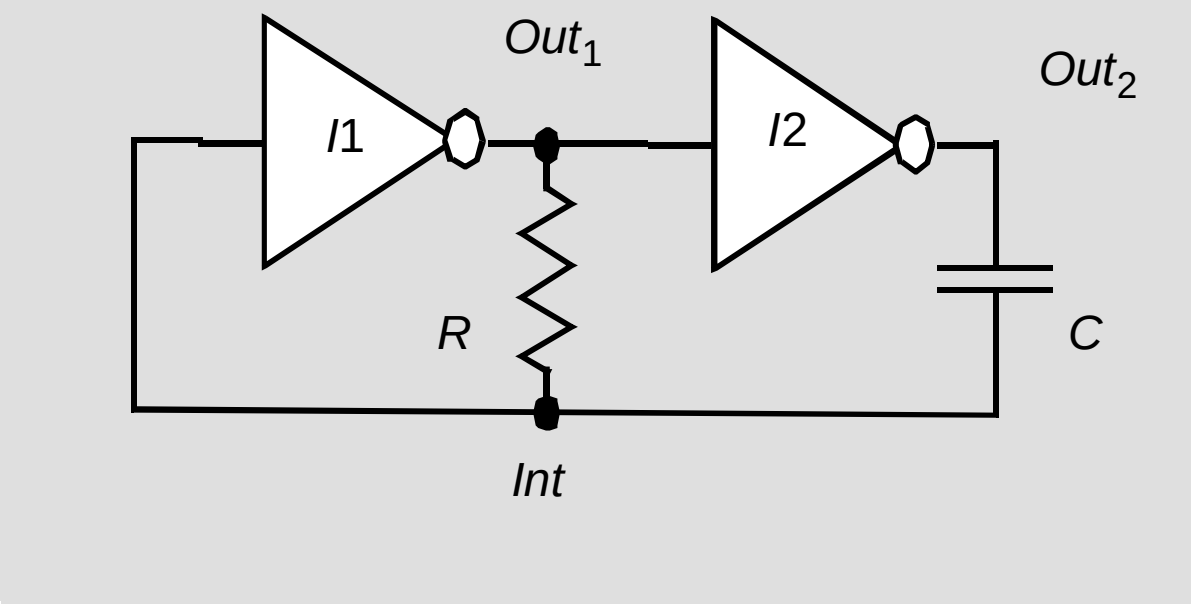
Voltage Controller Oscillator (VCO)





propagation delay as a function of control voltage

Relaxation Oscillator



$$T = 2\,(\log 3)\,RC$$