Problems in Old Midterm 1 Exam

To receive credits show all your work clearly. Write only answer gets 0.

1. **Number system and conversion**

   1a.1) Convert 155 to

   a) ***Binary*** number and

   b) ***Hexadecimal*** number

   1a.2) Convert 764 in octal-based number (base-8) to

   a) ***Binary*** number and

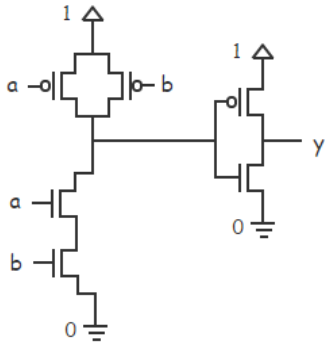
   b) ***Hexadecimal*** number

1b) Find a ***binary number*** of a given *decimal* number **456**

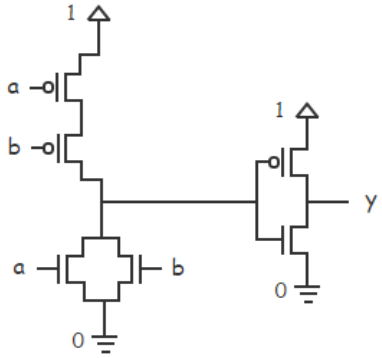
1c) Find ***hexadecimal number*** of a given *octal (based-8)* number $\mathbf{6471}_8$

2) Given the circuit implemented with transistors, choose (circle) the one that implements the logic 2-input **NOR gate**.

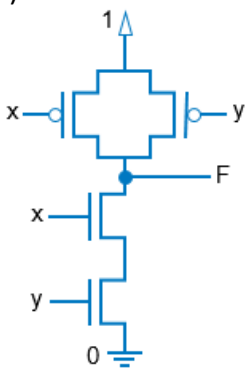
(a)



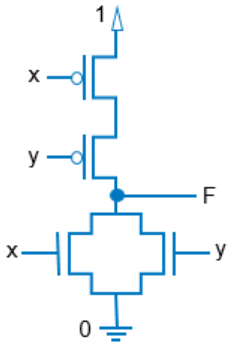
(b)



(c)



(d)



3) Which of the following is the correct Boolean equation for **output d12 of a 4x16 decoder**?
Note: inputs are in the order i3 i2 i1 i0 and outputs are in the order of d15 d14 … d1 d0

(a) d12 = i3 + i2 + i1' + i0

(b) d12 = i3 + i2 + i1' + i0'

(c) d12 = i3 i2 i1' i0

(d) d12 = i3' i2' i1 i0'

(e) d12 = i3' i2' i1 i0

(f) d12 = i3 i2 i1' i0'

4) Given a 4x2 priority encoder (where d3 has the highest priority and inputs are in the order d3 d2 d1 d0), what is the output of e1 and e0 given that d0 = 1, d1 = 0, d2 = 1, d3 = 0.

(a) e1 = 0, e0 = 0

(b) e1 = 0, e0 = 1

(c) e1 = 1, e0 = 0

(d) e1 = 1, e0 = 1

(e) The output is unknown since the input combination is invalid for a priority encoder.

5) Given F(a, b, c) = ac + b'c, which of the following is the **inverse of F**?

(a) F' = c'

(b) F' = a'c' + b

(c) F'= a'b + c'

(d) F' = a'c' + bc'

(e) F' = a'b + c

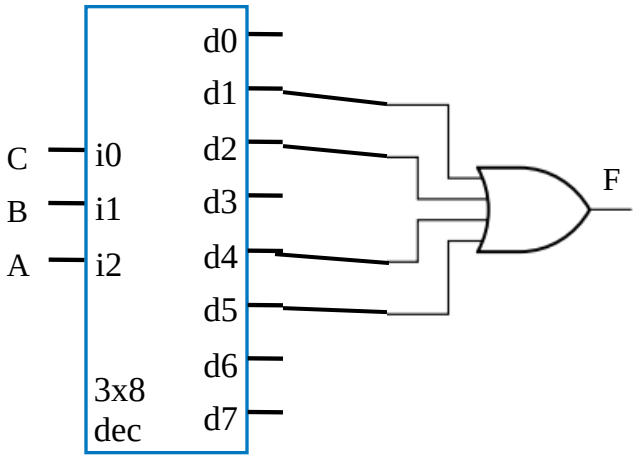
(f) None of the above

6) Given the following logic equation

F = A'B' + A'BC' + B'C + A(B+C)'

Minimize/Simplify using *only* *Boolean algebra*.

7) Given the following circuit using ***3x8 decoder and 4-input OR gate***, write the Boolean equation/expression in a **sum-of-minterm** form.

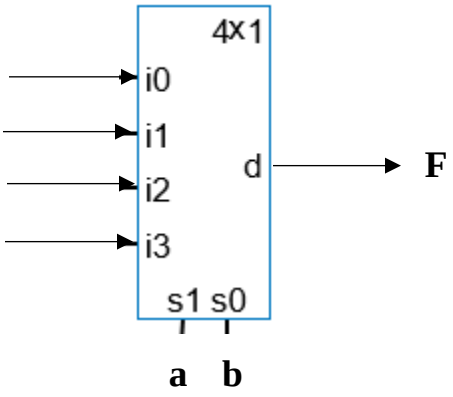


8) Given the following Boolean equation:

$$F(c, d, a, b) = \Sigma(0, 2, 6, 7, 8, 10, 12, 14)$$

8a) Use Karnaugh-map to find its ***minimal*** sum-of-product form.

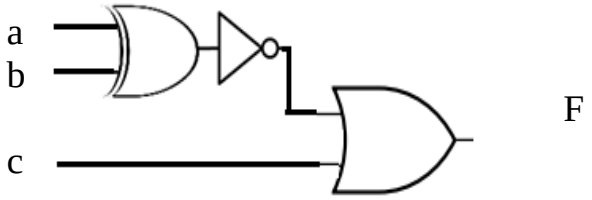
8b) Implement the given equation F(c, d, a, b) using 4x1 MUX with signals a and b connecting to select lines S1 and S0, respectively.



9) Write the ***simplified/minimized sum-of-products*** form for F using **K-map**

F = (x + y + w')(x' + y' + z)(x' + w + z')

10) Given a digital circuit below, implement the circuit above using **only *2-input NAND gates***. Eliminate unnecessary NAND gates.



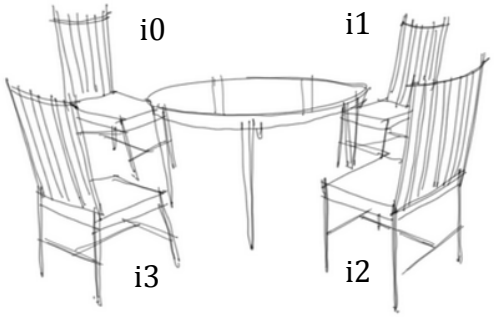
11) Using the combinational logic design process, design a circuit with two 2-bit inputs (A and B) and one 2-bit output (M). Your circuit should output the ***minimum*** of the two input values. For example,

- A =a1a0 = 10 and B = b1b0 = 11, then M = m1m0 = 10

  since 10 (= 2 in decimal) < 11 (= 3 in decimal)
- A =a1a0 = 11 and B = b1b0 = 01, then M = m1m0 = 01
- A = 10 and B = 10, then M = 10 since both inputs are the same value

Your answers must include
a) **Truth table**
b) **minimized** sum-of-products form for the outputs

12) Consider four seats arranged in a circle and described by **Boolean variables i0** to **i3**.



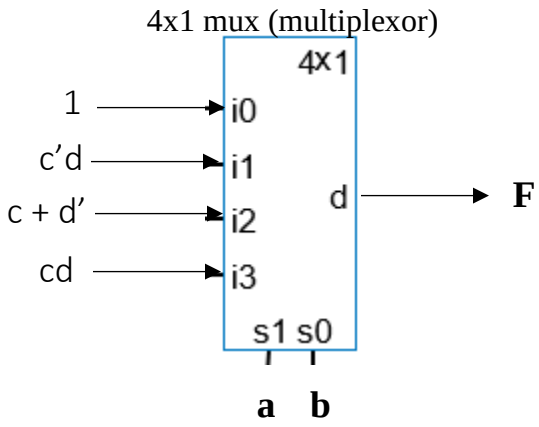
Boolean variable i0 is true (=1) if seat 0 is occupied and i0 is false if the seat is not occupied (no one is sitting in the seat), likewise for i1, i2, and i3.
a) Write a **truth table that is true (F = 1) if <u>at least</u> two people are sitting next to each other and <u>at least</u> one seat is not occupied.**

b) Simplify your design using K-map. Write the expression/equation in minimal sum-of-product form.

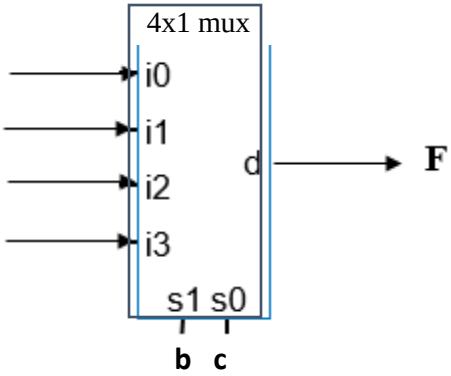
13) A "2-bit" comparator circuit receives **two 2-bit numbers**, A = A_1A_0, and
B = B_1B_0. Design this comparator that produces **an output F = 1 if A ≥ B.**
Write its <u>minimum</u> sum-of-product form.

14) Given the following circuit,

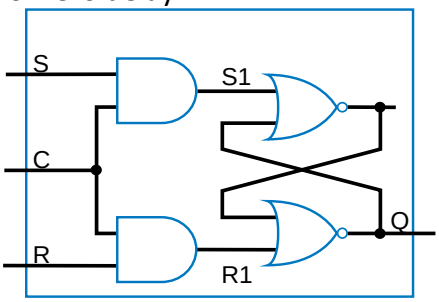
a) write its ***minimized sum-of-products form*** for F

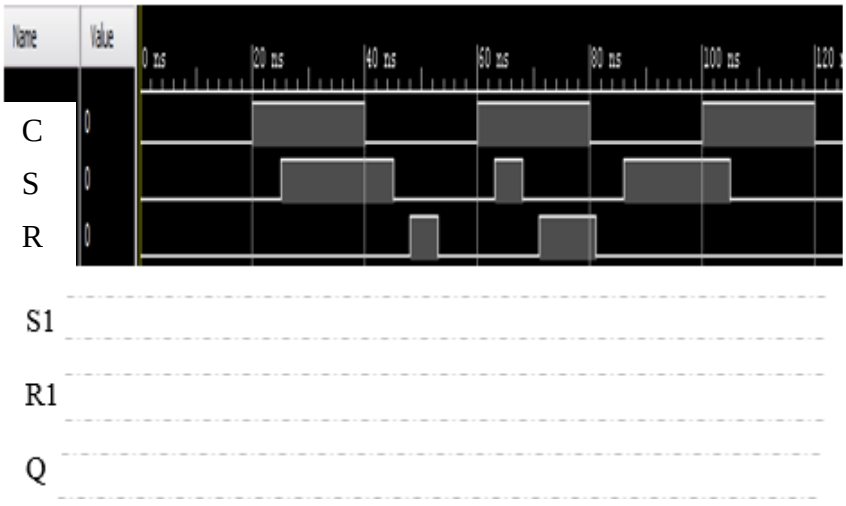


b) Implement the simplified equation of F from 14a) using 4x1 MUX with signals b and c connecting to select lines S1 and S0, respectively, as shown below.

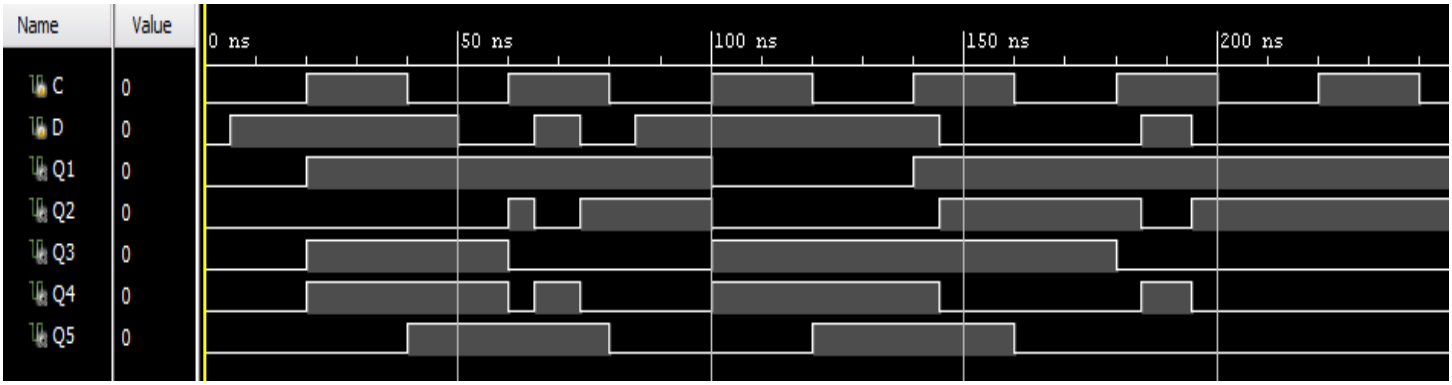


15) Given a level-sensitive SR Latch with the input pattern below, complete the timing diagram below (draw S1, R1, and Q). Assuming that S1, R1, and Q are initially 0 and the logic gates have a *very small* nonzero delay.



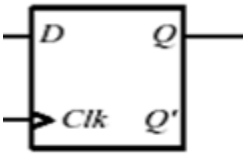


16) Given the following waveform where C and D are inputs and the rest are outputs, which output waveform (Q1, Q2, Q3, Q4, or Q5) belongs to



D-FF using rising edge of Clk

_____
Choose one of Q1, Q2, Q3, Q4, Q5

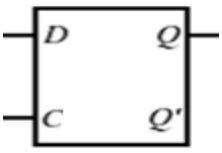


Clk	Q
↑	D

Note: ***C*** and **D** in the ***above waveform*** are connected to ***Clk*** and **D**, respectively of this flip-flop.

D-latch with the function table below

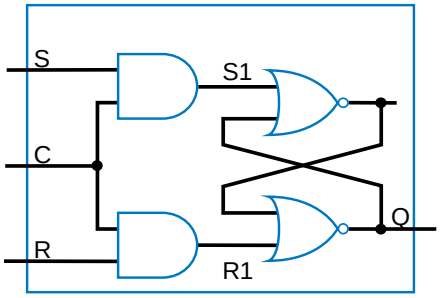
_____
Choose one of Q1, Q2, Q3, Q4, Q5

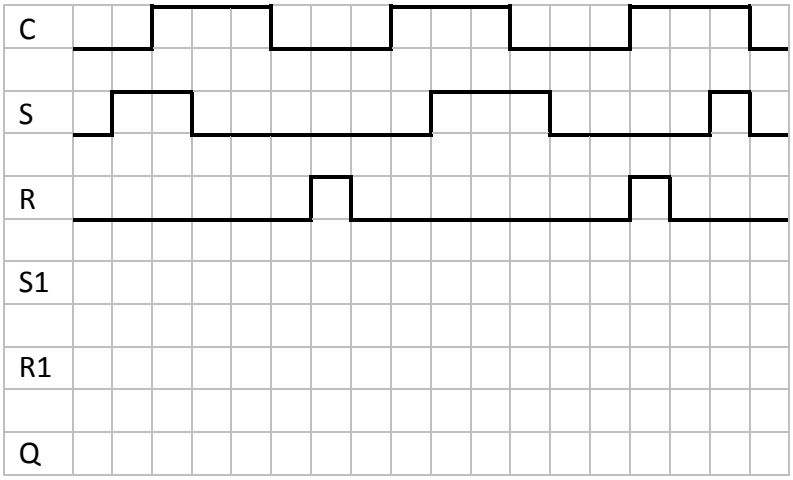


C	Q
1	D
0	Q (stay the same)

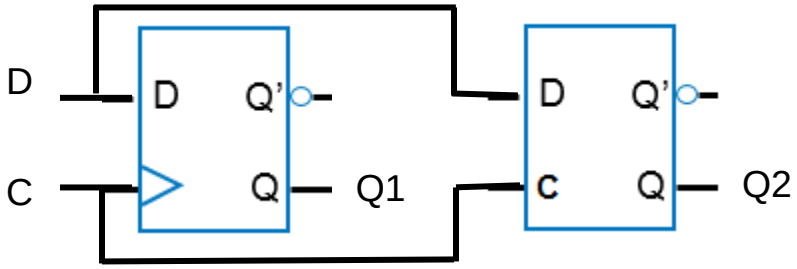
Note: ***C*** and **D** in the ***above waveform*** are connected to ***C*** and **D**, respectively of this latch.

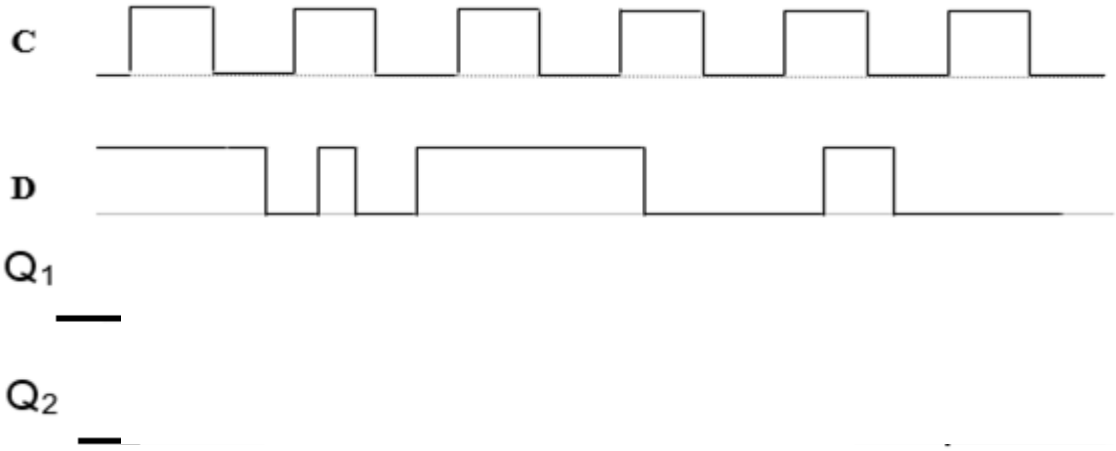
17) Given a level-sensitive SR Latch with the input pattern below, complete the timing diagram below (draw S1, R1, and Q). Assuming that S1, R1, and Q are initially 0



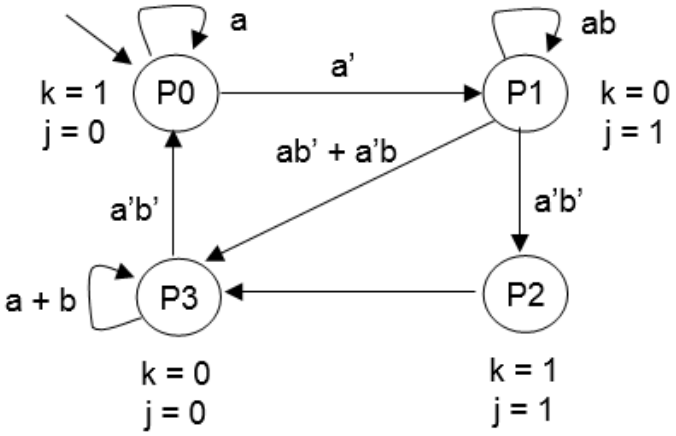


18) Trace the behavior of **D-Latch** and **D flip-flop** for the following input patterns. Assume that Q1 and Q2 is initially 0 and logic gates have a very small nonzero delay.





19) Using the **sequential logic design process**, **convert the provided state diagram (FSM) to a circuit**. Be sure to label and show each step.
Note: **Write the Boolean equations (in minimum sum-of-products form) is sufficient.** *NO need to draw a circuit.*



Inputs: a, b
Outputs: k, j

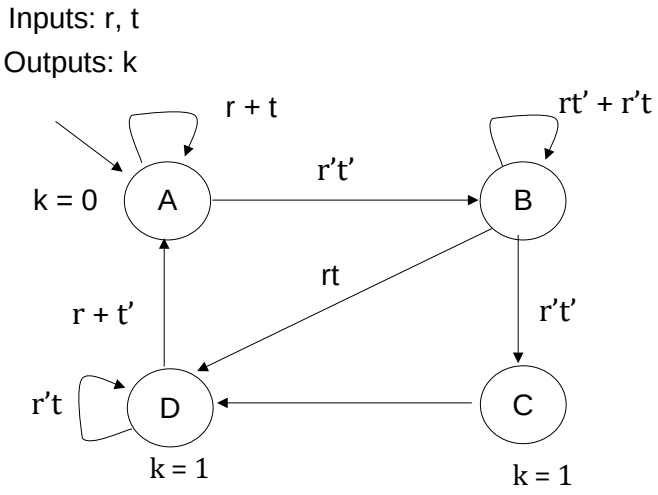
20) Design a synchronous sequential circuit of a sequence detector, which has one input b and one output w. It accepts a sequence of bits (one bit (0 or 1) at a time) and outputs w = 1 when the **target sequence 1001** is detected. ***Non-Overlapping*** *sequence is detected.*

a) Draw its **state diagram**

b) ***Minimum of bits*** to represent/encode states in your designed state diagram are _____

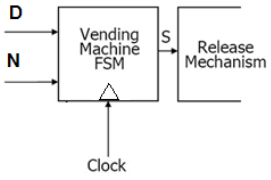
21) Using the sequential logic design process, convert the provided state diagram (FSM) to a circuit. Be sure to label and show each step.

Note: Write the Boolean equations (in minimum sum-of-products form) is sufficient. You DO NOT need to provide a gate-level implementation (no drawing a circuit).



22) Design a vending machine that **delivers coffee after depositing 35 cents**.

There is a single coin slot for two types of coins, N and D.
D is for dimes (10 cents) and N is for nickels (5 cents).
It does not take other coin types. Single coin slot means that you can insert one coin at a time!

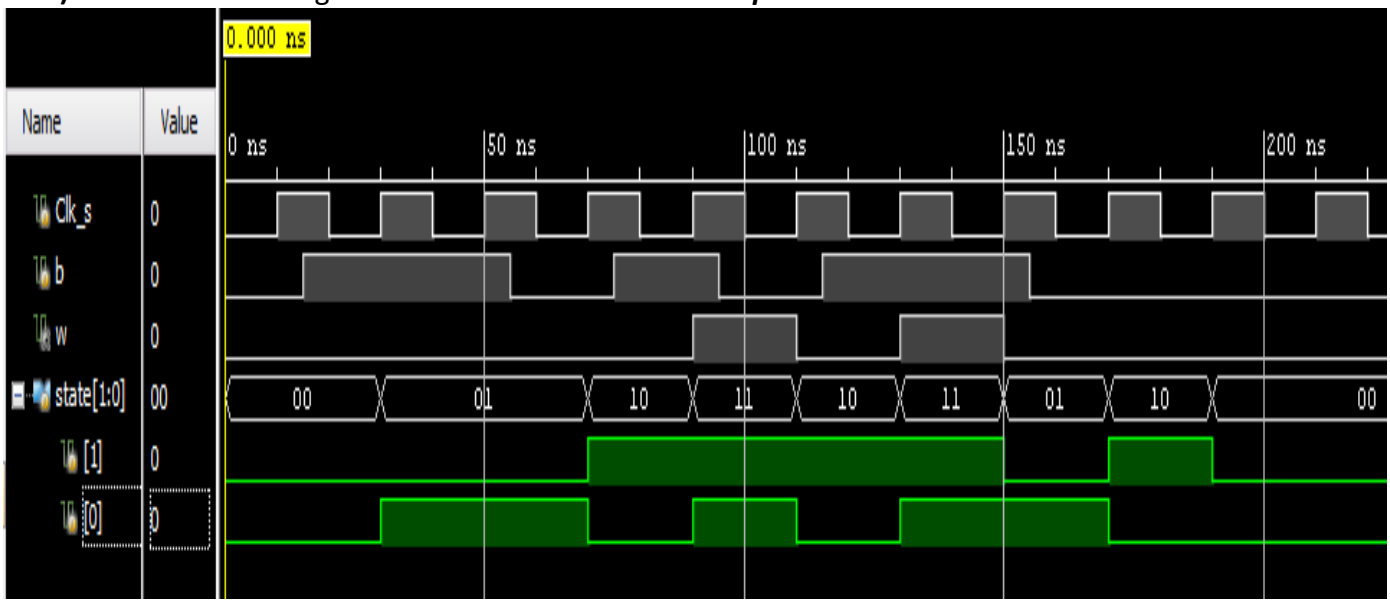


If a dime is deposited, D is 1 and N is 0.
If a nickel is deposited N is 1, D is 0.
N and D cannot be 1 at the same time.
The vending machine does ***not*** return changes if you deposit more than 35 cents.

When 35 cents is reached, coffee is served by outputting S as 1 that enables the coffee dripping system. ***In the next cycle, the vending machine goes back to the initial state for the next coin input for another coffee***.

a) Draw a state diagram (FSM).
b) From your state diagram, what are the minimum of bits that your design needs to use for a state register?

23) Given the following simulation waveform for the ***sequence detector***.



It has one input b and one output w and its state register uses 2 bits (state[1:0]) as shown in the waveform.

a) Draw its state diagram (FSM diagram).

b) What is the target sequence that this detector can detect? (Hint: starting from the initial state (00), find the input sequence such that this detector gives output w = 1.)