First name_ _____ **LASTNAME (in UPPERCASE)** _____

LAB Session (Circle one):

Mon 9-11.50 am Tues 2-4.50 pm Wed 9-11.50 am

Thurs 2-4.50 pm Fri 9-11.50 am Fri 2-4.50 pm

Show your work to receive the credits. Write only answers will get 0 point.

Quiz 2 (10 points): Friday October 12, 2018 (at the beginning of lecture session)

1) (5 pts) Design a circuit that outputs F = 1 when an **absolute value (abs)** of its 8-bit input A (A is an 8-bit signed number using 2's complement format) is less than 30 or greater 85. In other words, if abs(A) < 30 OR abs(A) > 85, F = 1, else F = 0

For example, if A = -100, abs(-100) = 100 =>then F = 1
A = -35, abs(-35) = 35 => then F = 0
A = 54, abs(54) = 54 => then F = 0
A = 99, abs(99) = 99 => then F = 1

Your circuit must be designed such that it works for any given value of 8-bit signed number A.

Assume that you have the following datapath components available ***(unsigned only)***:
8-bit unsigned magnitude comparator(s), 8-bit full adder, muxes (size of your choice) and the n-bit input AND, OR, NOT gates (here "n" is your choice).

Cleary label your components, indicate the input values when necessary, properly connect all components and show bit-width on each wire (if more than 1 bit).

2) (5 pts) Design a **2-bit ALU** using 2-bit adder and muxes for the following operation table:

s1	**s0**	**ALU operation**
0	0	A << 1 filled with 0 (shift A to the left by 1 bit, using 0 to fill the empty position)
0	1	NOT B
1	0	A + B
1	1	A - B

Note: See section 6.6 in your zyBooks for examples.