ECE 274a/ Fall 2016

First name _____ **LAST NAME** _____

LAB Session (Circle one):

Mon 9-12 Tues 8 – 11 Wed 9-12 Fri 9 - 12

Tues 2-5 Thurs 2-5 Fri 2-5

MIDTERM 2 (Version 1): Monday Oct 31, 2016

1. Write your name above. **Circle your lab session!**
   Know your lab session. Circle the wrong session or Not circle it, 1 point will be deducted from your total score.

2. **One-side note sheet is allowed**
3. **No Calculator, No electronic device** (computer, smart/cell phone, …) is allowed
4. To receive credit, show all your work clearly and readably.

   Write only answer gets 0

5. There are 5 pages in this exam.
6. Do not write multiple answers, otherwise, the wrong one will be graded.
7. Ask if you have any questions or confusion.
8. For problem 3, you are responsible for solving one problem (***choose*** 3a or 3b)

Problem	Score	Your score
1	30	
2	30	
3	40	
Total	100	

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1. (30 points)

1a) (10 pts) Using **2's complement format** for signed numbers in 6 bits, fill in the blanks

6-bit signed number	**Decimal**
101010	_____
_____	-12

1b) (10 pts) Given the 6-bit signed numbers (2's complement format), find the result of 100110 – 000111 and state whether an overflow occurs.

100110 – 000111 = _____ (in binary)

Overflow? (circle one) and explain your reason below: Yes No

1c) Given a **32 x 16 register file**,

1c.1 (2 pts) How many bits for W_data and R_data? _____ bits

1c.2 (3 pts) How many bits for W_addr and R_addr? _____ bits

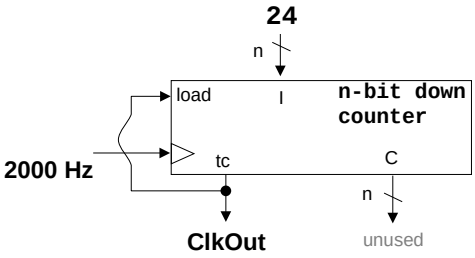
1c.3 (4 pts) What is the size of decoder?

1c.4 (1 pt) The tri-state (three-state) buffers are used with (circle one answer below)

Read port Write port

2) (30 points)

2a) (14 pts) Given the following circuit using an n-bit down counter, answer the questions



2a) What is the *minimum* value of **n**?

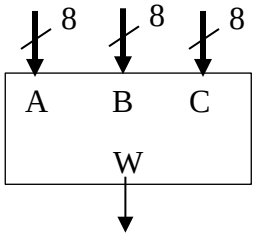
2b) What is the *frequency* (in Hz) of **ClkOut**?

2b) (16 pts) Design a **2-bit ALU** using 2-bit adder and muxes for the following operation table

s1	**s0**	**ALU operation**
0	0	A << 1 filled with 0
0	1	NOT B
1	0	A + B
1	1	A - B

READ ME: For problem 3, choose 1 problem to complete
(pick Problem **3a <u>or</u> 3b**)
10 bonus points if you can complete both 3a and 3b with 100% correct answers

3a) (40 points) Given three 8-bit unsigned inputs A, B, C, design a circuit that outputs 1 if the **smallest** *absolute* distance between any pair of values is less than 15 or greater than 50.



Note: your circuit must work for any 8-bit unsigned numbers given in A, B, C.
- Assume that you have the following Datapath components available (***unsigned*** only) – decoders, encoders, muxes, parallel load registers, adders, subtractors, magnitude comparators, array style multipliers, shifters, and logic gates (NOT, AND, OR, NAND, NOR, … for any *n* inputs (*n* is your choice)).
- Properly connect all components and indicate bit-width of each wire (if more than 1 bit).

Ex 1: If A = 108, B = 53 and C = 27, absolute distance between A and B = |A-B| or |B-A| = 55
absolute distance between A and C = 81
absolute distance between B and C = 26
Since the smallest absolute distance is 26 which is NOT less than 15 or greater than 50, the output W = 0.

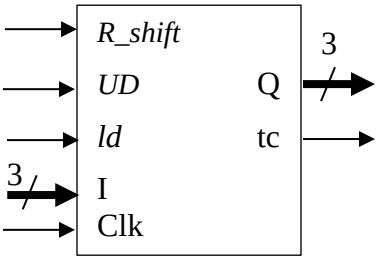
Ex 2: If A = 18, B = 25 and C = 72, absolute distance between A and B = |A-B| or |B-A| = 7
absolute distance between A and C = 54
absolute distance between B and C = 47
Since the smallest absolute distance is 7 which is less than 15, the 1-bit output W = 1.

Reminder: You are responsible for solving only one problem (pick 3a or 3b)

3b) (40 points) **Design** a **3-bit up/down-counter** that has the following control inputs:

- *R_shift* shifts its counter value to the right,
- *UD* enables counting up or down (UD = 1 for up),
- *ld* loads value I to the counter

The counter has 3-bit "Q" as the counter output and 1-bit terminal count (tc) output as shown in the block diagram on the right-hand side.



The *order of operation* from *highest to lowest priority* is *ld*, *R_shift*, *UD*. The operation table is given below:

ld	***R_shift***	***UD***	**Q**
1	x	x	I
0	1	0	maintain
0	1	1	Shift Q to the right by 1 position filled with 0
0	0	1	Q + 1 (count up)
0	0	0	Q - 1 (count down)

Properly connect all components and indicate bit-width of each wire (if more than 1 bit).

Assume that you have the following datapath components available (**unsigned** only): decoders, encoders, muxes, 3-bit parallel load registers, 3-bit magnitude comparators, 3-bit adders, 3-bit subtractors, 1-bit left shifter (use symbol << 1), 1-bit right shifter (use >> 1),and logic gates (NOT, AND, OR, NAND, NOR, … for any *n* inputs (*n* is your choice)).