**Lab 5: 32-bit Single-cycle Datapath and Controller Design**

**Overview:** In a series of laboratory exercises you will incrementally implement a 32-bit processor that supports a basic set of operations. In Task 0, you implement the datapath components required by the processor. In Task 1, you put together a datapath using these components and implement the controller that controls this datapath. Datapath will be configured by the controller to execute a specific operation in a single clock cycle. This way the datapath will be able to execute different operations in each cycle. You will eventually execute matrix multiplication code on your datapath to validate the functionality of your datapath.

**Lab 5 schedule overview**

|  |  |  |  |
| --- | --- | --- | --- |
|  | **Score** | **Start date** | **Due date** |
| Task 0 | 125 points | Week of  Oct 22 – Oct 26 | The first 60 minutes of your lab session during the week of Oct 29 – Nov 2, 2018 |
| Pre-lab of Task 1 |  | Week of  Oct 29 – Nov 2 | The first 30 minutes of your lab session during the week of Nov 5- Nov 9, 2018 |
| Task 1 | 325 points | As soon as you finish Task 0 | By 4.45 pm on Friday Nov 16th, 2018 |
| **Task 2** | **150 points** | **As soon as you finish Task 1** | **By 4.45 pm on Thursday Nov 29th, 2018** |
| Task 3 | 100 points | As soon as you finish Task 2 | By 11.45 am on Wednesday May 2nd, 2018 |
| **Total** | **700 points** |  |  |

**Lab 5 - Task 2 (150 points)**

**Starts:**  as soon as you finish Task 1

**Demo:** See below

**Due date:** see the table above

**References:**

* Lecture Notes: Verilog ppt slides and Verilog chapter on Zybook
* “single\_cycle\_datapth\_Task1” on D2L under Lab 5
* “single\_cycle\_datapth\_Task2” on D2L under Lab 5

**Objectives:**

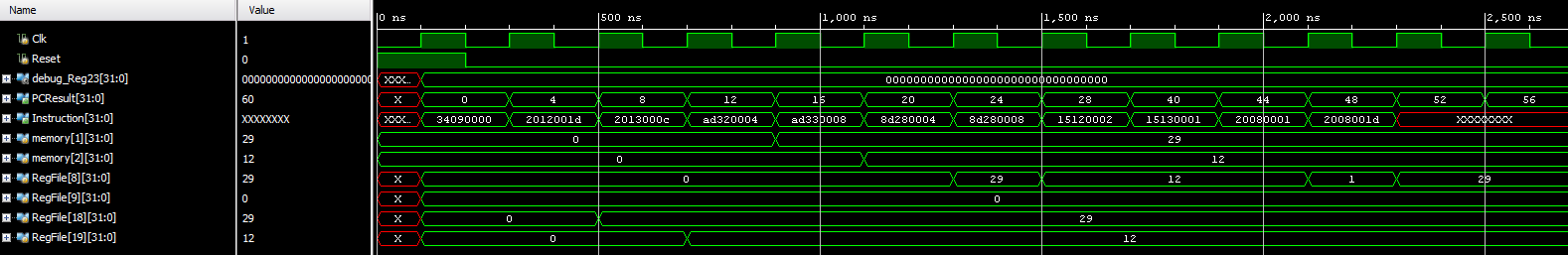
* Continue implementing more instructions in the single-cycle processor
* Use the processor to execute a set of given instructions
* Continue using the ***post-synthesis simulation*** for your design

**Assignments for Lab 5 Task 2:**

* Download “task2\_lw\_sw\_bne\_type” folder and “single\_cycle\_datapth\_Task2” ppt slides.
* (10 pts) Complete slides 4 and 7 of the PowerPoint slides *single\_cycle\_datapth\_Task2*. Show your work to your TA before you start the next steps below. Why? If this is wrong, your code will be wrong.
* Follow slide 8 of the PPT slides ***single\_cycle\_datapth\_Task2*** to complete all the tasks for Task 2.
* **(90 pts)** Demo the working Behavioral simulation to your TA. See Figure 1 (next page) for the working behavioral simulation waveform
* **(50 pts)** Demo the working Post-Synthesis simulation to your TA. See Figure 2 (next page) for the working Post-Synthesis simulation waveform

Note: See point distribution on slide 10 of the PPT slides ***single\_cycle\_datapth\_Task2.***

Figure 1: Behavioral Simulation



Note: **RegFile[8] is the main outputs that we want to look at**. Also

Reg[8] still changes to 29 at the same time

* show RegFile[9], [18], [19] on your waveform
* memory[1] and [2] from Data memory

Reg[19] still changes to 0xc at the same time

* Address[31:0] from ProgramCounter

Reg[18] still changes to 0x1d at 500 ns

* Instruction[31:0] from InstructionMemory

Figure 2: Post-synthesis Simulation

