**LASTNAME:** SHENGRUI, First name: Zhang

**LAB Session:** Fri 2-4.50 pm

**Show your work to receive the credits. Write only answers will get 0 point.**

**Quiz 1 (10 points):** Monday September 24, 2018 (at the beginning of the lecture session)

1. Draw a state diagram of a sequence detector, which has one input b and one output w, that accepts a sequence of bits (one bit (0 or 1) at a time) and outputs 1 when target sequences have been detected. The circuit outputs w = 1 when the previous four values of b were **1010** (target sequence). Overlapping sequence needs to be detected.

Note: Your circuit should also have an active-high synchronous reset (Rst).

b 100**101010**0**1010**00**101010**

w 000000**1**0**1**0000**1**00000**1**0**1**

1. Utilize the sequential design process to convert your state diagram to the circuit. Be sure to label and show each step within the sequential design process. Write all Boolean equations.