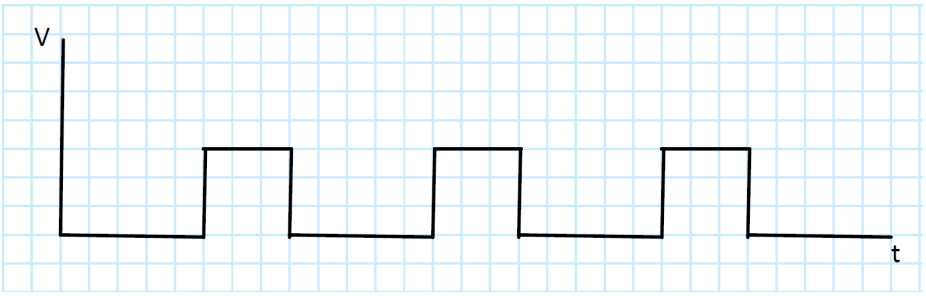
ECE 372A
Sample Exam 2c - with solutions

1. The duty cycle of a signal given below is:



a. 62.5 %

b. 40 %

c. 37.5 %

d. 22.5%

2. If you vary a signal between 0V and 5V and the effective voltage measured using a voltmeter is 3V, then the duty cycle is:

a. 20%

b. 60%

c. 80%

d. 40%

3. The PWM functionality is accomplished using the output compare modules within the Timer Systems.

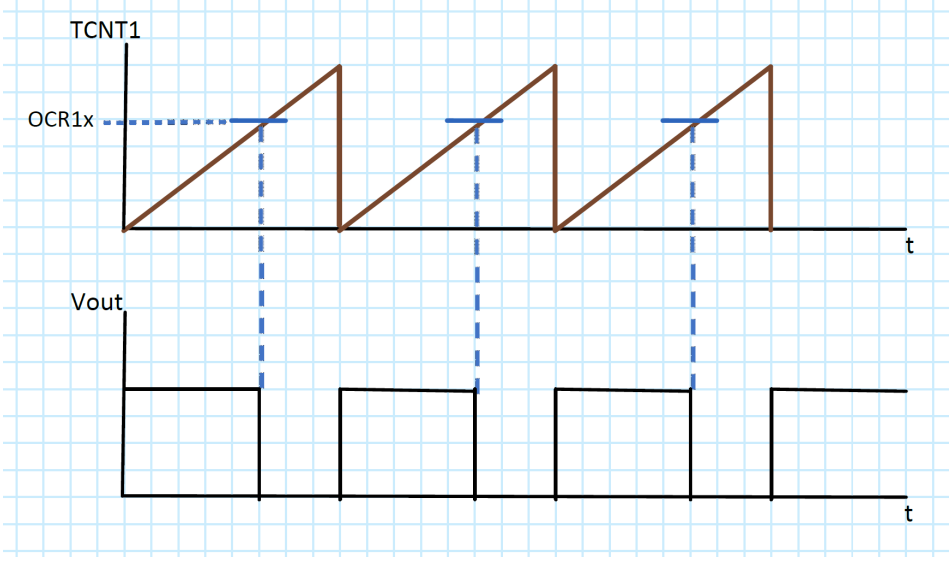
a. TRUE

b. FALSE

4. The following diagram is an example of non-inverting mode PWM for Timer 1

a. TRUE

b. FALSE



5. For Timer 1 using fast PWM 9-bit mode, a pre-scaler divider of 8 and a I/O clock frequency of 16 Mhz, what is the waveform frequency?

   a. 31250 Hz

   b. 2 Mhz

   c. 15625 Hz

   d. 3906 Hz

6. To generate a waveform with duty cycle of 75% in non-inverted mode using Timer 1 with fast PWM 10-bit mode, what is the value of OCR1A?

   a. 383

   b. 767

   c. 256

   d. 1023

7. Timer 1 is configured with fast PWM 8-bit mode, non-inverting output and a prescaler divider of 8. The I/O clock frequency is 16 Mhz. What is the waveform frequency and value of OCRA1 is needed to achieve a duty cycle of 65%?

   a. f = 62500 Hz, OCR1A = 191

   b. f = 7812 Hz, OCR1A = 191

   c. f = 62500 Hz, OCR1A = 100

   d. f = 7812 Hz, OCR1A = 165

8. The lower the duty cycle, the greater the average voltage applied to a dc motor which results in a higher rotational speed for the motor

   a. True

   b. False

9. A program you inherited uses Fast PWM mode with the value in OCR1A set to the TOP value. You are checking the software to ensure that the register bits for WGM13, WGM12, WGM11, and WGM10 are set correctly and that OCR1A has the correct value to generate a waveform frequency of 10 kHz. You've already determined that the prescaler divider is 8 and the I/O clock frequency is 16 MHz. The WGM bits and OCR1A should read:

   a. WGM13 = 1, WGM12 = 1, WGM11 = 1, WGM10 = 1, OCR1A = 199
   b. WGM13 = 1, WGM12 = 1, WGM11 = 1, WGM10 = 0, OCR1A = 450
   c. WGM13 = 0, WGM12 = 1, WGM11 = 0, WGM10 = 0, OCR1A = 200
   d. WGM13 = 1, WGM12 = 1, WGM11 = 1, WGM10 = 1, OCR1A = 56

10. Calculate OCR1A to generate a wave with a frequency of 20 kHz for the following Timer 1 PWM configuration: Mode 15, Non-inverting output, Prescaler divider = 8, I/O clock frequency = 16Mhz.

    a. OCR1A = 100
    b. OCR1A = 13
    c. OCR1A = 799
    d. OCR1A = 99

11. An ADC that can digitize 4096 different levels has what bit-depth?

    a. 10
    b. 16
    c. 8
    d. 12

12. If we have a 16-bit ADC, V_high = 5V, V_low = 0 V, what is the resolution?

    a. 312 µV
    b. 76 µV
    c. 76 mV
    d. 7 µV

13. An analog input signal has a maximum frequency component of 20 kHz. What is the minimum sampling frequency that the ADC should be set at so that all bandwidth information is digitized?

    a. 100 kHz
    b. 80kHz
    c. 40 kHz
    d. 20 kHz

14. When reading the result from the ADC in a right justified format, register ADCH should be read before ADCL.

    a. TRUE
    b. FALSE

15. Which line of code will set the autotrigger source selection in ADC module to "Free Running" mode?

    a. ADCSRB &= ~(1 << ADTS2 | 1 << ADTS1 | 1 << ADTS0);
    b. ADCSRB |= (1 << ADTS2 | 1 << ADTS1 | 1 << ADTS0);
    c. ADCSRA &= ~(1 << ADEN);
    d. ADCSRA |= (1 << ADEN | 1 << ADSC | 1 << ADATE);

16. How long does a normal ADC single conversion take when the system clock is 16 Mhz and the prescaler bits ADPS2:0 are all set to 1 in the ADCSRA Control and Status Register?

    a. 100 ms
    b. 300 μs
    c. 104 μs
    d. 65 μs

17. What is the correct line of code to disable the digital input for an ADC pin A14 on the Arduino board? (hint: refer to the Arduino schematic as a starting point)

    a. DIDR0 |= (1 << ADC0D);

    b. DIDR2 |= (1 << ADC14D);

    c. ADCSRA &= ~(1 << ADEN);

    d. DIDR2 |= (1 << ADC8D);

18. What are the correct lines of code to set the reference voltage to VCC for an ADC conversion?

    a. ADMUX |= (1 << REFS0);
    ADMUX &= ~(1 << REFS1);

    b. ADMUX &= ~(1 << REFS0);
    ADMUX &= ~(1 << REFS1);

    c. ADMUX |= (1 << REFS0);
    ADMUX |= (1 << REFS1);

19. I2C serial communication protocol is considered:

    a. Full duplex, asynchronous

    b. Half duplex, synchronous

    c. Half duplex, asynchronous

    d. Full duplex, synchronous

20. If the USART if configured to work in an 8-O-1 configuration and the data that is sent in binary is 0b01101101, what should the value of the parity bit be:

    e. 1

    f. 0

    g. There is no parity bit

21. It is desired to transmit serial data at 9600 Baud rate using the ATMEGA 2560 USART module in asynchronous normal mode. The frequency of the system is 16 MHz. Determine the % error that occurs due to the fact that UBRR0 can only be a whole number.

h. 2.20%
i. 0.99%
j. 0.16%
k. 1.15%

22. For I2C protocol, the SLAVE is responsible for generating the acknowledge signal upon receiving a write operation

a. TRUE
b. FALSE

23. In I2C, the START and STOP conditions are uniquely signaled by changing the level of the SDA line when the SCL line is low.

a. TRUE
b. FALSE

24. Organize the steps in the box below to show the sequence involved in a Master Read using I2C protocol

b. 2 1 3 5 8 4 6 7
c. 2 5 3 4 8 6 1 7
d. 2 5 3 6 8 1 4 7

1. Master reads data byte sent from Slave sensor module
2. Master sends a start sequence.
3. Master sends Internal address of the sensor module that needs to be read and checks for ACK.
4. Master sends a Not Acknowledge (NACK)
5. Master sends I2C address of the sensor module with the R/W bit low and checks for ACK.
6. Master sends a repeated start sequence.
7. Master sends the stop sequence.
8. Master sends I2C address of the sensor module with the R/W bit high and checks for ACK.

25. For the I2C transmission shown below by the Master, determine the SLAVE address and whether it is a read or write operation. The numbering shows the 1st , 2nd , 3rd …… 8th clock cycle.

a. 0x53, Write

b. 0xD3, Read

c. 0xA6, Write

d. 0x65, Read