PWM Section

- Know what duty cycle means
- Know primary modes of operation for PWM (Table Modes 1-15)
  - Fast PWM 8 bit, 9 bit, 10 bit and TOP VALUE OCRnA (table 17-2)
- How to calculate duty cycle, PWM frequency using formula.
- Know how to initialize Timer for PWM mode
  - Initial WGM bits
  - Non-inverting vs inverting (COM bits)
  - Select prescaler bits CS bits
  - Set the pin on the Dev. Board for output DDR regsister (look on schematic)
  - Calculate OCRnA to set the duty.
    - Duty cycle ~= OCRnA/TOPValue

ADC

- Know bit depth means and how that translates to # of levels
- Know how to determine resolution of the ADC
  - Resolution = Full scale voltage range/# of levels
- Know how to initialize the ADC module
  - MUX bits – set the ADC channel.
  - ADEN bit – enable for specific VREF and the ADC channel turned on
  - Choose VREF – VCC
  - If using auto trigger – ADATE bit set, determine the type of Auto trigger mode
    - Free running, Output Compare from Timer, External interrupt (INT)
  - Disable the digital input to ADC channel (DIDRn register)
  - Start the conversion ADSC bit
  - Note : if using the external interrupt, you have toenable the ADIE bit and then ISR Vector table and enable sei and write an ISR code.
  - Set the justify bit (L justify or Right justify)
  - Set the prescaler bits
- Know how to read the digitized ouput from the ADC registers
  - ADCL first followed by ADCH (if doing 10 bit number)
- How long it takes to do one conversion – 13 ADC clock
- Nyquist sampling rate – 2 x highest frequency of info.

Serial Communication

- Know difference between asynchronous, synchronous, half duplex and full duplex
- How the protocol that we have discussed maps into these terms
  - I2C – synchronous, half duplex
  - RS232 – asynchronous, full duplex
  - SPI – synchronous , full duplex

USART module

- Know how to calculate bit error rate.
  - Baud rate of 9600. use formula to determine the UBRRn (note that it will be a fractional number). Then use the formula for Baud rate with your UBRRn and you will get a different value.
  - Bit error rate = (Actual baud rate – ideal baud rate)/ ideal baud rate
- Know how to set the parity bit
  - Even parity (8 bit of data) add up all the ones in the data set and then use the parity bit to make the all the number of ones add up to an even number.
    - 0b 01110001 - how many ones are there? 4 (already even) parity bit is a 0.
    - 0b 11101010 - how many ones are there? 5 (odd) parity bit is a 1 to make the total number even.

I2C module

- Know general concept
- Know what a start and stop condition looks like
  - Start condition data line goes low while the clock line is high
  - Stop condition data line goes high while the clock line is high
- Know the sequence to read data from a slave device
  - Start condition
  - Call up the device address (7 bit address), followed by write bit, wait for ACK
  - Master will send the device the internal memory address with write bit, wait for ACK
  - Restart condition
  - Master will send the device address, followed by read bit, wait for ACK
  - Slave will send data to MASTER, master will ACK until it is done reading and then MASTER will not ACKNOWLEDGE.
  - MASTER will send stop condition.