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基于Zynq的边缘检测滤波

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Sobel算法简介

PART ONE　Sobel算法简介

边缘检测是通过检测图像亮度上的差别,增强图像中的边界特征,确定图像的边缘信息。 图像处理中用幅值和方向属性描述图像边缘。

RGB[23:0]-->G[7:0]

−1	0	1
−2	0	2
−1	0	1

(a)

1	2	1
0	0	0
−1	−2	−1

(b)

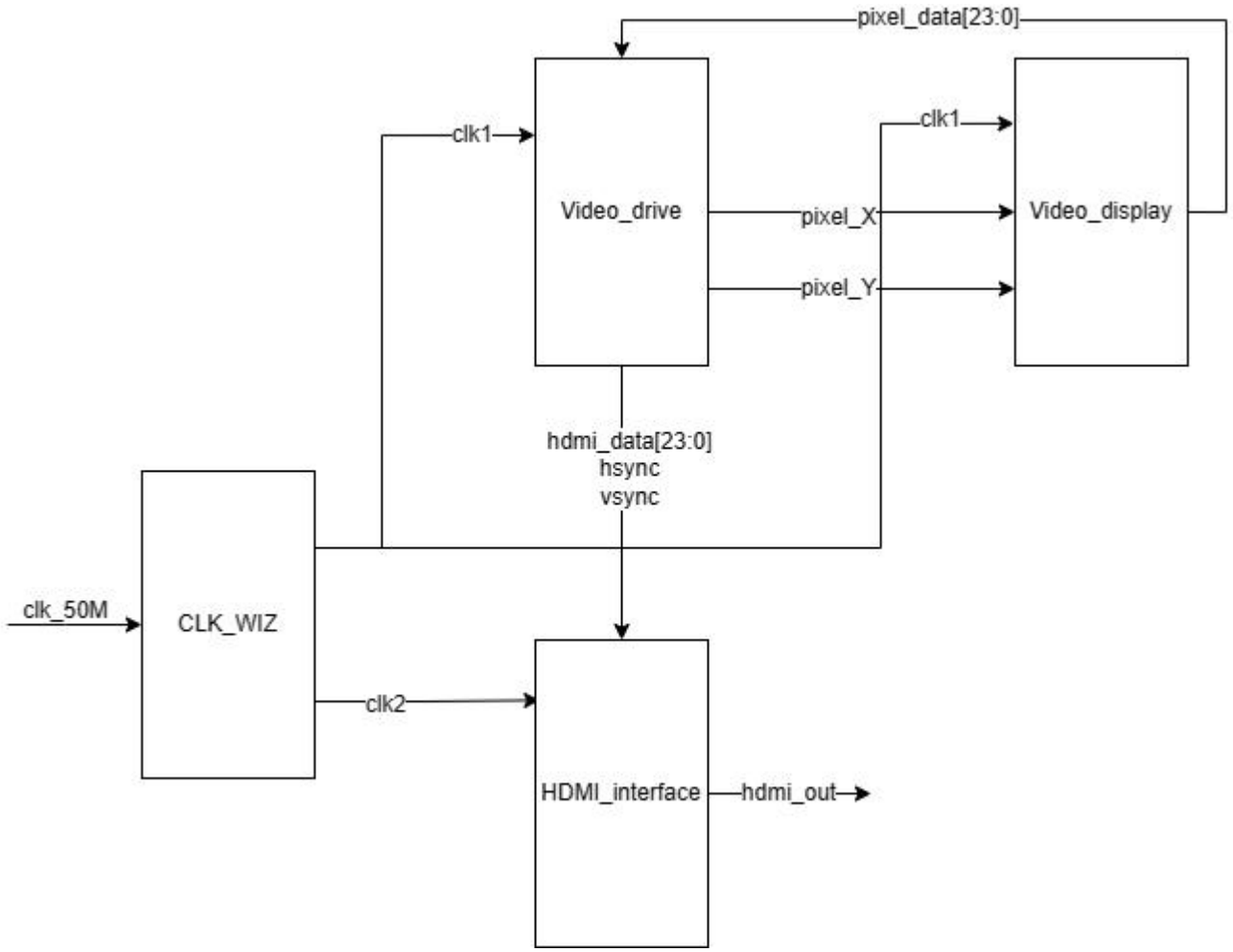
$$G=\sqrt{a^2+b^2}$$

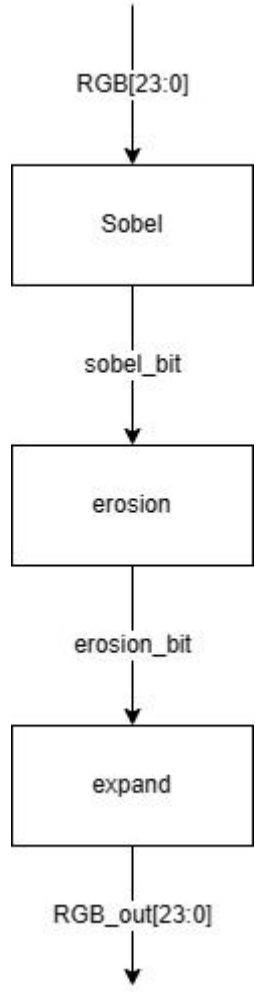
$$G\_Soebl=\begin{cases}1(G>\text{阈值})\\0(G<\text{阈值})\end{cases}$$

PART TWO

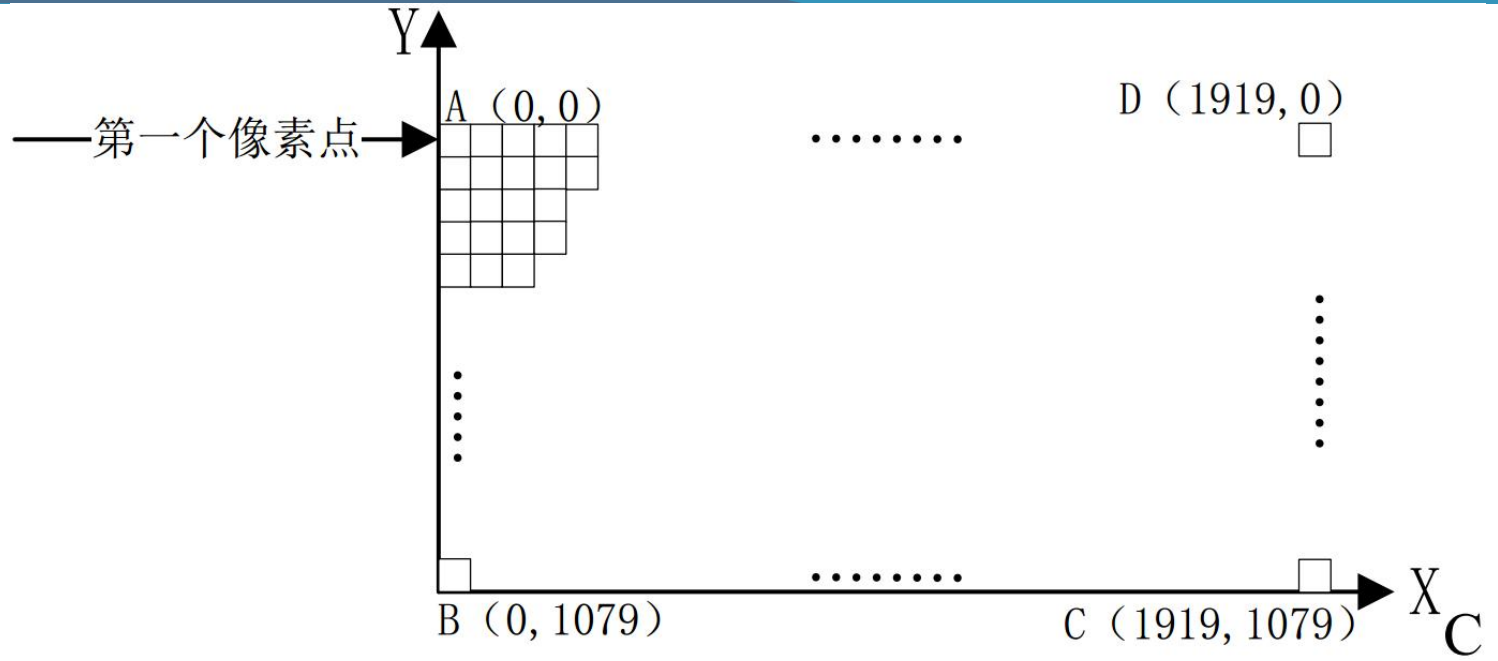
Sobel滤波实现

PART TWO 顶层设计





PART TWO Sobel滤波器实现



像素的寄存器:

```
reg [7:0] line1[199:0];
reg [7:0] line2[199:0];
reg [7:0] p0;
reg [7:0] p1;
```

3x3卷积 → 比较阈值 → 二值化

PART THREE

Sobel滤波器优化与ASIC综合

PART THREE 滤波器优化

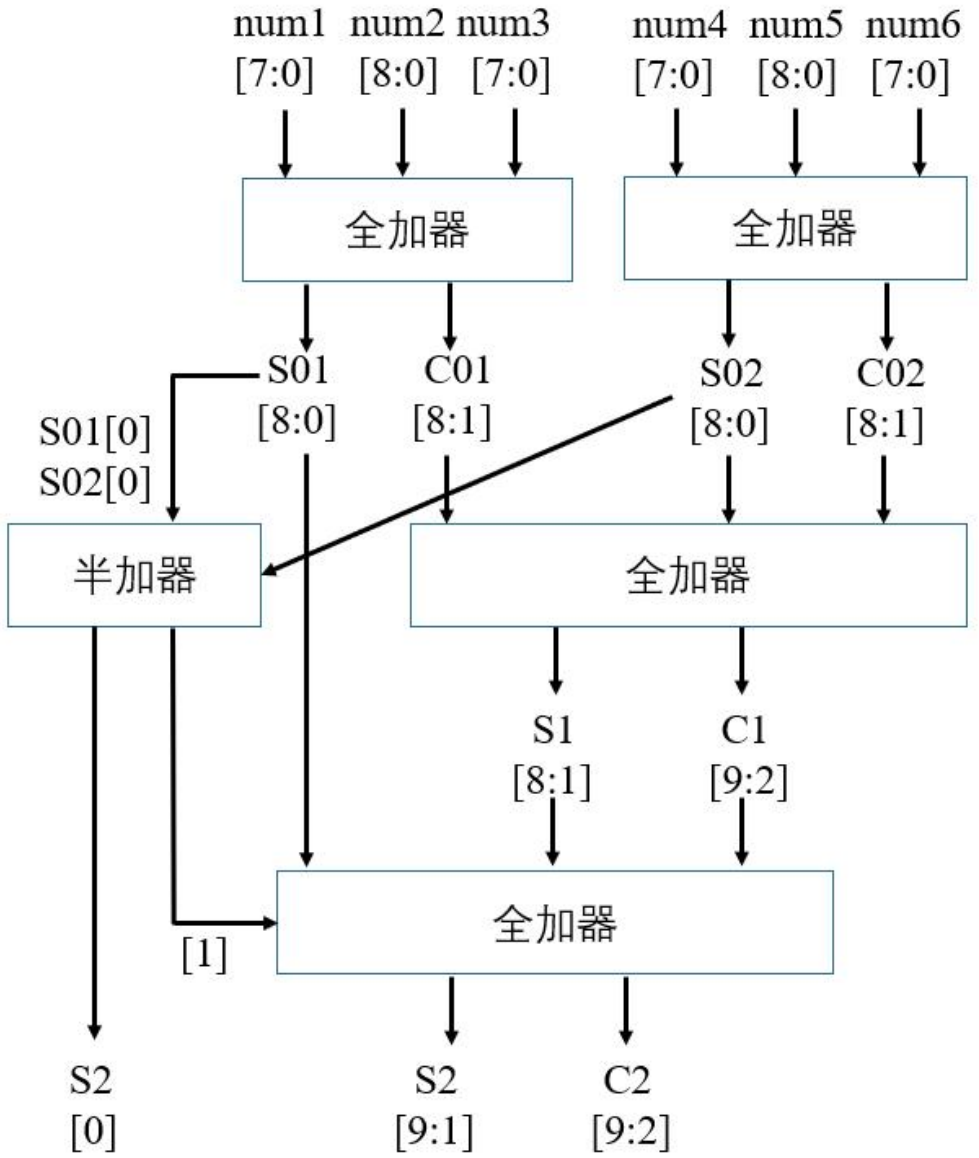
Sobel滤波器加法：num1[7:0]+2*num2[7:0]+num3[7:0]-num4[7:0]-2*num5[7:0]-num6[7:0]

优化原理：
第一步： num4，num5，num6取补码；
num=~num+1；

第二步：num2，num5左移一位；

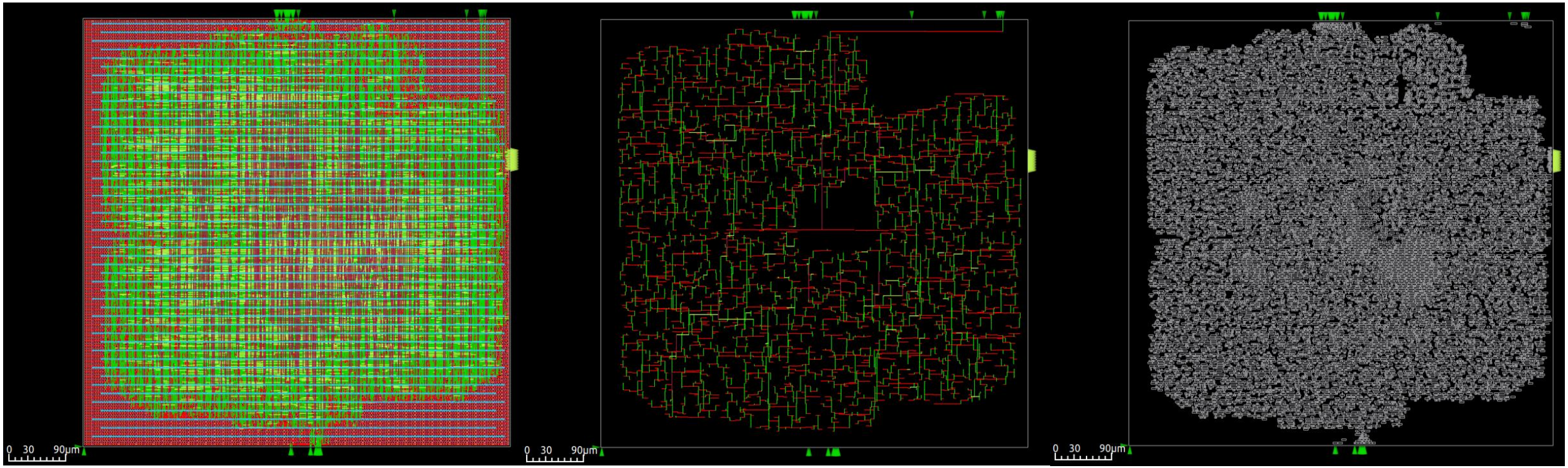
第三步：将6组数压缩为2组数；

第四步：八位加法器采用CLA结构进行加法计算。



PART THREE ASIC综合

Filter:



final_routing　　final_clocks　　final_placement

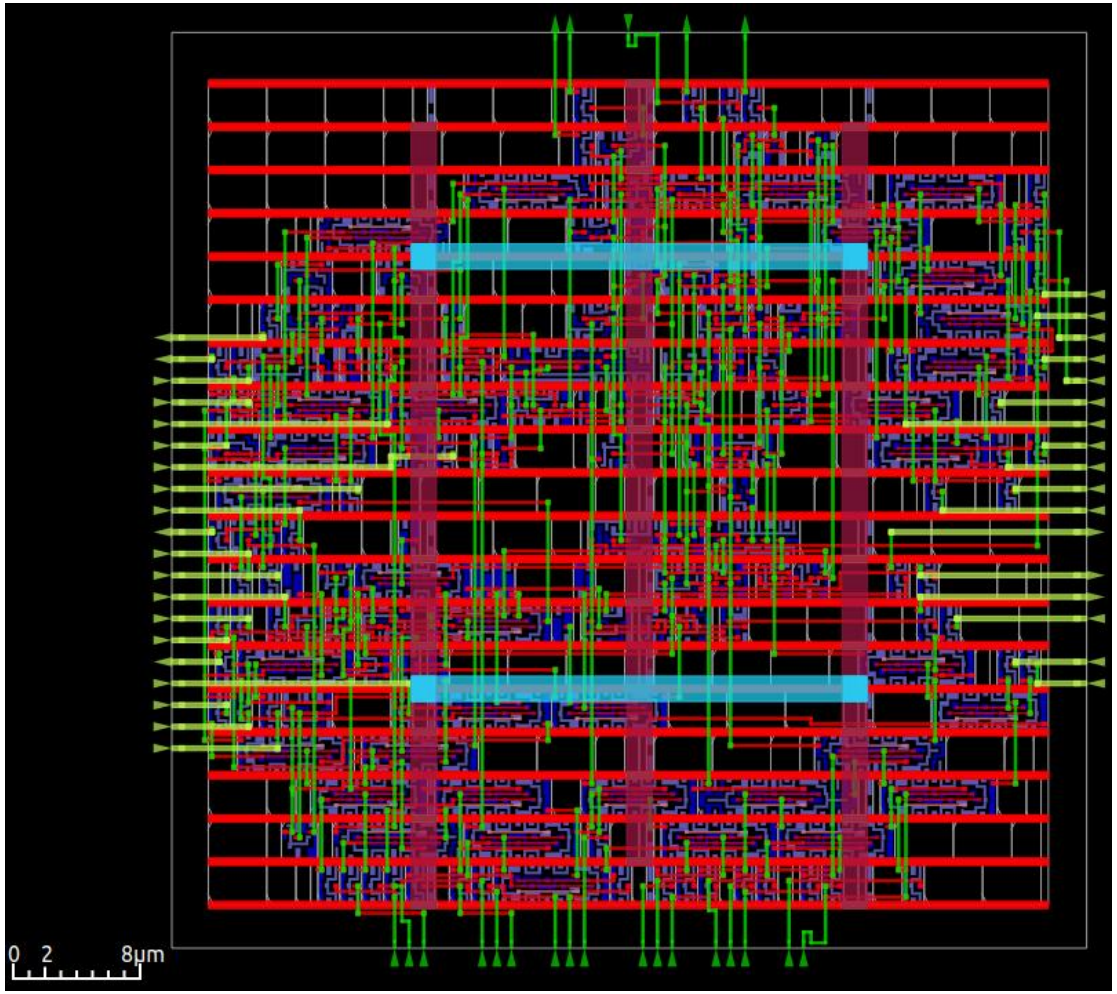
PART THREE ASIC综合

```
finish report_checks -path_delay max
--------------------------------------------------------------------------------
Startpoint: pixel_x[2] (input port clocked by core_clock)
Endpoint: _34781_ (rising edge-triggered flip-flop clocked by core_clock)
--------------------------------------------------------------------------------
                          5.99   data required time
                         -10.10   data arrival time
                         -4.12   slack (VIOLATED)
finish report_power
--------------------------------------------------------------------------------
Group            Internal  Switching    Leakage      Total
                 Power     Power        Power        Power (Watts)
----------------------------------------------------------------
Sequential       3.15e-02  1.91e-03   2.74e-08   3.34e-02  34.0%
Combinational    2.35e-02  4.15e-02   5.64e-08   6.50e-02  66.0%
Macro            0.00e+00  0.00e+00   0.00e+00   0.00e+00   0.0%
Pad              0.00e+00  0.00e+00   0.00e+00   0.00e+00   0.0%
----------------------------------------------------------------
Total            5.50e-02  4.34e-02   8.38e-08   9.84e-02 100.0%
                 55.9%     44.1%      0.0%
================================================================
finish report_design_area
--------------------------------------------------------------------------------
Design area 223133 u^2 48% utilization.
```

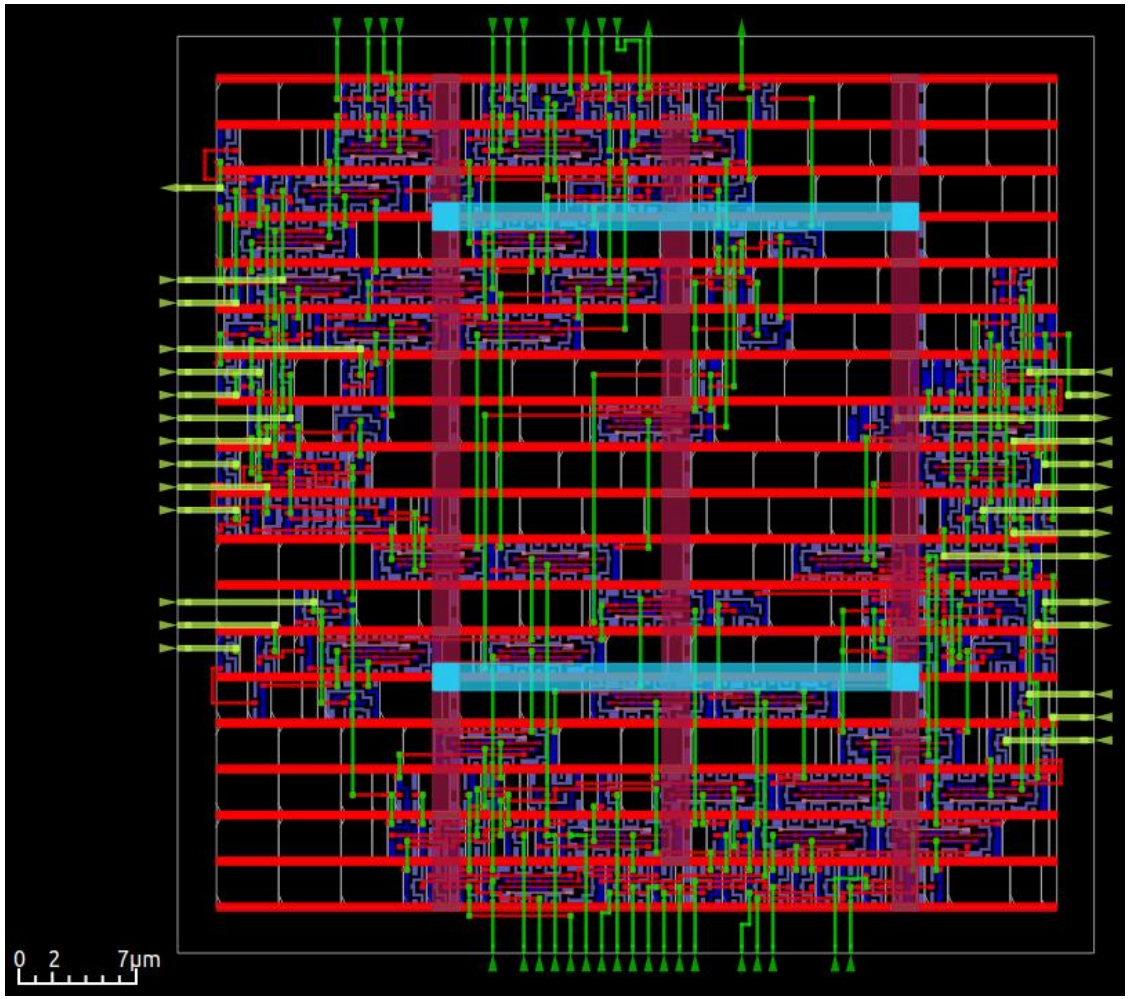
```
finish report_checks -path_delay max
--------------------------------------------------------------------------------
Startpoint: pixel_x[2] (input port clocked by core_clock)
Endpoint: _34105_ (rising edge-triggered flip-flop clocked by core_clock)
--------------------------------------------------------------------------------
                          41.46   data required time
                          -19.27   data arrival time
                          22.19   slack (MET)
finish report_power
--------------------------------------------------------------------------------
Group            Internal  Switching    Leakage      Total
                 Power     Power        Power        Power (Watts)
----------------------------------------------------------------
Sequential       3.43e-03  1.64e-04   2.74e-08   3.59e-03  44.0%
Combinational    1.47e-03  3.09e-03   5.09e-08   4.57e-03  56.0%
Macro            0.00e+00  0.00e+00   0.00e+00   0.00e+00   0.0%
Pad              0.00e+00  0.00e+00   0.00e+00   0.00e+00   0.0%
----------------------------------------------------------------
Total            4.90e-03  3.26e-03   7.83e-08   8.16e-03 100.0%
                 60.1%     39.9%      0.0%
================================================================
finish report_design_area
--------------------------------------------------------------------------------
Design area 212265 u^2 47% utilization.
```

Modify the clock period!

PART THREE ASIC综合



优化前adder



优化后adder

PART THREE ASIC综合

```
finish report_checks -path_delay max
--------------------------------------------------------------------------------
Startpoint: num4[0] (input port clocked by core_clock)
Endpoint: add[9] (output port clocked by core_clock)
--------------------------------------------------------------------------------
                         32.00   data required time
                        -12.97   data arrival time
--------------------------------------------------------------------------------
                         19.03   slack (MET)
finish report_power
--------------------------------------------------------------------------------
Group            Internal  Switching    Leakage      Total
                 Power     Power        Power        Power (Watts)
----------------------------------------------------------------
Sequential       0.00e+00  0.00e+00     0.00e+00     0.00e+00   0.0%
Combinational    2.43e-05  2.48e-05     4.88e-10     4.90e-05   100.0%
Macro            0.00e+00  0.00e+00     0.00e+00     0.00e+00   0.0%
Pad              0.00e+00  0.00e+00     0.00e+00     0.00e+00   0.0%
----------------------------------------------------------------
Total            2.43e-05  2.48e-05     4.88e-10     4.90e-05   100.0%
                 49.5%     50.5%        0.0%
================================================================
finish report_design_area
--------------------------------------------------------------------------------
Design area 1460 u^2 53% utilization.
```

优化前adder

```
finish report_checks -path_delay max
--------------------------------------------------------------------------------
Startpoint: num3[0] (input port clocked by core_clock)
Endpoint: num[8] (output port clocked by core_clock)
--------------------------------------------------------------------------------
                         32.00   data required time
                        -11.18   data arrival time
--------------------------------------------------------------------------------
                         20.82   slack (MET)
finish report_power
--------------------------------------------------------------------------------
Group            Internal  Switching    Leakage      Total
                 Power     Power        Power        Power (Watts)
----------------------------------------------------------------
Sequential       0.00e+00  0.00e+00     0.00e+00     0.00e+00   0.0%
Combinational    1.26e-05  1.10e-05     5.02e-10     2.36e-05   100.0%
Macro            0.00e+00  0.00e+00     0.00e+00     0.00e+00   0.0%
Pad              0.00e+00  0.00e+00     0.00e+00     0.00e+00   0.0%
----------------------------------------------------------------
Total            1.26e-05  1.10e-05     5.02e-10     2.36e-05   100.0%
                 53.5%     46.5%        0.0%
================================================================
finish report_design_area
--------------------------------------------------------------------------------
Design area 1231 u^2 51% utilization.
```

优化后adder

PART THREE ASIC综合

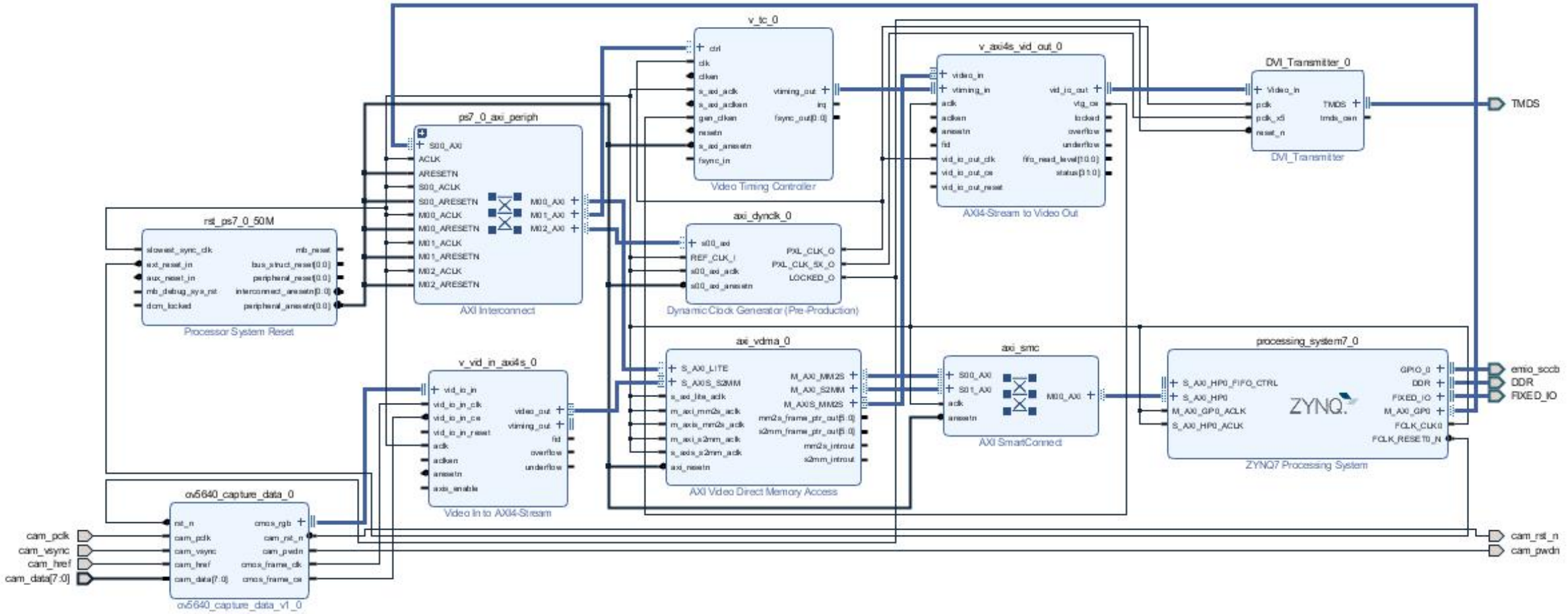
	优化前adder	优化后adder
Critical path	12.97	11.18
Total power	4.90e-05	2.36e-05
Design area	1460 u^2 53% utilization	1231 u^2 51% utilization

PART FOUR

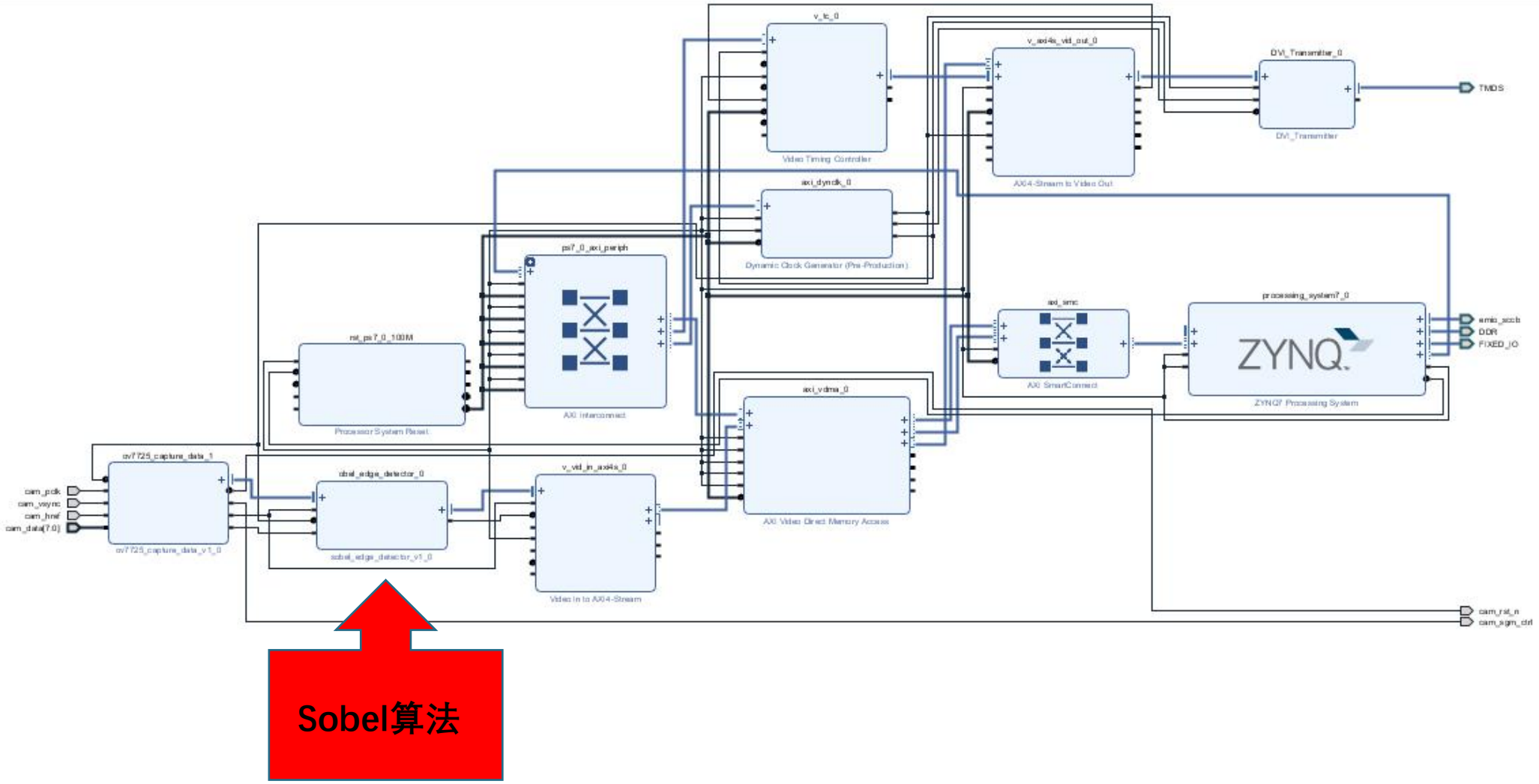
Sobel的实时滤波实现

PART FOUR Sobel的实时滤波实现

基于正点原子摄像头的PS-PL顶层:



PART FOUR 最终顶层设计



Sobel算法

感 谢 聆 听

Thank You