EE140LAB Report

LAB 2

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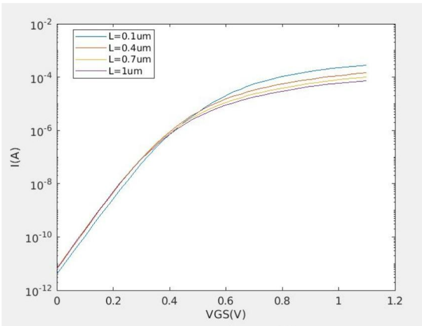
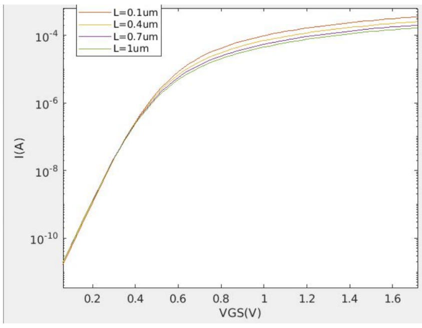
Before Exercise



(a)nmos1V



(b)nmos2V

Figure 1: ID–VGS

NMOS1V: VDS1=0.55V Vth1=0.425V
NMOS2V: VDS2 max=1.8V Vth2=0.775V
We find that : $Vth2 > Vth1$

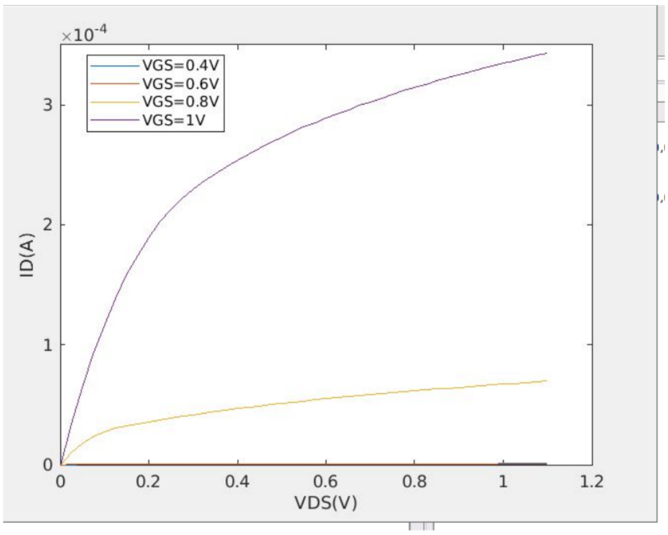


Figure 2: ID–VDS

L = 0.05um

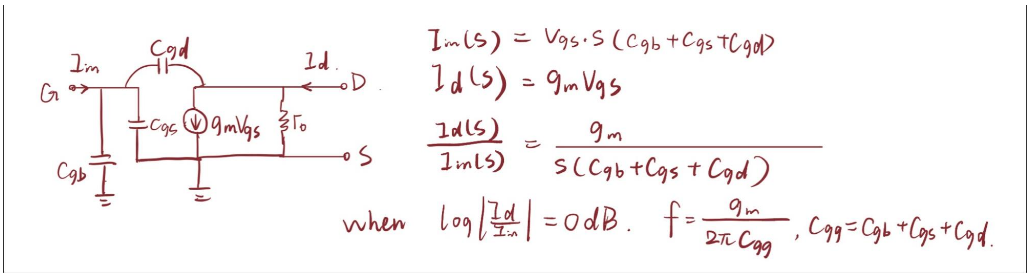


Figure 3: prove the function

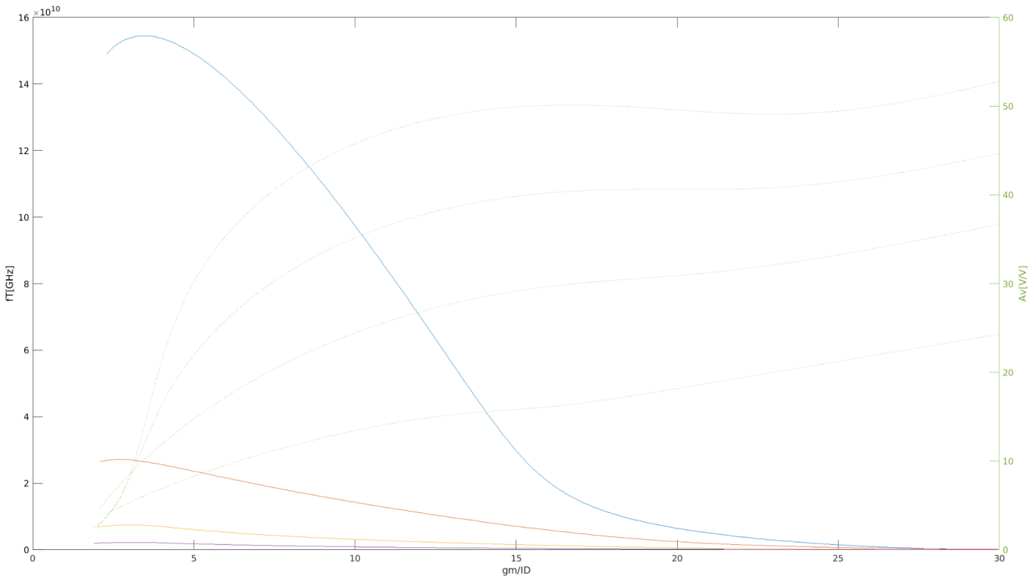


Figure 4: fT and Av = gm/gds of an intrinsic gain stage

Exercise 1: IGS with known gm/ID and L

```
gm_ID = 15;
L = 0.1;
fu = 1e9;
CL = 1e-12;
fT = look_up(nch, 'GM_CGG', 'GM_ID', gm_ID, 'L',L)/2/pi
% your code to obtain the intrinsic gain
gain = look_up(nch, 'GM_GDS', 'GM_ID', gm_ID, 'L',L)
% your code to obtain current density JD = ID/W
JD = look_up(nch, 'ID_W', 'GM_ID', gm_ID, 'L',L)
% your code to calculate  gm’ from ‘fu’ and ‘CL’
gm = 2*pi*fu*CL
ID = gm/gm_ID;
W = ID/JD;
VGS = look_upVGS(nch, 'GM_ID', gm_ID, 'L',L)
```

From the result of Matlab, we got f(T) = 1.914089549821622e+10 Hz, W = 45.834617192740836 um.

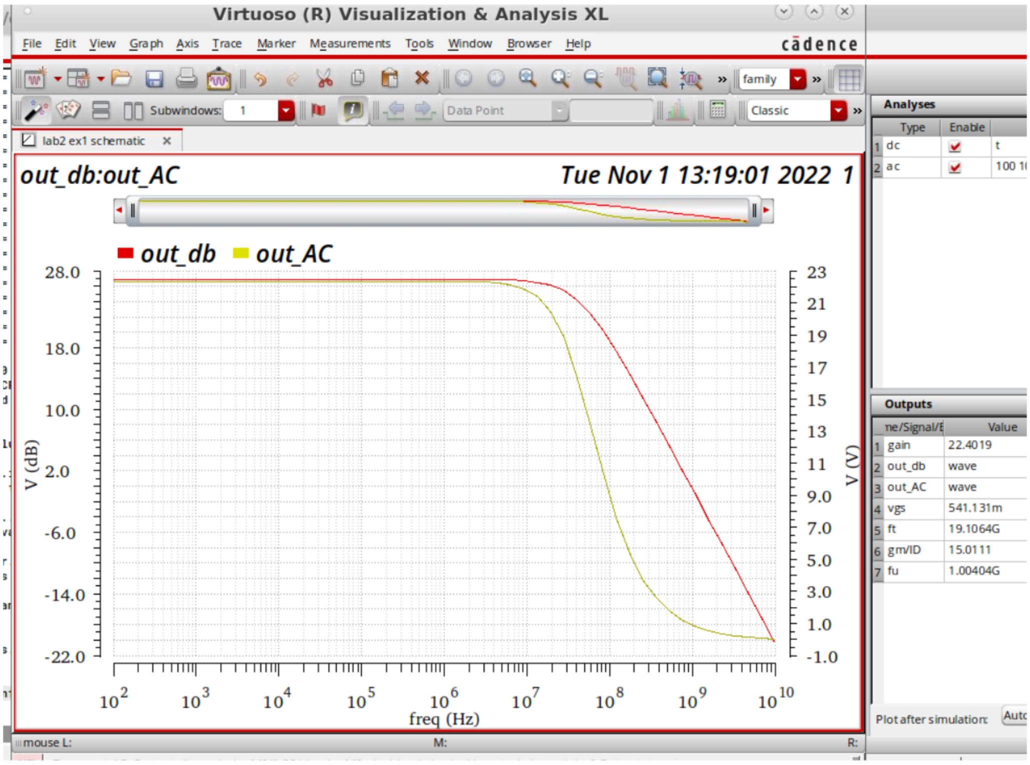


Figure 5: EX1: Bode Plot and simulation output

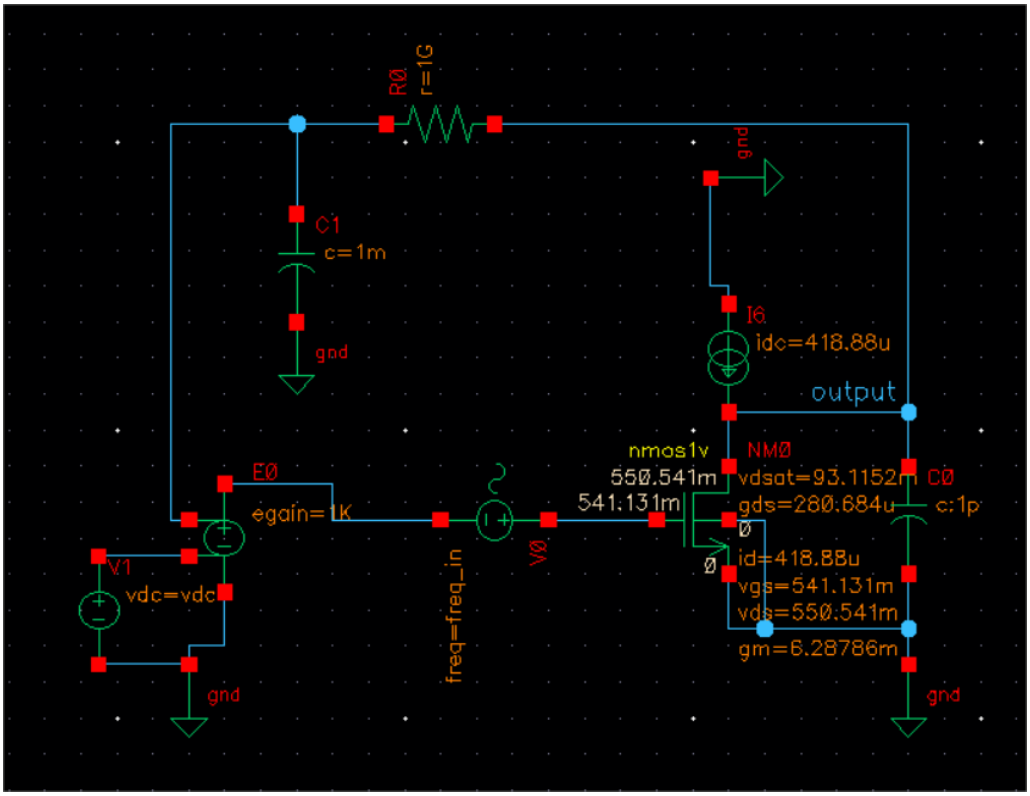


Figure 6: EX1: Schemetic

Table 1: Comparison in EX1

	Specification	Simulated result
gain	**22.3738**	**22.4**
fu	**1G**	**1.004G**
gm/ID	**15**	**15.011**
VGS	**0.5414**	**0.5413**

Exercise2 IGS with known gm/ID, Variable L

```
gm_ID = 5;
L = nch.L;
fu = 5e8;
CL = 1e-12;
% your code to calculate 'gm' from 'fu' and 'CL'
gm = 2*pi*fu*CL
ID = gm/gm_ID;
JD = look_up(nch, 'ID_W', 'GM_ID', gm_ID, 'L',L)
W = ID./JD;
% your code to obtain fT = gm/2cgg
fT = look_up(nch, 'GM_CGG', 'GM_ID', gm_ID, 'L',L)/2/pi
Av = look_up(nch, 'GM_GDS', 'GM_ID', gm_ID, 'L',L)
loglog(L, fT/1e9, '-k', L, Av, ':k');
```

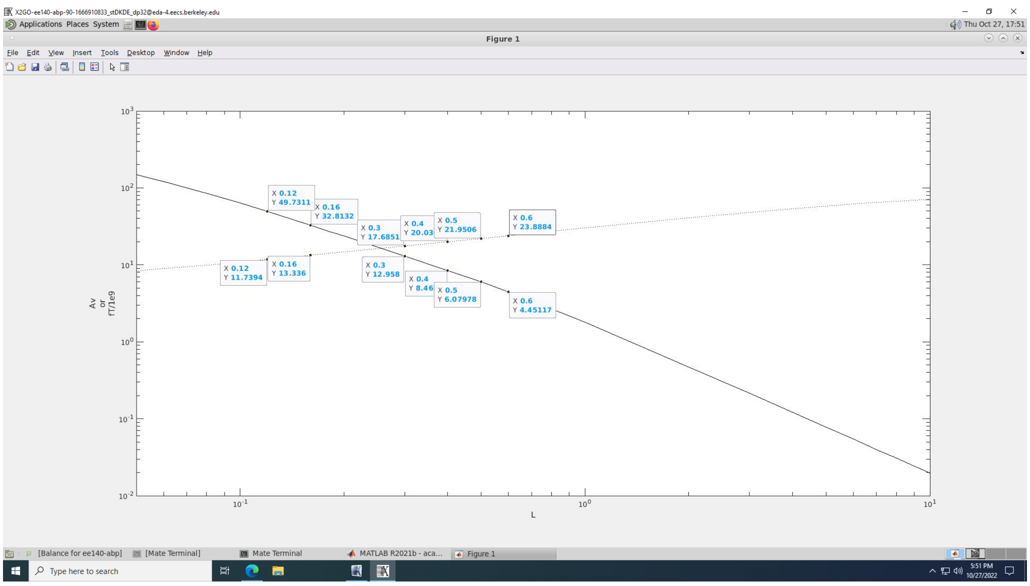


Figure 7: EX2: Find the achievable fT and Av

From the 7, we found that, in order to satisfy $fu <= ft/10$, ft should be larger than 5e9, we chose some solutions that satisfy the constraint.
I choose the solution L,W,ID=0.3, 10.84, 6.28E-4 ; L,W,ID=0.16, 7.42, 6.28E-4 to confirm the simulation.

Table 2: The achievable fT and Av

L(um)	W(um)	ID(A)	ft(Hz)	Av
0.5	14.42	6.2832e-4	6.1e9	22
0.4	12.76	6.2832e-4	8.46e9	20
0.3	10.84	6.2832e-4	1.30e10	17.7
0.16	7.42	6.2832e-4	3.28e10	13.3

Table 3: Comparison of the performance of 2 solutions

	simulation	specification	simulation	specification
L(um)	0.16	0.16	0.3	0.3
W(um)	7.42	7.42	10.84	10.84
ID(mA)	6.2832e-4	6.2832e-4	6.2832e-4	6.2832e-4
fu(Hz)	4.89e8	5e8	4.89e8	5e8
Av	12.9	13.3	17.9	17.7

We can find that to get the same fu, as ID is a constant, when L=3um, gain of the circuit is larger than when L=0.16um.

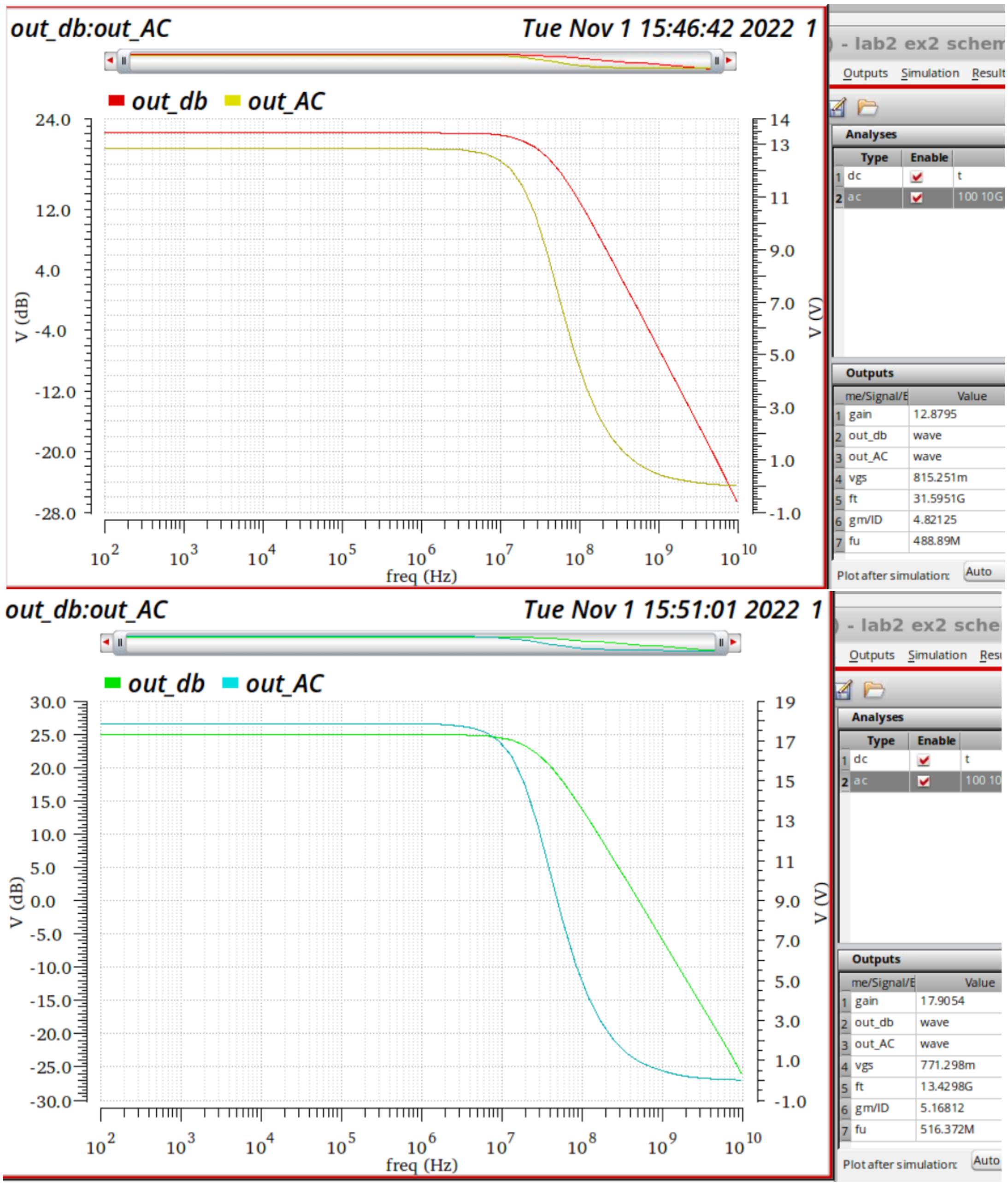


Figure 8: ID–VGS

Schematic of both exercise2 and exercise3.

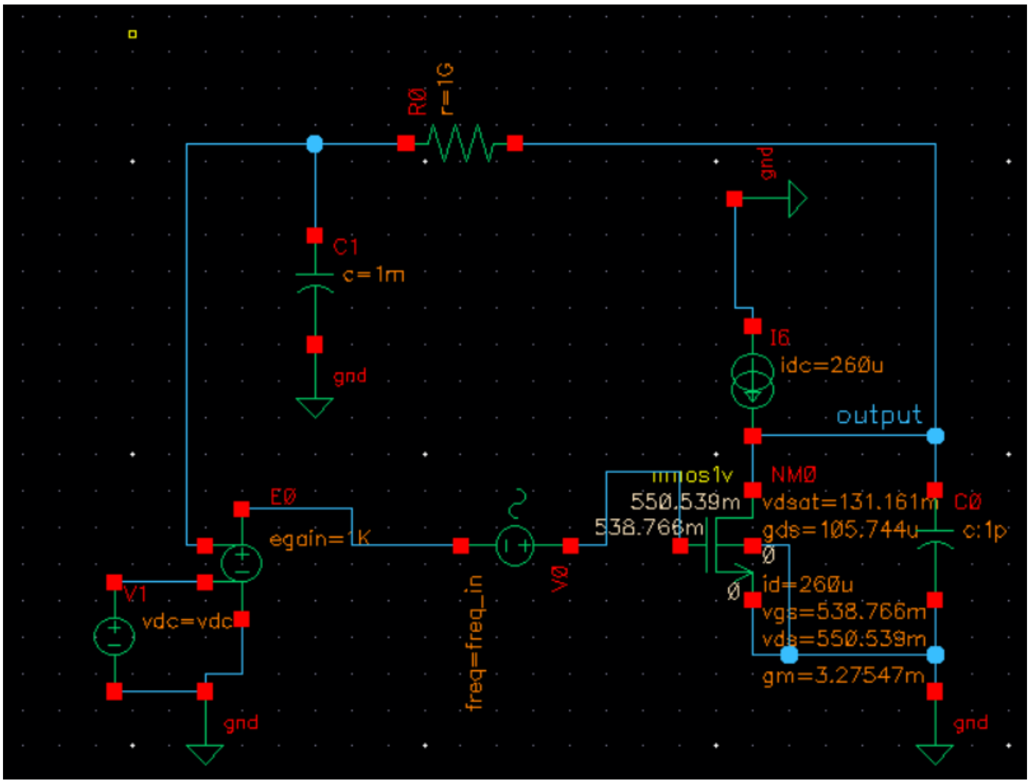


Figure 9: EX2,3: Schemetic of design

Exercise 3: IGS with variable gm/ID and L, Max Av optimization

```
L = nch.L;
fu = 5e8;
CL = 1e-12;
gm_ID_range = linspace(1, 30, length(L));
gm_ID = [];
for i = 1:length(L)
% your code to obtain fT = gm/2cgg
fT = look_up(nch, 'GM_CGG', 'GM_ID', gm_ID_range, 'L',L(i))/2/pi;
M = fT >= 10*fu;
if(any(M))
gm_ID(i) = gm_ID_range(max(find(M==1)));
else
gm_ID(i) = NaN;
end
% your code to obtain Av(i) = gm/gds
Av(i) = look_up(nch, 'GM_GDS', 'GM_ID', gm_ID(i), 'L',L(i));
end
plot(L, Av, L, gm_ID)

%%
gm_ID_opt = 12.1538; % replace X based on the results obtained above
```

```
L_opt = 0.3; % replace Y based on the results obtained above
% your code tJD = look_up(nch, 'ID_W', 'GM_ID', gm_ID, 'L',L)o obtain JD
JD = look_up(nch,'ID_W','GM_ID',gm_ID_opt,'L',L_opt);
Cdd_W = look_up(nch,'CDD_W','GM_ID',gm_ID_opt,'L',L_opt);
Cdd(1) = 0;
for m = 1:10
gm_opt = 2*pi*fu*(CL+Cdd(m));
% your code to obtain ID(m)
ID(m) = gm_opt/gm_ID_opt;
W(m) = ID(m)./JD;
Cdd(m+1) = W(m)*Cdd_W;
end
fT_opt = look_up(nch, 'GM_CGG', 'GM_ID', gm_ID_opt, 'L',L_opt)/2/pi;
```

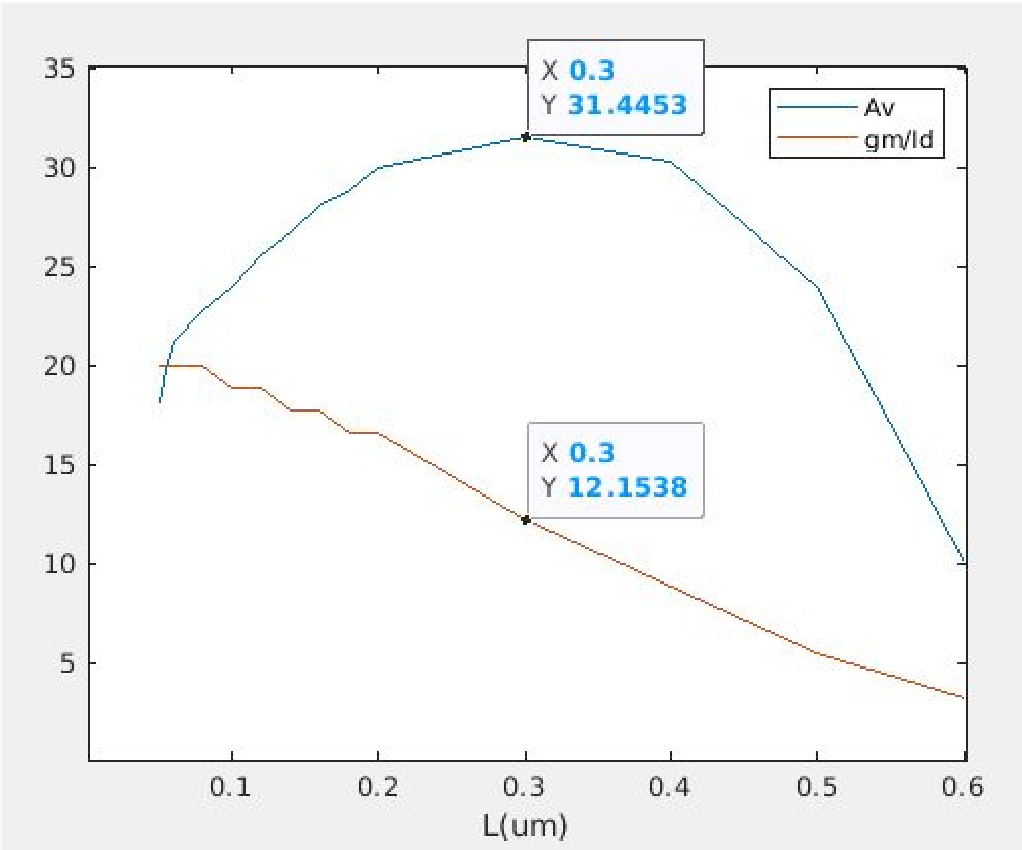
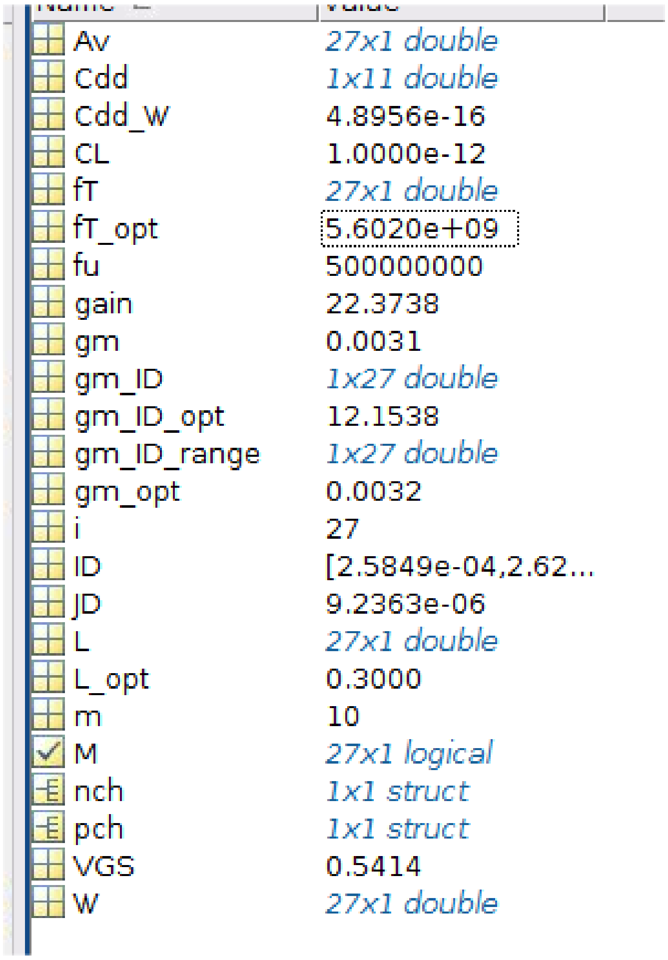


Figure 10: EX3: Find L,gm/ID pair to compute the intrinsic gain

Option gm/Id =12.15 Av=31.4 Option L=0.3um Through iterative fashion, we got a converge W=28.37um, Cdd=1.39e-14.



Name	Value
Av	27x1 double
Cdd	1x11 double
Cdd_W	4.8956e-16
CL	1.0000e-12
fT	27x1 double
fT_opt	5.6020e+09
fu	500000000
gain	22.3738
gm	0.0031
gm_ID	1x27 double
gm_ID_opt	12.1538
gm_ID_range	1x27 double
gm_opt	0.0032
i	27
ID	[2.5849e-04,2.62...
JD	9.2363e-06
L	27x1 double
L_opt	0.3000
m	10
M	27x1 logical
nch	1x1 struct
pch	1x1 struct
VGS	0.5414
W	27x1 double

Figure 11: EX3: matlab result

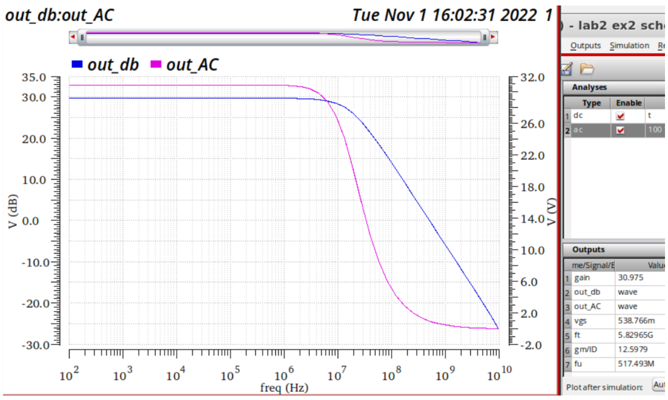


Figure 12: EX3: AC simulation output

After comparing the performance of the design in exercise 3 against the design in the previous exercise, we find that new design consume lower power and higher gain.

Table 4: Comparison of the performance in ex3 and ex2

	sim3	spec3	sim2	spec2
L(um)	**0.3**	**0.3**	**0.3**	**0.3**
W(um)	**28.37**	**28.37**	**10.84**	**10.84**
ID(mA)	**2.6e-4**	**2.6e-4**	**6.2832e-4**	**6.2832e-4**
fu(Hz)	**5.1e8**	**5.1e8**	**5e8**	**5e8**
Av	**31.0**	**31.4**	**17.9**	**17.7**

Exercise 4a: Common-source with active PMOS load

```
fu = 1e8;
fT = 1e9;
CL = 1e-12;
Vdsat2 = 0.2;
L1 = 0.05:0.01:1.5;
% your code to obtain gm_ID1, using fT and L1;
gm_cgg = 2*pi*fT;
gm_ID1 = look_up(nch, 'GM_ID', 'GM_CGG', gm_cgg, 'L', L1);

gds_ID1 = diag(look_up(nch, 'GDS_ID', 'GM_ID', gm_ID1, 'L', L1));

L2 = 0.05:0.05:2;

gm_ID2 = 2/Vdsat2;

for k = 1:length(L2)

    % your code to obtain gds_ID2, using gm_ID2 and L2(k)
    gds_ID2 = look_up(pch, 'GDS_ID', 'GM_ID', gm_ID2, 'L', L2(k));

    Av(:,k) = gm_ID1./(gds_ID1+gds_ID2);

end
[max_gains L2_opt] = max(Av);
%L2_opt1 = transpose(L2_opt)

%%

Cdd(:,1) = zeros(length(L2_opt),1);
for k = 1:10
    gm = 2*pi*fu*(CL+Cdd(:,k));
    ID = gm./gm_ID1(L2_opt);
    W1 = ID./diag(look_up(nch,'ID_W','GM_ID', gm_ID1(L2_opt),'L',L1(L2_op
    Cdd1 = W1.*diag(look_up(nch,'CDD_W','GM_ID',gm_ID1(L2_opt),'L', L1(L2
    % your code to obtain W2
```

```
    W2 = ID./look_up(pch,'ID_W','GM_ID', gm_ID2,'L',L2);
    % your code to obtain Cdd2
    Cdd2 = W2.*look_up(pch,'CDD_W','GM_ID',gm_ID2,'L', L2);
    % your code to obtain updated Cdd(:,k+1)
    Cdd(:,k+1) = Cdd1+Cdd2;
end

L =L1(L2_opt);

 area = W1'.*L1(L2_opt) + 2*W2'.*L2
% your code to plot area vs. maximum gain
figure(10)
subplot(2,2,1)
plot(area, max_gains)
title('area vs. maximum gain')
% your code to plot area vs. L1 and W1
subplot(2,2,2)
plot(area, L1(L2_opt), '-')
hold on
yyaxis right
plot(area, W1, ':')
title('area vs. L1 and W1')
% your code to plot area vs. L2 and W2
subplot(2,2,3)
plot(area, L2, '-')
hold on
yyaxis right
plot(area, W2, ':')
title('area vs. L2 and W2')
% your code to plot area vs. ID
subplot(2,2,4)
plot(area, ID)
title('area vs. ID')
```

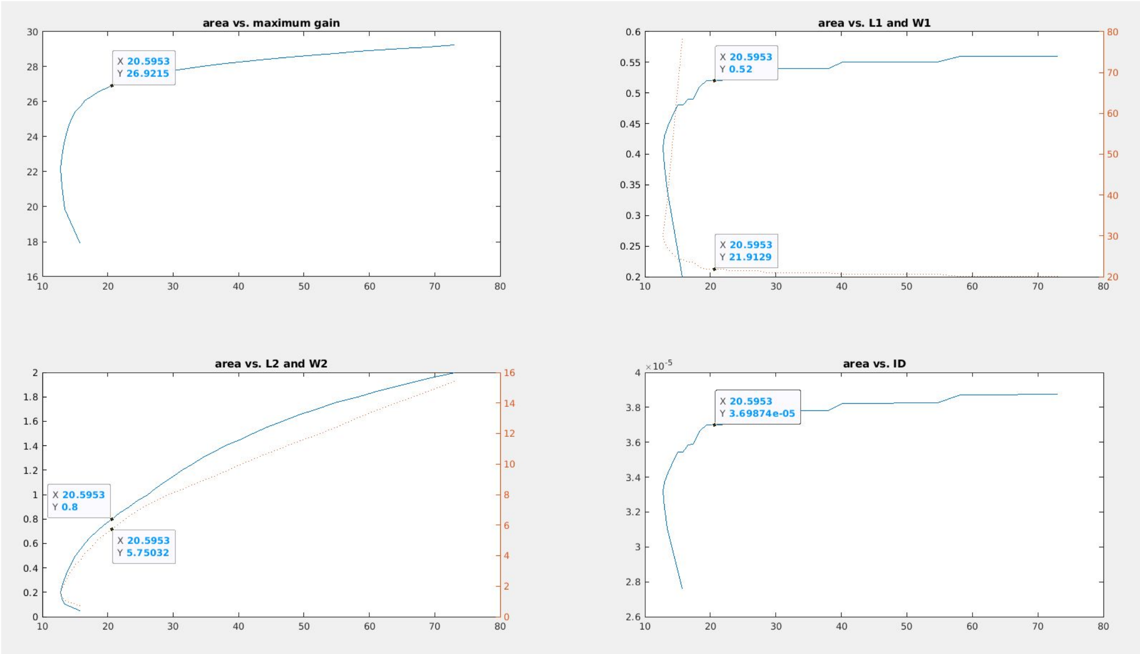


Figure 13: EX4: achieving maximum gain with minimum area and find W, L, ID, VGS

From the figure above, we got maximum gain = 26.92 when area = 20.6, W2 = 5.7um, L2 = 800nm, W1 =21.9um, L1 =520nm, ID =37uA , VGS= 437.29mV.
We build a schemetic.

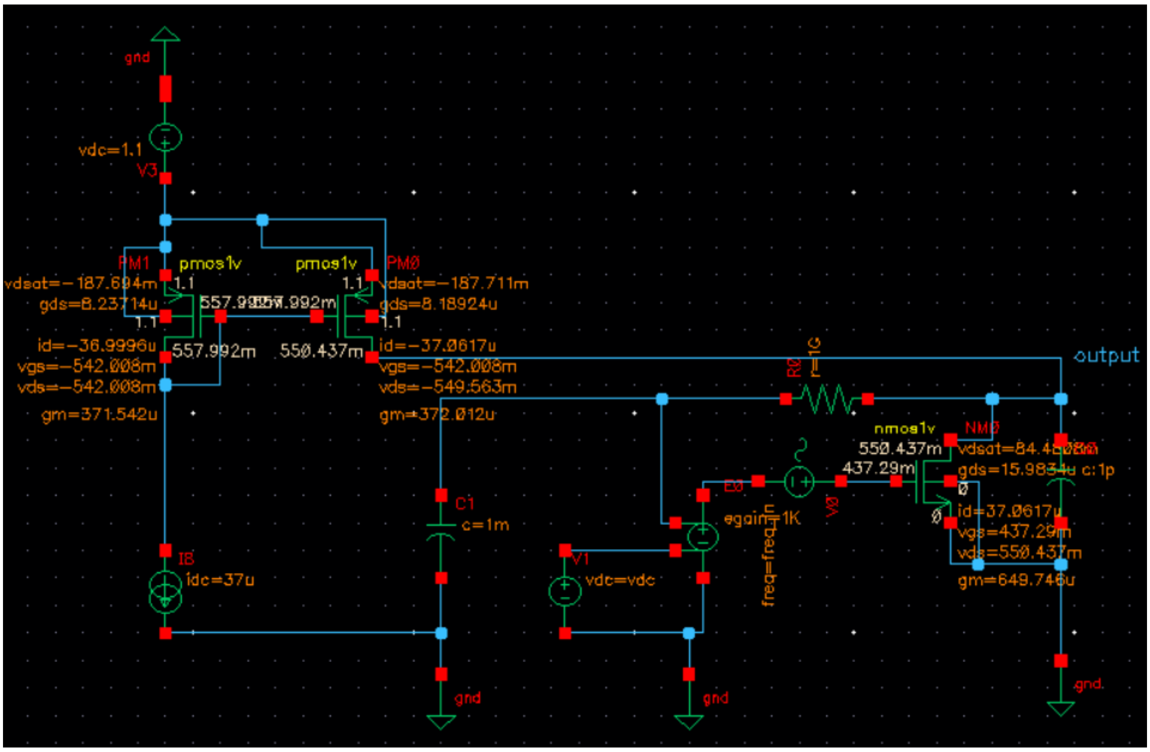


Figure 14: EX4: Schemetic of design

The AC simulation outputs is below.

Table 5: EX4a: comparison of the result of simulation and calculation

	simulation	calculation
gain	26.89	26.92
ID	37uA	37uA
fu	105MHz	100MHz

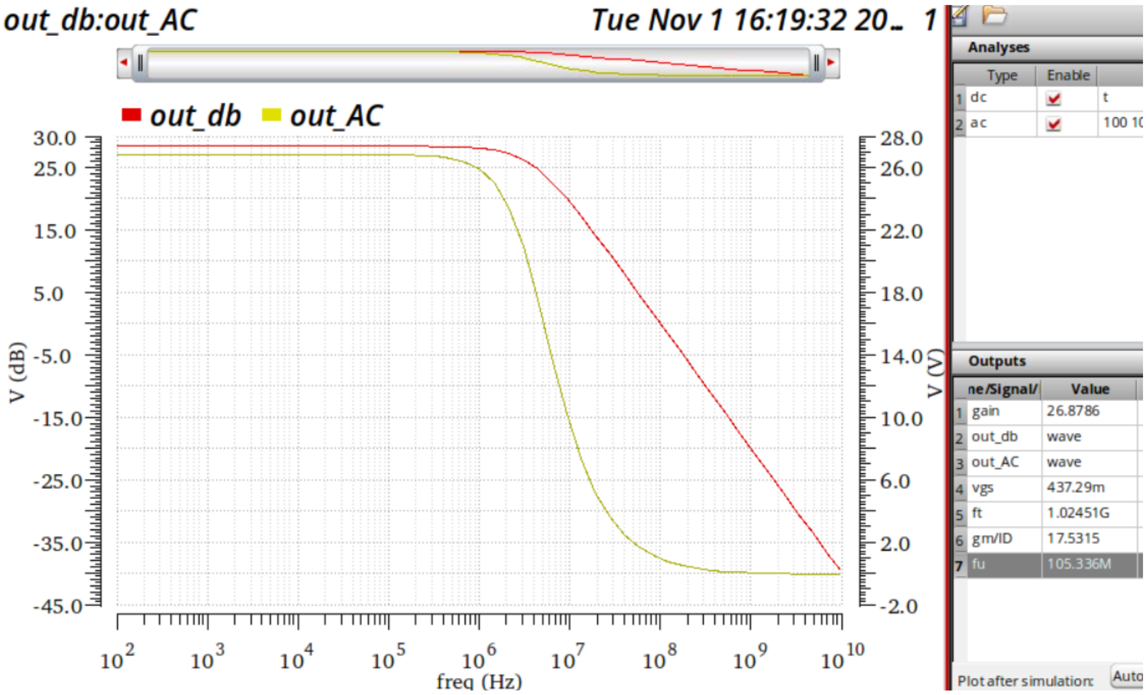


Figure 15: EX4: AC simulation from ex4a

Exercise 4b: Conversion to classic differential amplifier

Reusing the design in exercise 4a for the differential implementation of the amplifier. Schemetic of new design is below.

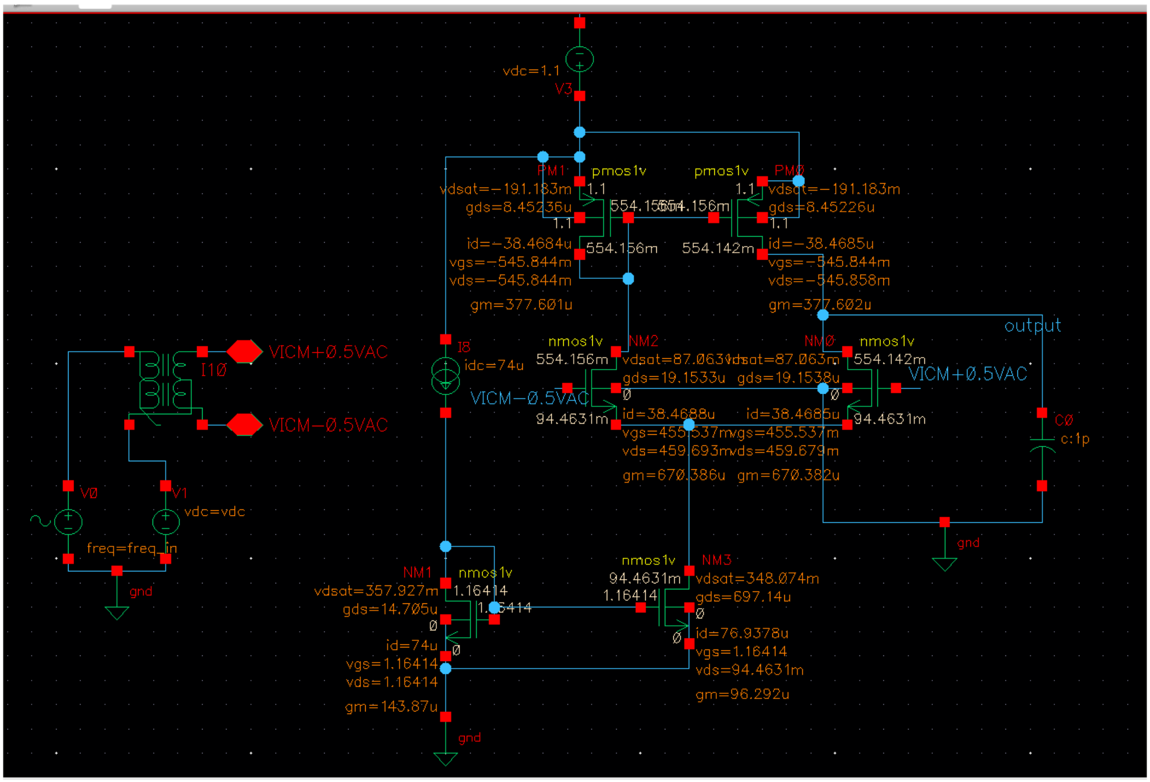


Figure 16: EX4b:Conversion to classic differential amplifier

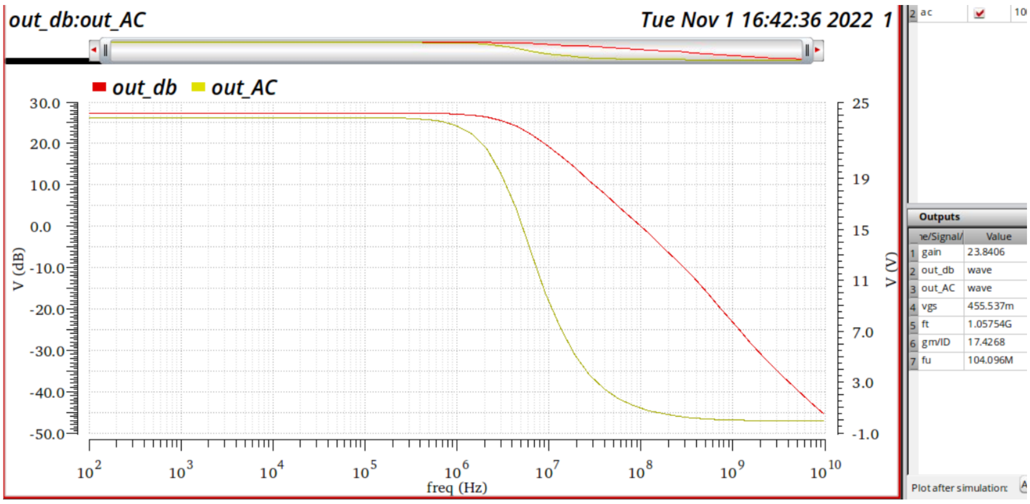


Figure 17: EX4b:AC simulation output of exercise 4b

We can do a comparison of the designs from 4a and 4b.
We find that the circuit of ex4b have less gain comparing to the circuit of ex4a. There are several reasons causing this error. Most notably, VDS of tail transistor is smaller than what we assume, it tend to make the ID of amplifier smaller than in ex4a.

Table 6: comparison of the performance of the design from 4a and 4b

Design	4a	4b
gain	26.8	23.8
gm/ID	17.5	17.4
fu(Hz)	105M	104M

Exercise 5: Common-source with resistive load

Design1 from lab0 circuit

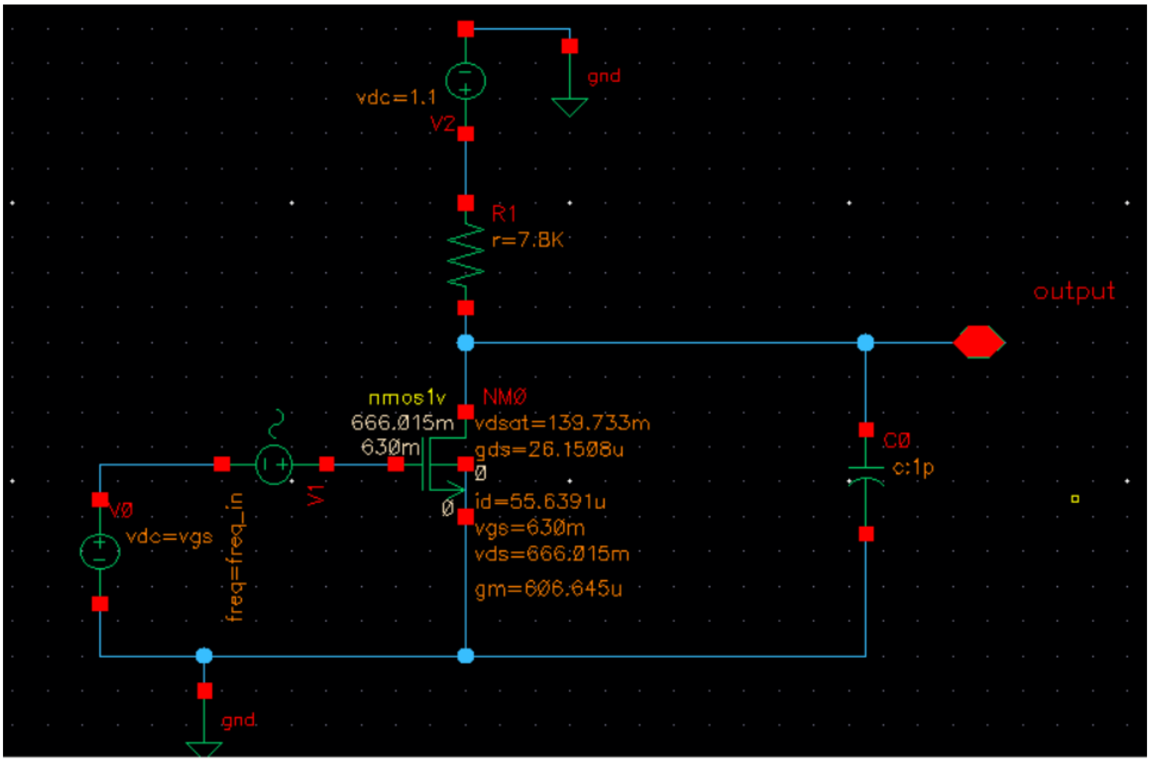


Figure 18: schematic from lab0 circuit

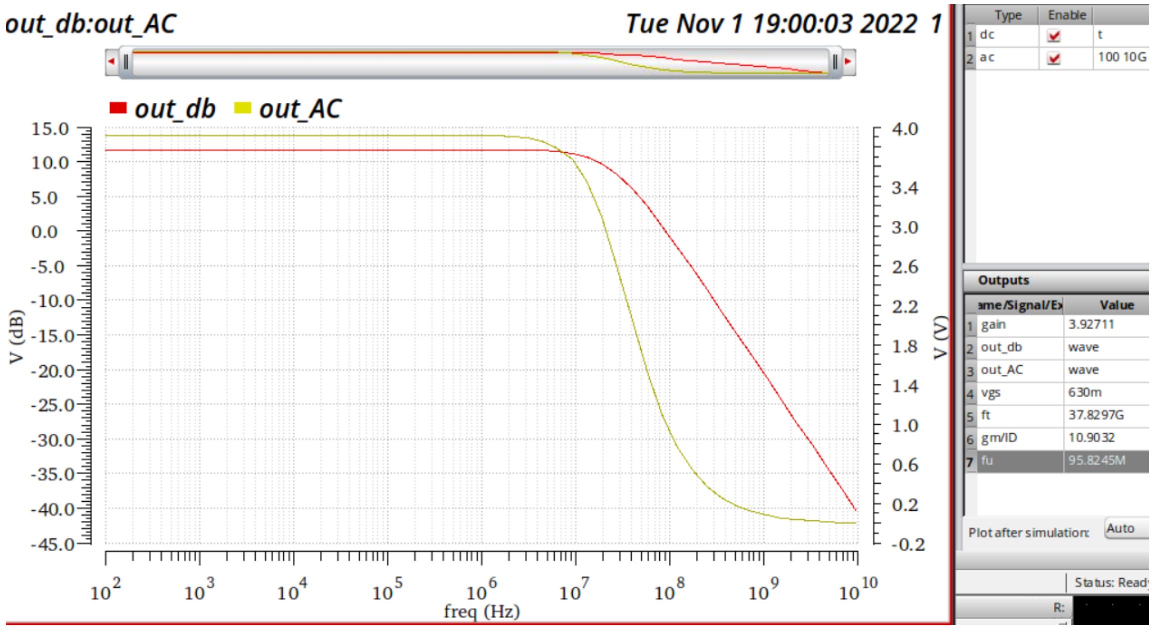
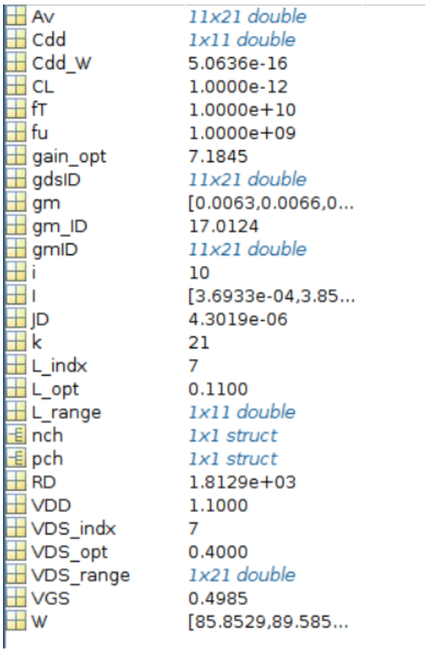


Figure 19: AC simulation output of lab0 circuit

Design2 from given code

```
fu = 1e9;
fT = fu*10;
CL = 1e-12;
VDD = 1.1;
VDS_range = 0.1:0.05:1.1;
L_range = 0.05:0.01:0.15;
for k = 1:length(VDS_range)
gmID(:,k)=look_up(nch,'GM_ID','GM_CGG',2*pi*fT,'VDS',VDS_range(k),'L', L_
% your code to calculate gdsID(:,k)
gdsID(:,k)=look_up(nch,'GDS_ID','GM_CGG',2*pi*fT,'VDS',VDS_range(k),'L',
% your code to find Av(:,k)
Av(:,k) = (gmID(:,k)./(gdsID(:,k)+1/(VDD-VDS_range(k))))
end
gain_opt = max(max(Av))
[L_indx, VDS_indx] = find(Av == gain_opt)
VDS_opt = VDS_range(VDS_indx)
L_opt = L_range(L_indx)
% your code to find gm_ID
gm_ID = look_up(nch,'GM_ID','GM_CGG',2*pi*fT,'VDS',VDS_opt,'L',L_opt);
% your code to find current density (JD) at the optimal design point
JD= look_up(nch,'ID_W','GM_ID',gm_ID,'L',L_opt);
Cdd_W = look_up(nch,'CDD_W','GM_ID',gm_ID,'VDS',VDS_opt,'L',L_opt);
%%%%%%%%%%%%%%%%%%%%%
Cdd(1) = 0;
for i = 1:10
% your code to obtain gm(i)
```

```
gm(i)=2*pi*fu*(CL+Cdd(i));
% your code to obtain I(i)
I(i)=gm(i)/gm_ID;
% your code to obtain W(i)
W(i)=I(i)/JD;
Cdd(i+1) = W(i)*Cdd_W;
end
% your code to find RD
RD =(VDD-VDS_opt)/I(10);
% your code to obtain the required gate-source bias voltage
VGS = look_upVGS(nch,'GM_ID',gm_ID,'VDS',VDS_opt,'L',L_opt);
```



Av	11x21 double
Cdd	1x11 double
Cdd_W	5.0636e-16
CL	1.0000e-12
fT	1.0000e+10
fu	1.0000e+09
gain_opt	7.1845
gdsID	11x21 double
gm	[0.0063,0.0066,0...
gm_ID	17.0124
gmID	11x21 double
i	10
I	[3.6933e-04,3.85...
JD	4.3019e-06
k	21
L_indx	7
L_opt	0.1100
L_range	1x11 double
nch	1x1 struct
pch	1x1 struct
RD	1.8129e+03
VDD	1.1000
VDS_indx	7
VDS_opt	0.4000
VDS_range	1x21 double
VGS	0.4985
W	[85.8529,89.585...

Figure 20: solution from Matlab

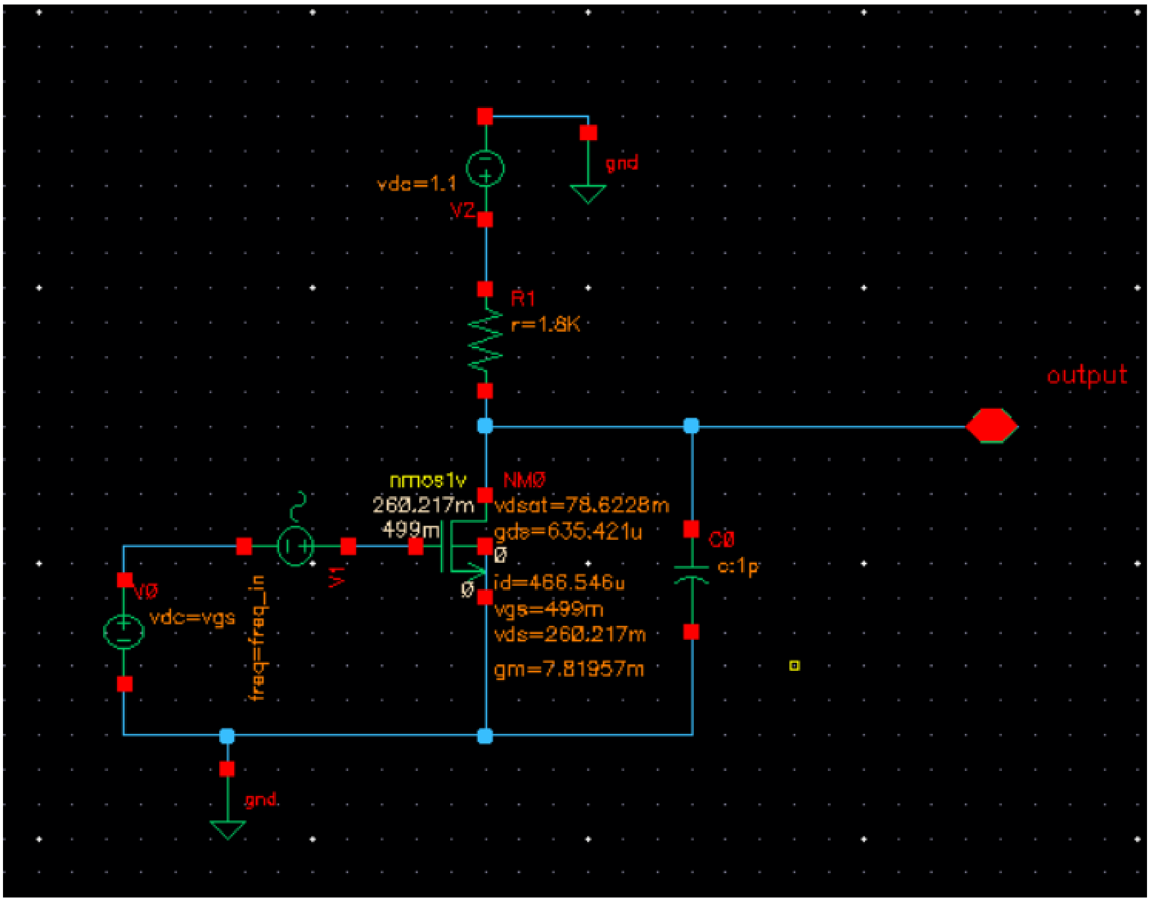


Figure 21: schematic of circuit2

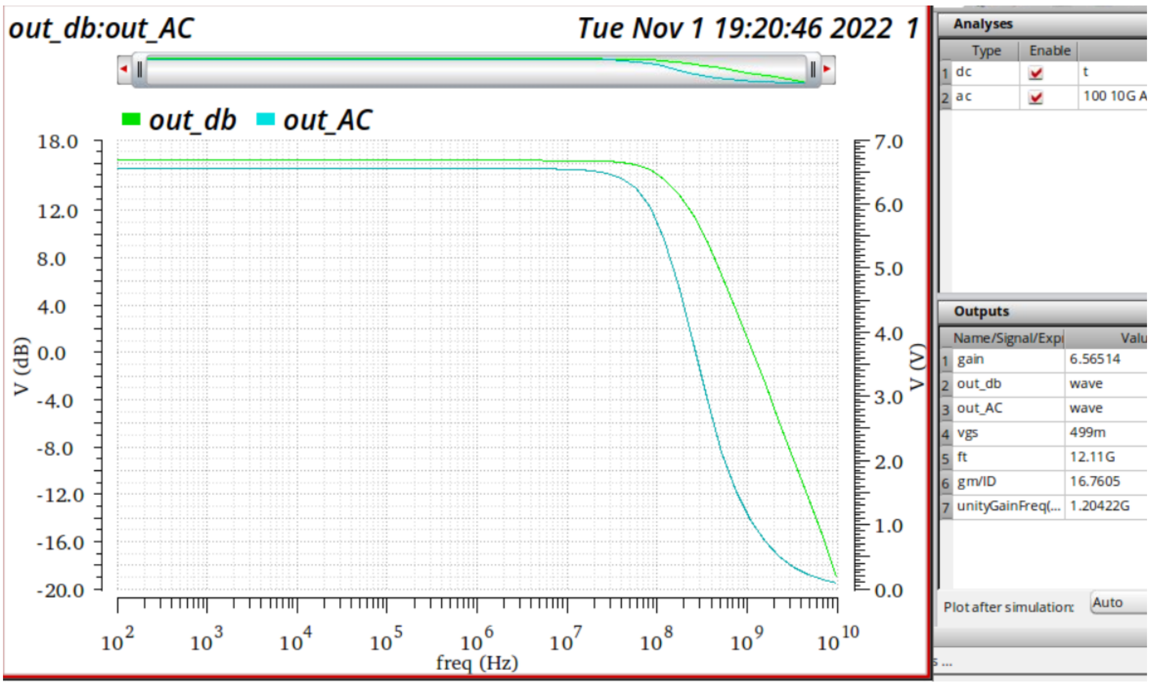


Figure 22: AC simulation outputs of circuit2

Design3 from redesigned lab0 circuit

```
fu = 96e6;
fT = fu*10;
CL = 1e-12;
VDD = 1.1;
VDS_range = 0.1:0.05:1.1;
L_range = 0.05:0.01:0.15;
for k = 1:length(VDS_range)
gmID(:,k)=look_up(nch,'GM_ID','GM_CGG',2*pi*fT,'VDS',VDS_range(k),'L', L_
% your code to calculate gdsID(:,k)
gdsID(:,k)=look_up(nch,'GDS_ID','GM_CGG',2*pi*fT,'VDS',VDS_range(k),'L',
% your code to find Av(:,k)
Av(:,k) = (gmID(:,k)./(gdsID(:,k)+1/(VDD-VDS_range(k))))
end
gain_opt = max(max(Av))
[L_indx, VDS_indx] = find(Av == gain_opt)
VDS_opt = VDS_range(VDS_indx)
L_opt = L_range(L_indx)
% your code to find gm_ID
gm_ID = look_up(nch,'GM_ID','GM_CGG',2*pi*fT,'VDS',VDS_opt,'L',L_opt);
% your code to find current density (JD) at the optimal design point
JD= look_up(nch,'ID_W','GM_ID',gm_ID,'L',L_opt);
Cdd_W = look_up(nch,'CDD_W','GM_ID',gm_ID,'VDS',VDS_opt,'L',L_opt);
%%%%%%%%%%%%%%%%%%%%%
Cdd(1) = 0;
for i = 1:10
% your code to obtain gm(i)
gm(i)=2*pi*fu*(CL+Cdd(i));
% your code to obtain I(i)
I(i)=gm(i)/gm_ID;
% your code to obtain W(i)
W(i)=I(i)/JD;
Cdd(i+1) = W(i)*Cdd_W;
end
% your code to find RD
RD =(VDD-VDS_opt)/I(10);
% your code to obtain the required gate-source bias voltage
VGS = look_upVGS(nch,'GM_ID',gm_ID,'VDS',VDS_opt,'L',L_opt);
```

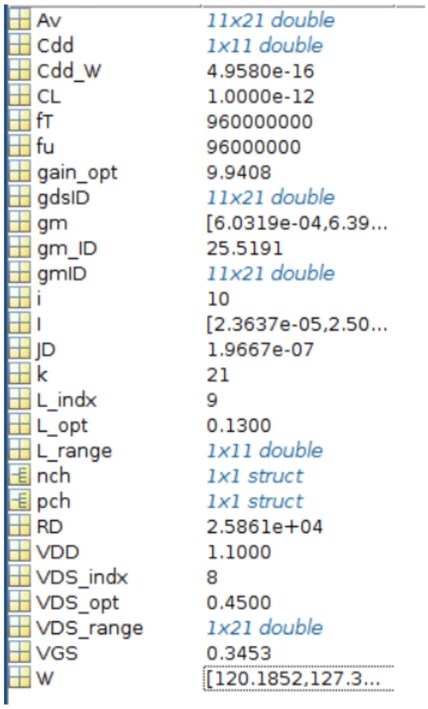


Figure 23: solution from Matlab of redesigned circuit

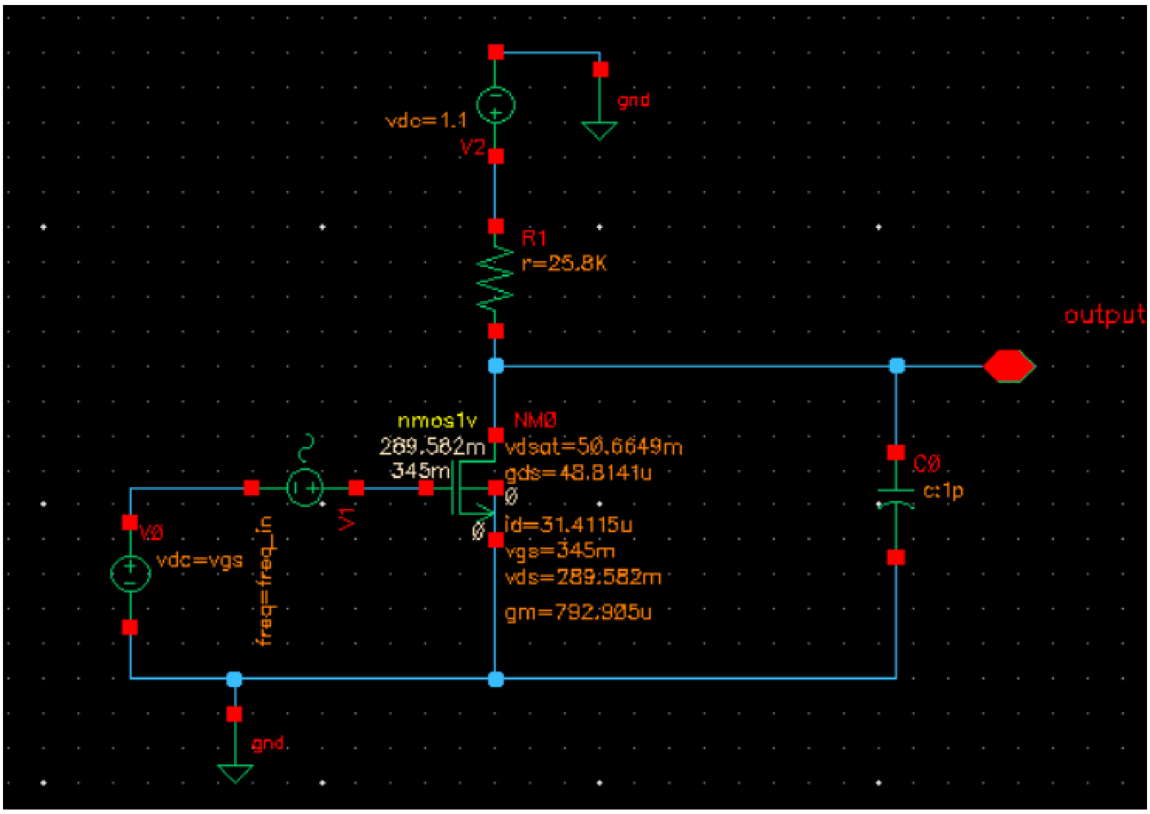


Figure 24: schematic of redesigned lab0 circuit

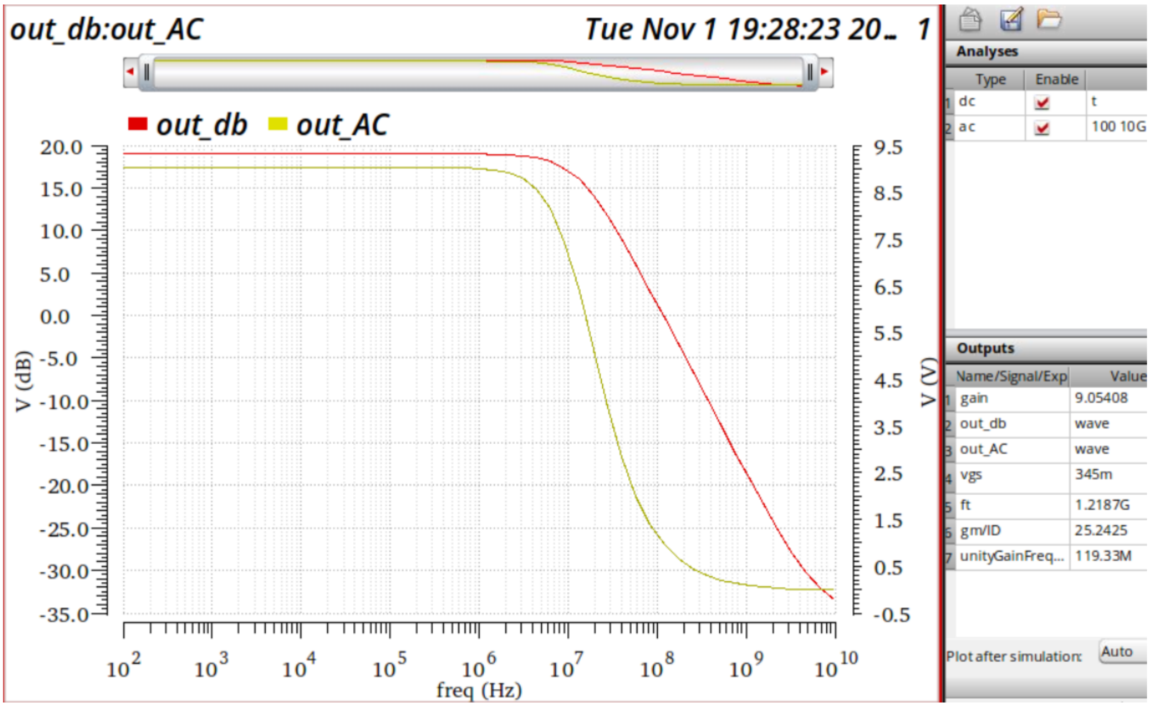


Figure 25: AC simulation outputs of redesigned lab0 circuit

Table 7: comparison of 3 circuits in exercise 5

Design	sim1	spec2	sim2	spec3	sim3
gain	3.93	7.18	6.6	9.94	9.05
fu(Hz)	95.82M	1G	1.2G	96M	119.33M
gm/ID	10.9	17	16.8	25.5	25.2
W(um)	2	89.7	89.7	128	128
L(nm)	100	110	110	130	130
VDS(mV)	666	400	260.2	450	290
RD(k)	7.8	1.8	1.8	25.8	25.8
P(W)	6e-5	27e-5	39.2e-5	1.6e-5	2.5e-5

From the table 7, I think the amplifier we used in Lab 0 was not an optimal design. When we redesigned it, we found that when we design a new circuit which has approximately the same unity gain bandwidth of the circuit in lab0. We can get higher gain and lower power. But what we shouldn't ignore is that the new circuit need a transistor whose width is larger than 128 um. So if we take area into consideration, we can make an optimal design.