# EE140 LAB1 report

#### Shengxi Liang

PART1

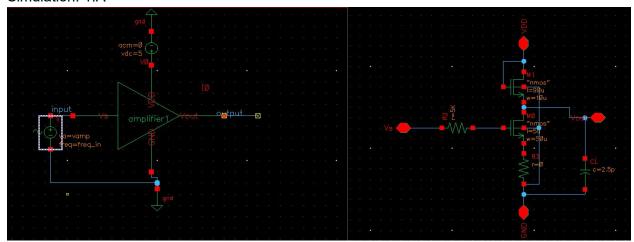
Hand-Calculation: 1.A

1. A. 
$$I_{D} = \frac{1}{2}MC_{0}x\frac{W}{L}(V_{E15}-V_{TH})^{2}(1+\lambda_{1}V_{D5})$$
  $I_{D} = I_{D2}$ 

Refo.  $V_{B} = 1.1V$ .  $V_{B15} = 1.1V$ .

 $I_{D} = 40.5 \mu A_{1}$ 
 $I_{D} = 40.5 \mu A$ 

#### Simulation: 1.A



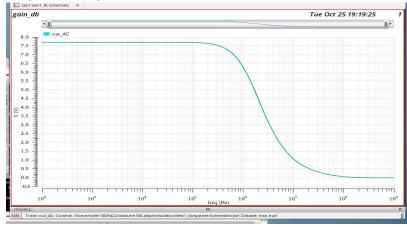
#### vout/vs & Bandwidth



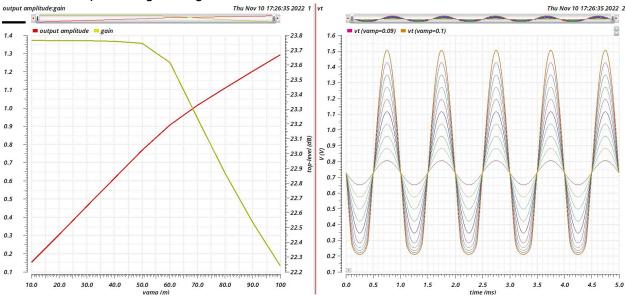
#### Rout



# Magnitude of gain



#### Maximum output voltage swing

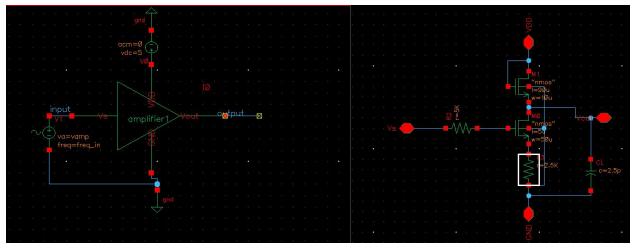


Output swing: 1.5V - 0.2V = 1.3V

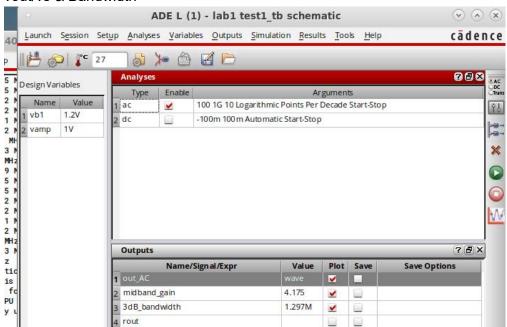
In this part, we found that the differences of hand-calculation and simulation is not very noticeable(table1), but it can't be ignored. Due to the fact that in the process of hand calculation, we ignored lateral diffusion and sometimes we ignored body effect, so the Rout and mid-band gain from hand-calculation and simulation are different in a small degree. Especially for bandwidth, we learned that in the process of hand-calculation, we used the asymptotic approximation technique, so it has a very obvious difference.

#### Hand-calculation: 1.B

#### Simulation: 1.B



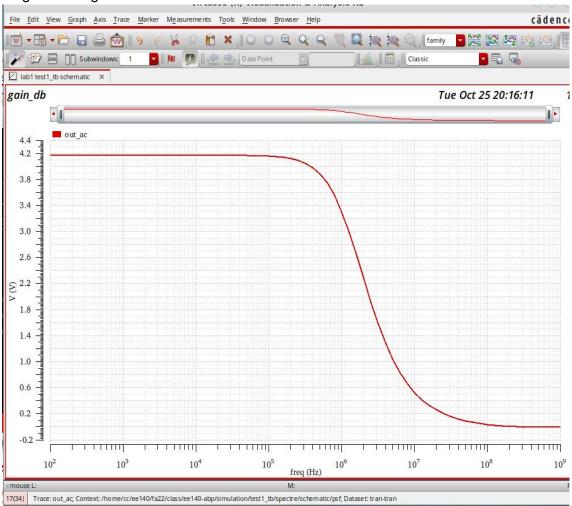
#### vout/vs & Bandwidth

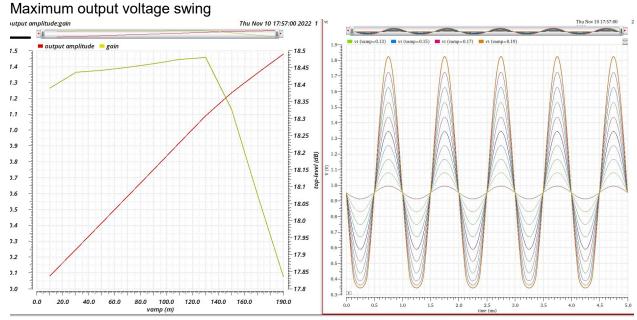


#### Rout

L	Name/Signal/Expr	Value	Plot	Save	Save Option	is 🔼
1	out_AC	wave	~	100		
2	midband_gain					Ū
3	3dB_bandwidth			(a)		
4	rout	31.47K	~			-
P	lot after simulation: Auto	Plotting mode	Repl	ace		
		3000				State: state4
		Status: Read	y   T=	27 C	Simulator: spectr	e

## Magnitude of gain





When vamp=0.15V, we got the maximum output swing: 1.82V - 0.35 V = 1.47 V

In part B, we found that the differences of hand-calculation and simulation is much more obvious than part A(table1), it is because we have Rd=2.5k  $\Omega$ , not 0, the mid-band gain is influenced a lot.

Due to the fact that in the process of hand calculation, we ignored lateral diffusion and sometimes we ignored body effect, the Rout from hand-calculation and simulation are different in a small degree.

Additionally, for bandwidth, we learned that in the process of hand-calculation, we used the asymptotic approximation technique, so it has a very obvious difference.

	1A calculation	1A simulation	1B calculation	1B simulation
Rout	28.1k Ω	28.46k Ω	<b>30.4k</b> Ω	<b>31.47k</b> Ω
BW	1.6MHz	1.422MHz	1.443MHz	1.297MHz
Mid-band gain	7.8	7.7	5.6	4.175

Table 1 list of relevant perform parameters

From A to B, we got almost same bandwidth, but midband gain is lower.

#### PART2:

Parameter	Specification – EE140	Specification - EE240A		
Midband gain	≥ 120 V/V	≥ 140 V/V		
3 dB cutoff frequency (bandwidth)	≥ 180 kHz	≥ 200 kHz		
Output voltage swing	≥ 3 Vpp 2.5 pF			
Load capacitance				
Source resistance	5 kΩ			
Supply voltage	VDD = 5 V, VSS = Ground = 0 V			

#### Hand-calculation 2:

In the process of doing hand-writing, firstly I choose the specification of my design. And I try to let every transistor is in satuation.

From these specs, I can get gm first. Then we find the Rout of this circuit as function of ID. Due to the fact that gm can be calculate with  $\triangle V_1$  and ID, we use an approximation to let  $Gm=gm_1$ .

Now we can get the function of mid-band gain, which is only depends on  $\Delta V_1$ , rather than Id. With  $\Delta V_1$ , gm, we are able to calculate Id.

As I have choose the specs of design. We got the boundary of  $\triangle V_1$  and  $\triangle V_2$  from output swing.

From the boundary of  $\triangle V_1$  and  $\triangle V_2$ , we choose a pair of value to calculate Rout, mid-band gain as well as bandwidth until they meet requirements.

Now we got everything we need to calculation the right W1, W2.

As we are suggested to use correct mirror to bias M2, we do calculation to find the width of another pmos, and found the correct I<sub>bias</sub>.

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sat (even my change)
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(Courset mirror)

$$\frac{W_1}{L_1} = \frac{W_1}{5\mu m}$$

$$\frac{W_2}{L_2} = \frac{W_2}{5\mu m}$$

$$\frac{W_{r}}{\sqrt{2}} = \frac{W_{r}}{\sqrt{2}}$$

hint from instructions: VG15 > 1V

$$g_{m} = \mu (o_{X} \frac{W}{L} (V_{06} - V_{7H}) = \frac{2 I_{p}}{V_{06} - V_{7H}} = \sqrt{2 \mu (o_{X} \frac{W}{L})_{p}} \qquad \lambda_{1}$$

$$r_{0} = \frac{1}{\lambda I_{p}}$$

$$I_{D} = \frac{1}{2 \mu (o_{X} \frac{W}{L} (V_{06} - V_{7H})^{2} (1 + \lambda V_{D5})$$

To begin with, we choose the specifications of designi @ Midbond-gam: 150 V/V. Obandwidth 250 KHz

@ outputs swing = VOD-AV2-AV1 => VPP =>. aV1+AV2 = 2V other constrains: 2=5 mm. all in saturation. 3 Vast IV

start calculation.

DV2=1.56V.

if we choose  $\Delta V_1 = 0.39 \, \text{V}$ ,  $10 = \frac{\Delta V_1 \cdot q_{10}}{2} = 1.17 \times 10^{-4} \, \text{A}$ .

Rent = 
$$284 \text{ kJ} 2$$
.

These certificate that.

Av = 9m Rent = 167  $\Rightarrow$  we can choose

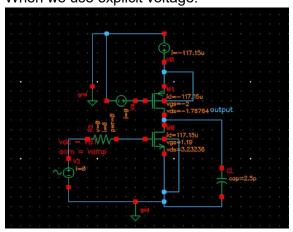
BW =  $\frac{1}{2\pi Rent \cdot C_L} = 224 \text{ kHz}$ 
 $2V_r = 145 \text{ V}$ 
 $2V_r = 145 \text{ V}$ 
 $2V_r = 145 \text{ V}$ 

$$W_{1} = \frac{21pL}{(MGx)_{0} \circ V_{1}^{2}} = \frac{2 \times 117 \times 50 \times 10^{-6}}{90 \times 0.59^{2}} = \frac{80MM}{80M}$$

$$W_{1} = \frac{21pL}{(MGx)_{0} \circ V_{1}^{2}} = \frac{2 \times 117 \times 50 \times 10^{-6}}{30 \times 1.4 \times 2} = \frac{24.4Mm}{20 \times 1.4 \times 2}$$

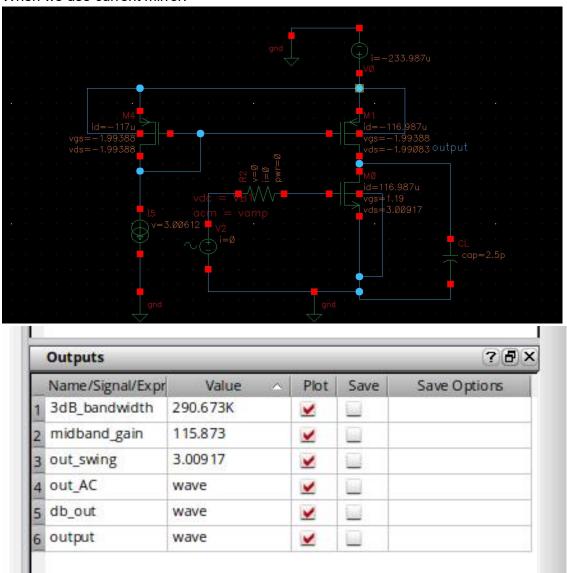
when we use this Ws to build a current mirror . ne found that specs is what we want.

# Simulation 2: When we use explicit voltage:



	Outputs ? 5 ×					
	Name/Signal/Expr	Value	^	Plot	Save	Save Options
1	3dB_bandwidth	326.624K		~		
2	midband_gain	103.614		~	160	
3	out_swing	3.23236		~		
4	out_AC	wave		~	lisi	
5	db_out	wave		~		
6	output	wave		~	160	

### When we use current mirror:



	Hand-calculation	Simulation with	Simulation with
		current mirror	explicit voltage bias
bandwidth	224kHz	290.673kHz	326.624kHz
Midband gain	120	115.873	103.614
Out swing	3.15	3.01	3.23

Now we can explain some questions of our designs.

- We found that using explicit voltage sources to bias amplifiers is not good practice, it is because as we need different voltage to bias transister, it is not very realistic that a piece of IC connected to many different power supplies. Additionally, explicit voltage sources introduce noises to the system.
- 2. As we rework the biasing network and simulate the gain and bandwidth of our amplifier. These values are different from the gain and bandwidth of your original amplifier. There are several reasons. The Id is very sensitive due to the change of ΔV with explicit voltage bias, the ΔV₂ wouldn't adapted all the time, but with use current mirror, Id is only depends on the ratio of width of M2 and M3. In this part, we ignore the effect of body effect. As we use asymptotic approximation technique, bandwidth is not accurate.
- 3. Calculate the output resistance of the final amplifier and compare it with the output resistance of the CS amplifier used in Task a of Part 1.

In part 1, Rout =  $30k\,\Omega$  approximately as it mainly depends on 1/gm . But in Part2 Rout is very large because output connect to the drain of PMOS and NMOS Rout =  $284\,k\,\Omega$ . In next question we explan why we use this topology.

4. How output resistance affect the gain and bandwidth? In this design, Rout is very large because output connect to the drain of PMOS and NMOS. So the dominant pole is set by Rout\*CL. We got

$$BW = \frac{1}{2 \Pi R_{OUT} C_L}$$

$$\rightarrow BW \propto \frac{1}{R_{OUT}}$$

Midband gain = gm\*R<sub>out</sub>,

→midband gain∝ R<sub>out</sub>

From how output resistance affect the gain and bandwidth, we learned that bandwidth is a trade off of midband gain. From part1 to Part2, we try to get larger gain as bandwidth is reduced. So we are suggested to choose parameters widely.

#### Appendix:

Here we gave out some designs didn't meet all the design specifications before we got the final design. And we provide some solutions to fix them.

1. When we choose VB1 = 1.2V rather than final design VB1=1.19V.



Output swing is too small.

2. At very beginning, we use explicit voltage bias to bias M2, only change the voltage 200mV lower, we got a very large output swing and everything in a mess. It is because one of transisters is in triode.



I tried to change the value of specs and calculated again. And I found that with same expected Id, using current mirror can solve this problem. It is because if we use a current mirror, whether a transistor in saturation or not is not depends on Vbias anymore, the current is set by Ibias.