

Layout Tutorial

Take Bandgap Reference Circuit as an Example

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June 1, 2025

1 Layout Based on Schematic

The first step is to draw the layout (Fig. 2) based on the schematic (Fig. 1).

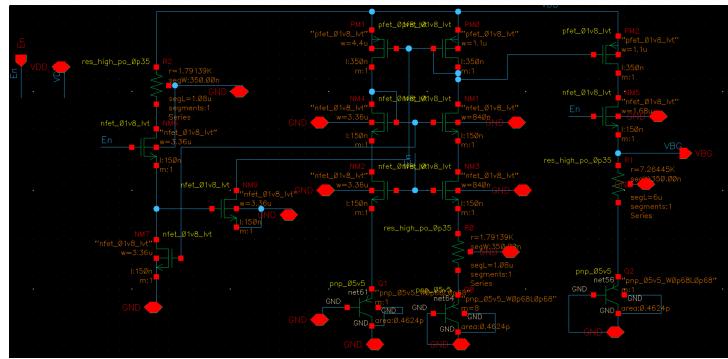
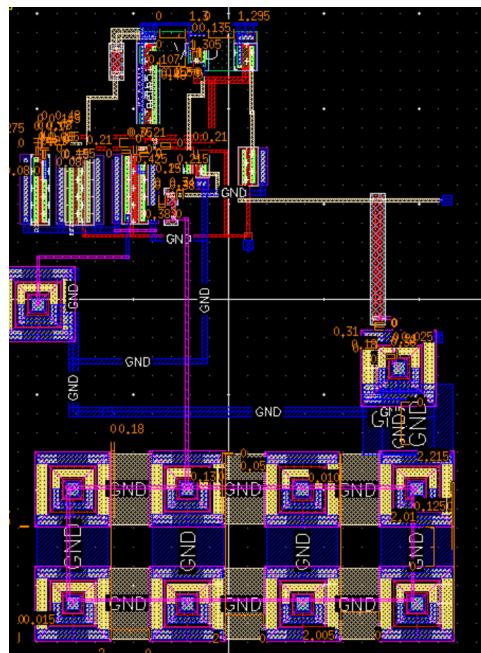


Figure 1: Schematic of the Bandgap Reference



In the following, I will take you through the layout creation process step by step, explaining each key stage along the way.

First, in the schematic window, we open the layout view by selecting **Launch → Layout XL**, then choose **Create New** and enable the **Automatic** option.

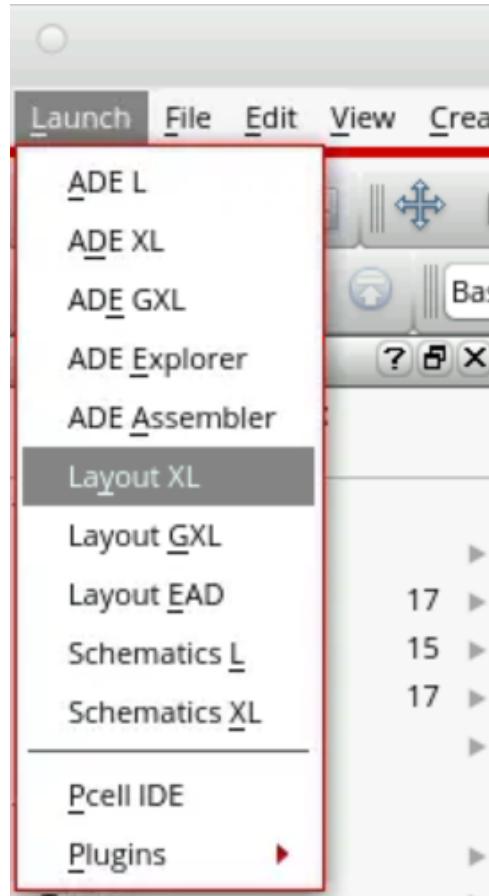


Figure 3: Launching Layout XL from the schematic window via **Launch → Layout XL**.

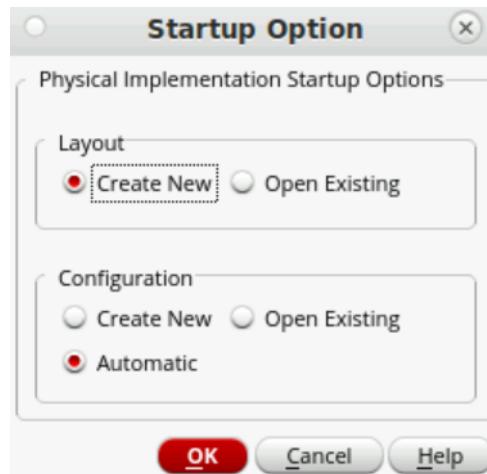


Figure 4: Layout XL Startup Option.

You will then see a blank layout window appear, as illustrated in Fig. 5.

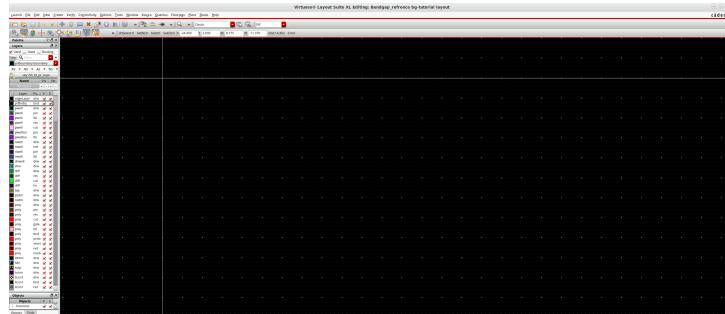


Figure 5: Blank Layout Window.

Next, we can use the **Generate** option in the layout window to bring in the devices from the schematic.

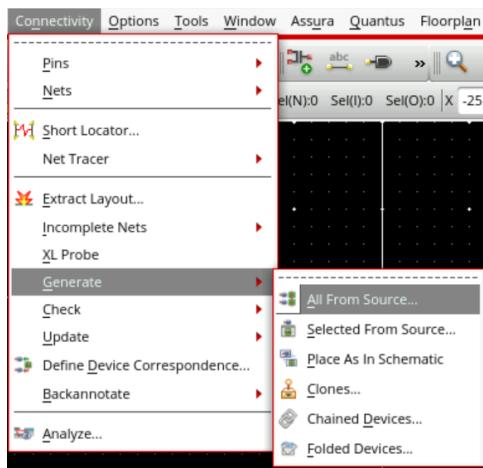


Figure 6: Use **Connectivity → Generate → All From Source** to automatically generate all devices from the schematic into the layout view.

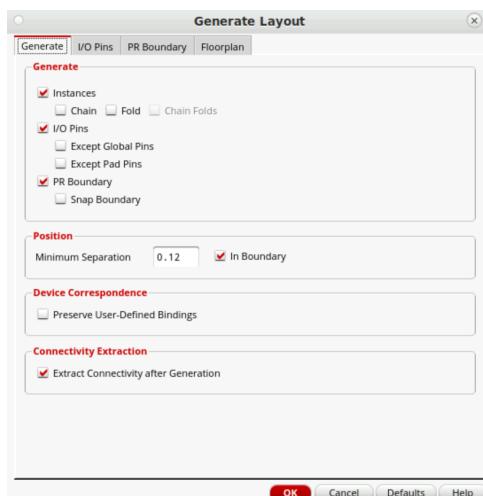


Figure 7: Generate Set

Then, we can see that the devices are placed randomly in the layout view.

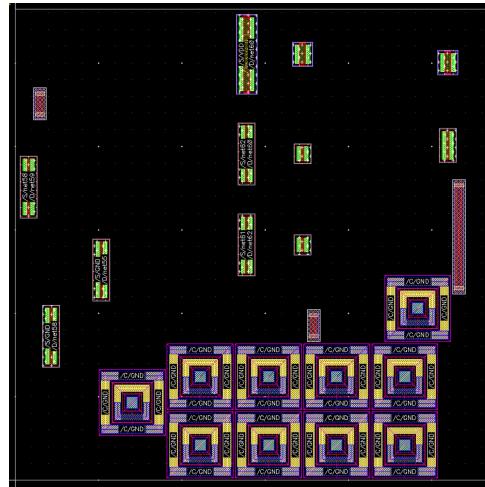


Figure 8: Initial device placement

After device generation, the next step is to wire them according to the schematic connections. To begin wiring, press **p** in the layout window to enter the wire drawing mode.

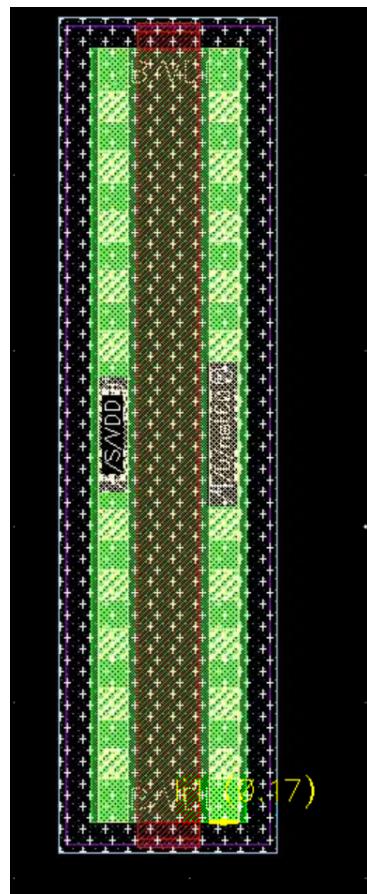


Figure 9: Wiring metal layers using the **p** shortcut in the layout window.

If you want to change the properties of a wire, you can select the wire and press **q**. This will bring up the wire properties window, where you can modify attributes such as the layer material. Commonly used layers include **l11**, **met1**, **met2**, **poly**, and **licon1**.

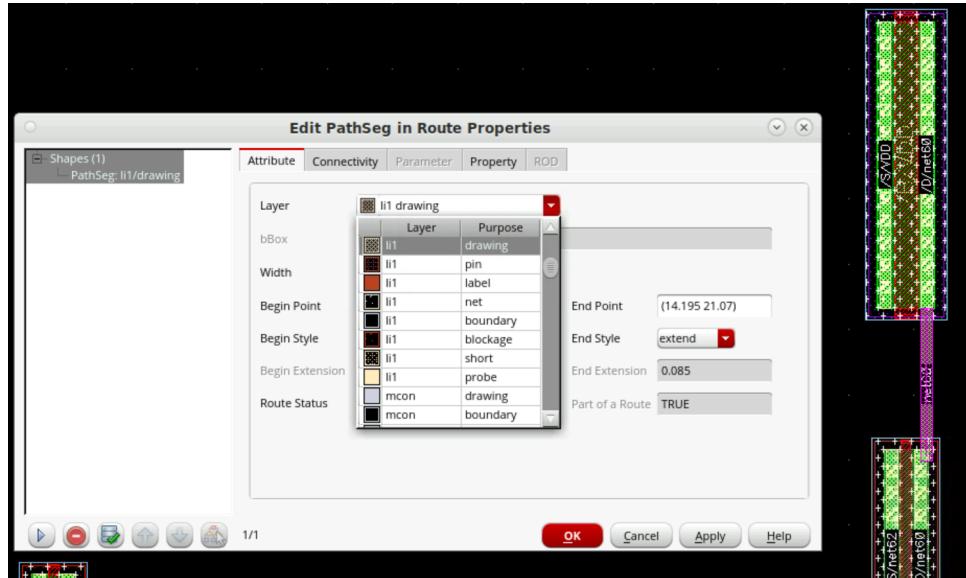


Figure 10: Modifying the layer of a selected wire via the properties window (opened by pressing **q**).

Sometimes, it is necessary to connect two wires made of different metal layers(Fig. 11). In such cases, a *via* must be placed at the intersection point to establish a proper connection between the two layers.

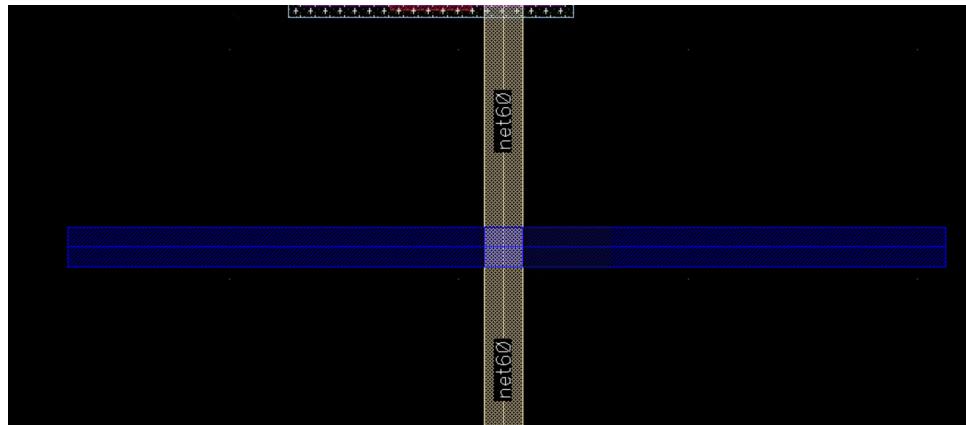


Figure 11: Wire intersection

To create a via, press **o** to open the Create Via dialog. Select the **stack** option, and then choose the two metal layers you want to connect.

Note: Not all pairs of metal layers can form a valid via. You must be aware of the materials used in your wires during design.

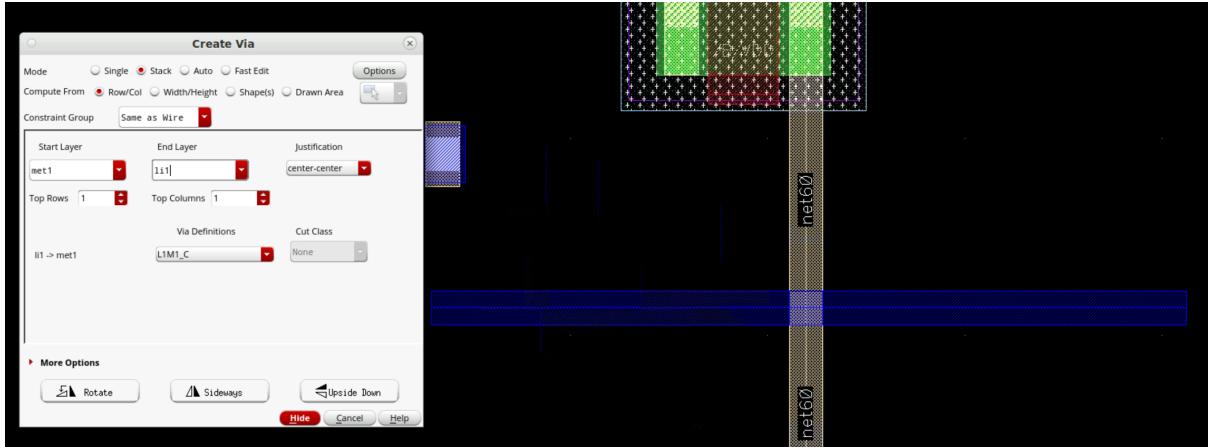


Figure 12: Via Setup

After placing the via, we can observe that both wires are now labeled as `net60`, indicating that they have been successfully connected.

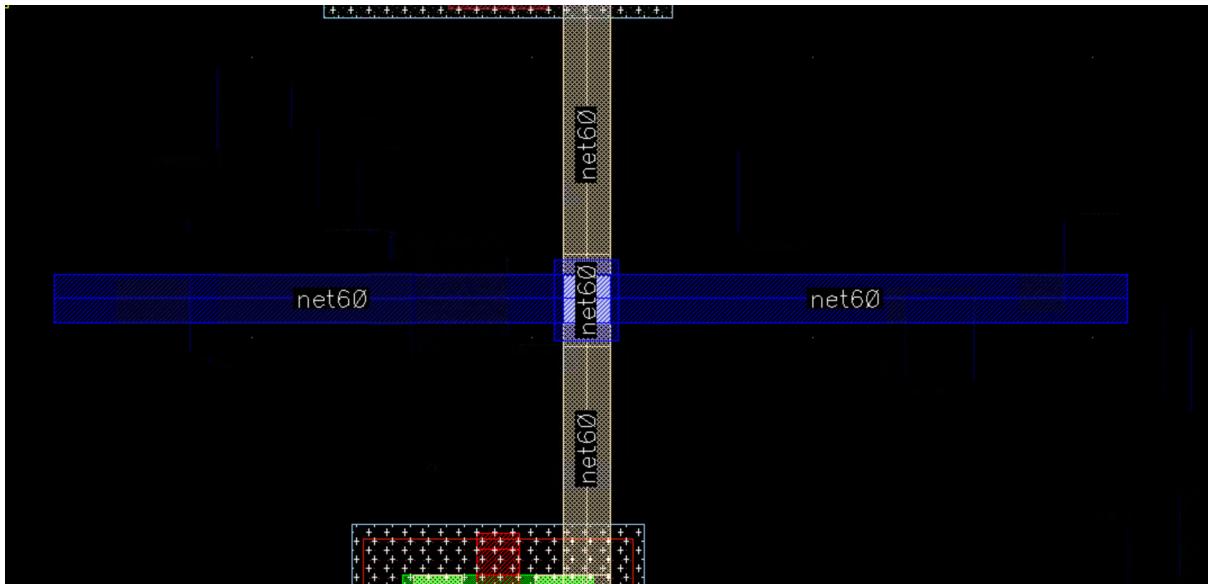


Figure 13: Place a via at the intersection point

For MOS transistors that share the same source or drain node, and have matching dimensions, it is possible to merge them in the layout. By placing their shared terminals close enough so that the diffusion regions overlap, the layout tool will automatically treat them as electrically connected. This technique not only reduces the overall layout area but also helps improve matching and routing efficiency. Here are two examples:

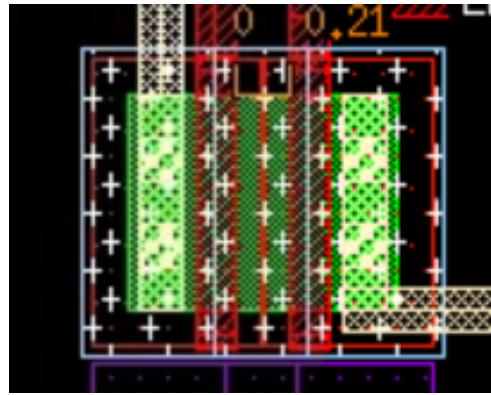


Figure 14: Merge example 1

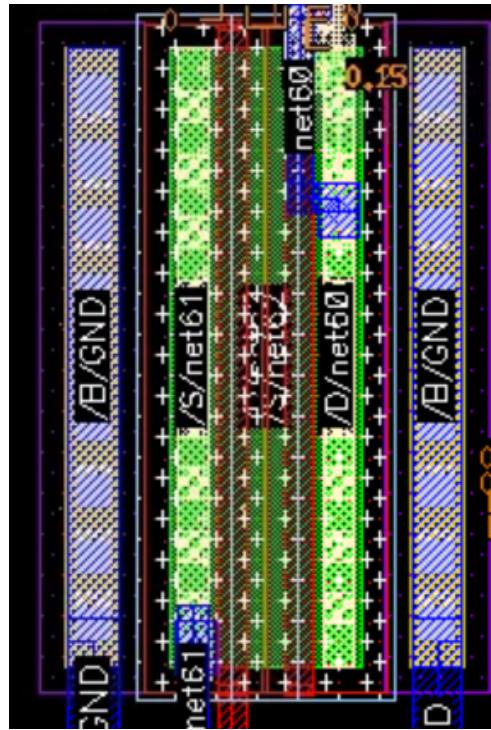


Figure 15: Merge example 2

With these layout techniques in mind, all you need to do is follow the schematic and connect the devices accordingly. While drawing wires, Cadence will display orange guide lines to indicate where each node should be connected(Fig.16). However, I personally use these guides primarily as a way to verify the correctness of the layout after routing, rather than relying on them to guide the wiring process.

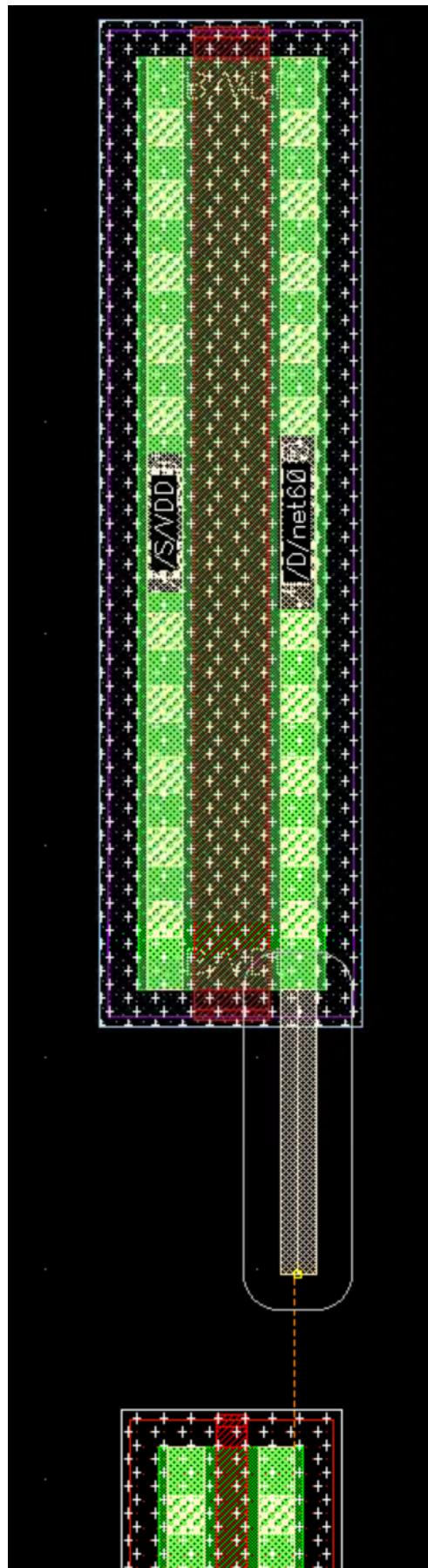


Figure 16: Orange guide line

2 Design Rule Check (DRC)

To run DRC, run the following commands in your cadence directory:

```
PVS_INST_DIR="/share/instsww/cadence/PEGASUS221"
PVSHOME="${PVS_INST_DIR}" ; export PVSHOME
PATH="$PVSHOME/tools/bin:$PATH"

export PEGASUS_DRC=".:/sky130_release_0.0.4/Sky130_DRC"

cd cadence
pegasus -drc -dp 12 -license_dp_continue -gds bg.gds -top_cell bg -ui_data ./
sky130_release_0.0.4/Sky130_DRC/sky130_rev_0.0_1.0.drc.pvl
```

Note: In the last line of the command, you need to replace **bg** with the name of your own top cell.

After running the command, you will see output in the terminal including the cell summary(Fig.18), error information(Fig.19), and Pegasus processing details(Fig.20).

```
eda-1 [444] ~/cadence > PVS_INST_DIR="/share/instsww/cadence/PEGASUS221"
eda-1 [445] ~/cadence >
eda-1 [445] ~/cadence > PVSHOME="$PVS_INST_DIR" ; export PVSHOME
eda-1 [446] ~/cadence > PATH="$PVSHOME/tools/bin:$PATH"
eda-1 [447] ~/cadence > export PEGASUS_DRC=".:/sky130_release_0.0.4/Sky130_DRC"
eda-1 [448] ~/cadence > pegasus -drc -dp 12 -license_dp_continue -gds bg.gds -top_cell bg -ui_data .:/sky130_release_0.0.4/Sky130_DRC/sky130_rev_0.0_1.0.drc.pvl
Pegasus version 22.14-5987 released on 2025-06-01 15:17:44 649949 eda-1.EECS.Berkeley.EDU
Copyright (c) 2023 Cadence Design Systems, Inc.
All rights reserved worldwide.

INFO: Command line Options: -drc -dp 12 -license_dp_continue -gds bg.gds -top_cell bg -ui_data .:/sky130_release_0.0.4/Sky130_DRC/sky130_rev_0.0_1.0.drc.pvl
INFO: check host Model: AND EPIC 01544 M-Core Processor, 6G Red Hat Enterprise Linux release 8.10 (Ootpa), Logical cores: 48, Physical cores: 48, Cache: 1024 KB, CPU Speed: 1500 MHz
INFO: Launch host Memory: MemTotal: 773217 MB, MemFree: 413834 MB, SwapTotal: 32767 MB, SwapFree: 32582 MB, VmallocTotal: 13421772799 MB, VmallocUsed: 869 MB
INFO: Current path: /home/aa/users/cs199-cdt/cadence
INFO: Run directory same as current path
INFO: Setting LAYOUT_PATH to: /home/aa/users/cs199-cdt/cadence/cadence/pegasus-1748816264-eda-1.EECS.Berkeley.EDU-649949
WARNING: The option -license_dp_continue is not available in this product.
INFO: Setting LAYOUT_PRIMARY to: bg
INFO: Setting LAYOUT_PRIM to: bg
INFO: PEGASUS running
WARNING: Cmd-line override: LAYOUT_PATH "/home/aa/users/cs199-cdt/cadence/bg.gds";
WARNING: Cmd-line override: LAYOUT_PRIMARY "bg";
WARNING: Cmd-line override: LAYOUT_PRIM "bg";
WARNING: Cmd-line override: LAYOUT_PRIMARY "bg";
INFO: See "/home/aa/users/cs199-cdt/cadence/pegasus-1748816264-eda-1.EECS.Berkeley.EDU-649949/pvl.log" for additional details.
INFO: Checking out 2 license(s) of feature: 'Pegasus DRC' version 22.1
INFO: License checkout ...
INFO: Checking out 1 license(s) of feature: 'Pegasus 16nm' version 22.1
INFO: License checkout successful ...
INFO: Odsll input summary
File name: /home/aa/users/cs199-cdt/cadence/bg.gds
File size: 49152
VERSION: 1.0
Library name: Bandgap_refrence
Last modified: 2025-4-22 16:20:52
Last accessed: 2025-4-22 19:34:28
```

Figure 17: DRC code running

Cell Summary:						
CELL	INSTANCE	GEOMETRY	LABELS	HREF	FREF	
L1M1_C_CDNS_745375668180	0	3	0	10	10	
M1M2_C_CDNS_745375668181	0	3	0	14	14	
L1M1_C_CDNS_745375668182	0	3	0	2	2	
PYLICON_C_CDNS_745375668183	0	3	0	1	1	
polyConn_CDNS_745375668180	0	6	0	4	4	
pnp_05v5_CDNS_745375668181	0	73	0	10	10	
nfec_01v8_lvt_CDNS_745375668182	0	32	0	1	1	
res_high_po_0p35_CDNS_745375668183	0	10	0	2	2	
res_high_po_0p35_CDNS_745375668184	0	10	0	1	1	
nfec_01v8_lvt_CDNS_745375668185	0	52	0	1	1	
pfec_01v8_lvt_CDNS_745375668186	0	27	0	2	2	
nfec_01v8_lvt_CDNS_745375668187	0	42	0	1	1	
nfec_01v8_lvt_CDNS_745375668188	0	52	0	1	1	
nfec_01v8_lvt_CDNS_745375668189	0	19	0	1	1	
pfec_01v8_lvt_CDNS_7453756681810	0	45	0	1	1	
nfec_01v8_lvt_CDNS_7453756681811	0	42	0	1	1	
nfec_01v8_lvt_CDNS_7453756681812	0	42	0	1	1	
nfec_01v8_lvt_CDNS_7453756681813	0	19	0	1	1	
bg	55	193	0	1	1	
TOTAL CELL = 19; INSTANCE = 55; GEOMETRY = 676; LABEL = 0						

Figure 18: Cell Summary

```

INFO: Rule dnwell.2 completed with no violations, 1/279
INFO: Rule dnwell.3 completed with no violations, 2/279
INFO: Rule dnwell.4 completed with no violations, 3/279
INFO: Rule dnwell.5 completed with no violations, 4/279
INFO: Rule dnwell.7 completed with no violations, 5/279
INFO: Rule hvtp.2 completed with no violations, 6/279
INFO: Rule nwell.5 completed with no violations, 7/279
INFO: Rule hvtp.1 completed with no violations, 8/279
INFO: Rule nwell.6 completed with no violations, 9/279
INFO: Rule nwell.2ab completed with no violations, 10/279
INFO: Rule hvnwell.8 completed with no violations, 11/279
INFO: Rule nwell.1 completed with no violations, 12/279
INFO: Rule hvtp.5 completed with no violations, 13/279
INFO: Rule hvtr.2 completed with no violations, 14/279
INFO: Rule hvtr.1 completed with no violations, 15/279
INFO: Rule hvtp.6 completed with no violations, 16/279
INFO: Rule lvtn.9 completed with no violations, 17/279
INFO: Rule lvtn.1a completed with no violations, 18/279
INFO: Rule lvtn.3a completed with no violations, 19/279
INFO: Rule nwell.4 completed with no violations, 20/279
INFO: Rule ncm.1 completed with no violations, 21/279
INFO: Rule lvtn.12 completed with no violations, 22/279
INFO: Rule lvtn.2 completed with no violations, 23/279
INFO: Rule lvtn.13 completed with no violations, 24/279
INFO: Rule ncm.7 completed with no violations, 25/279
INFO: Rule ncm.2a completed with no violations, 26/279
INFO: Rule ncm.8 completed with no violations, 27/279
INFO: Rule lvtn.14 completed with no violations, 28/279
INFO: Rule vpp.5 completed with no violations, 29/279
INFO: Rule hvtp.3 completed with no violations, 30/279
INFO: Rule lvtn.10 completed with no violations, 31/279
INFO: Rule difftap.4 completed with no violations, 32/279
INFO: Rule difftap.1 completed with no violations, 33/279
INFO: Rule difftap.6 completed with no violations, 34/279
INFO: Rule tnum.8 completed with no violations, 35/279
INFO: Rule tnum.2 completed with no violations, 36/279
INFO: Rule tnum.7 completed with no violations, 37/279
INFO: Rule tnum.6a completed with no violations, 38/279
INFO: Rule tnum.1 completed with no violations, 39/279
INFO: Rule poly.15 completed with no violations, 40/279
INFO: Rule difftap.10 completed with no violations, 41/279
INFO: Rule difftap.9 completed with no violations, 42/279
INFO: Rule poly.1a completed with no violations, 43/279
INFO: Rule poly.2 completed with no violations, 44/279
INFO: Rule difftap.3 completed with no violations, 45/279
INFO: Rule difftap.11 completed with no violations, 46/279
INFO: Rule poly.10 completed with no violations, 47/279
INFO: Rule rpm.11 completed with no violations, 48/279
INFO: Rule rpm.2 completed with no violations, 49/279
INFO: Rule rpm.8 completed with no violations, 50/279
INFO: Rule poly.4 completed with no violations, 51/279
INFO: Rule rpm.6 completed with no violations, 52/279
INFO: Rule rpm.7 completed with no violations, 53/279
INFO: Rule npc.2 completed with no violations, 54/279
INFO: Rule npc.1 completed with no violations, 55/279
INFO: Rule rpm.3 completed with no violations, 56/279
INFO: Rule psd.2 completed with no violations, 57/279
INFO: Rule psd.10a completed with no violations, 58/279
INFO: Rule psd.10b completed with no violations, 59/279
INFO: Rule psd.6 completed with no violations, 60/279
INFO: Rule psd.1 completed with no violations, 61/279
INFO: Rule psd.5a completed with no violations, 62/279
INFO: Rule psd.11 completed with no violations, 63/279
INFO: Rule licon.6 completed with no violations, 64/279
INFO: Rule licon.2 completed with no violations, 65/279

```

Figure 19: ERROR INFO

```

eda-1 [449] ~/cadence > pegasusDesignReview -qry -data ./bg.gds &
[2] 0$2026
eda-1 [450] ~/cadence >
#####
# Pegasus Design Review
#
# Copyright (c) 2003-2023
# Cadence Design Systems, Inc. All rights reserved.
#
# THIS PROGRAM IS CONFIDENTIAL AND PROPRIETARY
# TO CADENCE DESIGN SYSTEMS, INC. AND CONSTITUTES
# A VALUABLE TRADE SECRET.
#
# This work may not be copied, modified, re-published,
# uploaded, executed, or distributed in any way, in any
# medium, whether in whole or in part, without prior
# written permission from Cadence Design Systems, Inc.
#
# INFO: K2_EDITOR is set, enabling geometry editing capability.

INFO: Verifying license...
INFO: License Verification Successful.
INFO: Checking available Memory...
INFO: Initializing Python Interpreter...
INFO: Initializing Tcl Interpreter...
INFO: Initializing Design Review...
INFO: Starting Up Design Review...

Design Review Startup Sequence:
1: Reading K2_STARTUP: /share/instsw/cadence/PEGASUS221/tools/K2/Viewer/Viewer/macros/startup.mac
read_macro("/share/instsw/cadence/PEGASUS221/tools/K2/Viewer/Viewer/macros/startup.mac");
Prog: /share/instsw/cadence/PEGASUS_22.14.000/tools.lnx86/K2/Viewer/bin/amd64/gds_design_review
GDS Design Review with license version 22.14 starting up...

```

Figure 20: Pegasus Environment Setup

Then, you will see the Pegasus GUI interface appear.

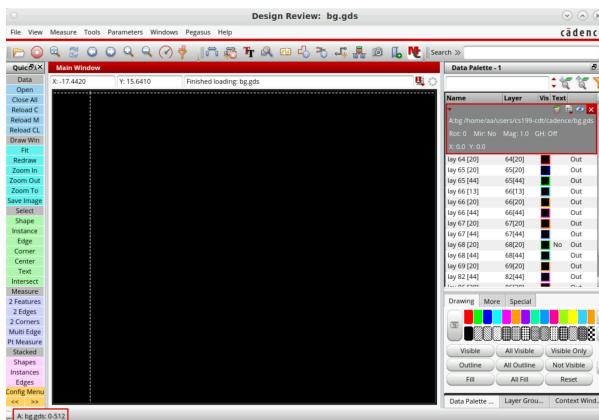


Figure 21: Pegasus GUI

Next, in the Pegasus GUI, click on **Pegasus → Open Run**, and select the file that ends with **.drc_errors.ascii**.

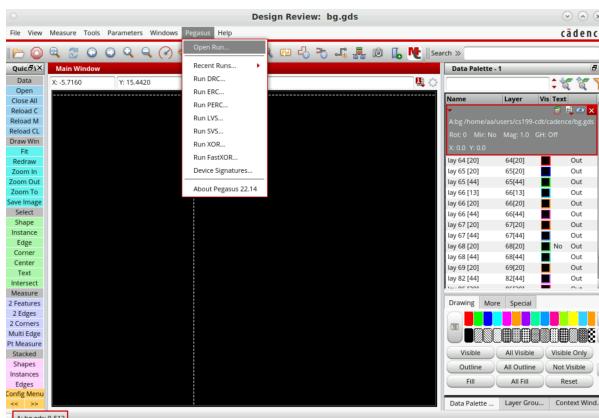


Figure 22: Opening a DRC result file via **Pegasus → Open Run** in the Pegasus GUI.

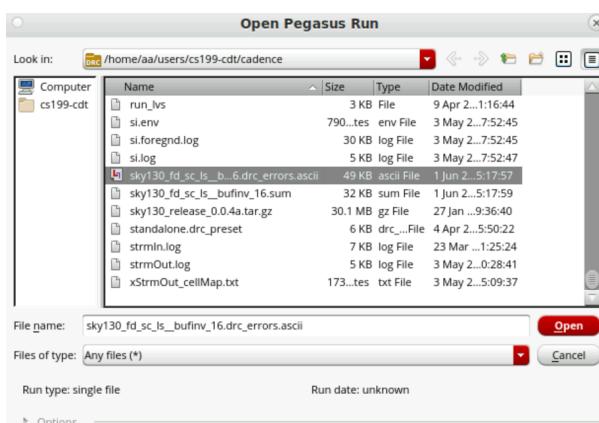


Figure 23: Choosing the **.drc_errors.ascii** file to load DRC results in Pegasus.

After that, you will be able to see the DRC results visualized directly in the Pegasus layout window.

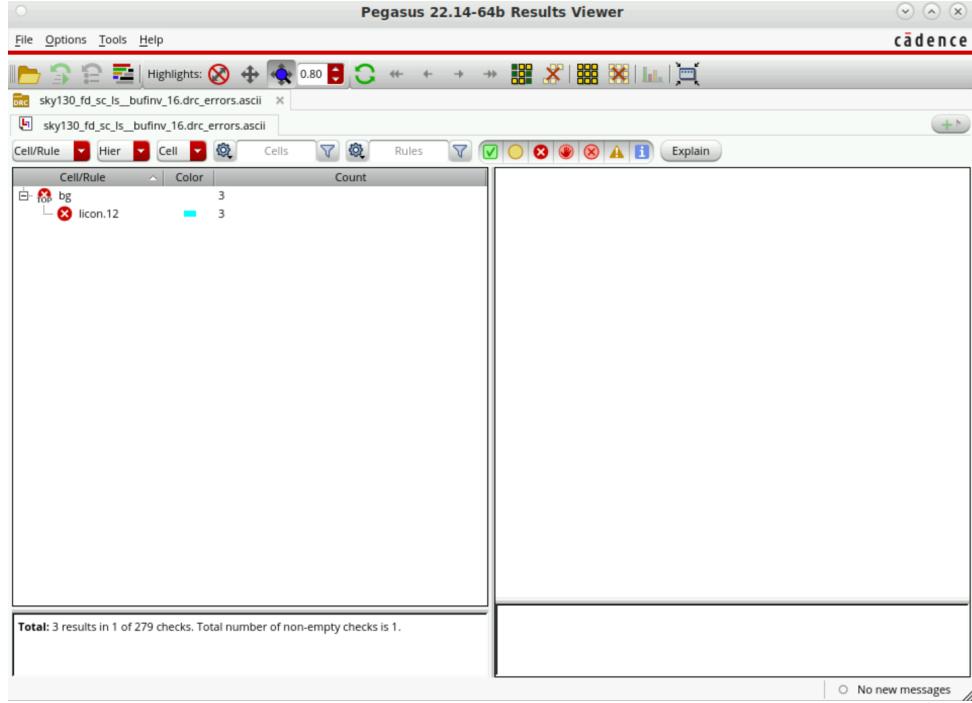


Figure 24: Clean DRC

You might notice that there are several `licon.12` errors. Ignore these. They are due to the fact that the Cadence SKY130 DRC deck is stricter than the actual foundry rules. If you were to sign off on this design, you will run a different DRC deck that will waive these errors.

—From SP25 EECS 251B

At this point, all my DRC errors have been resolved. For reference, I have included a screenshot below showing a layout with multiple DRC violations. By clicking on any highlighted error marker in the Pegasus GUI, you can zoom in to the specific location in the layout where the violation occurs. Additionally, a detailed message describing the violated DRC rule will appear in the bottom-right corner of the window.

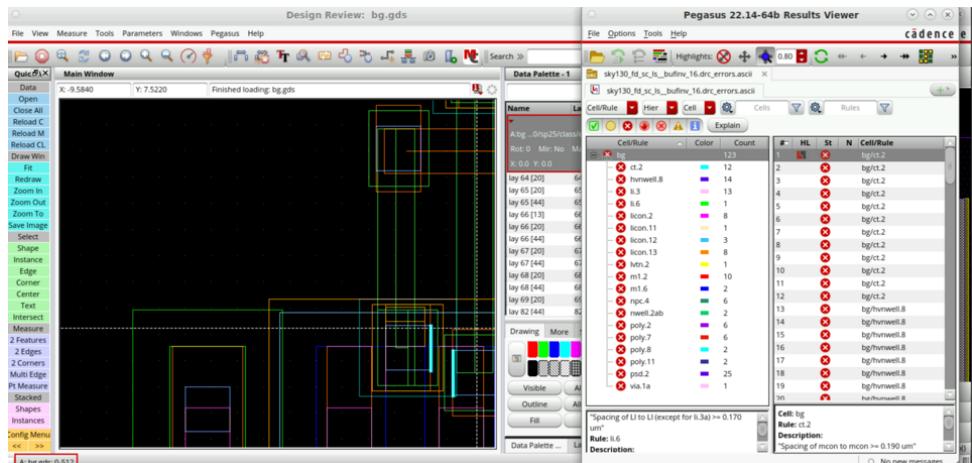


Figure 25: DRC errors example

3 Layout Versus Schematic (LVS)

To run LVS, you first need to export the SPICE netlist from your schematic.

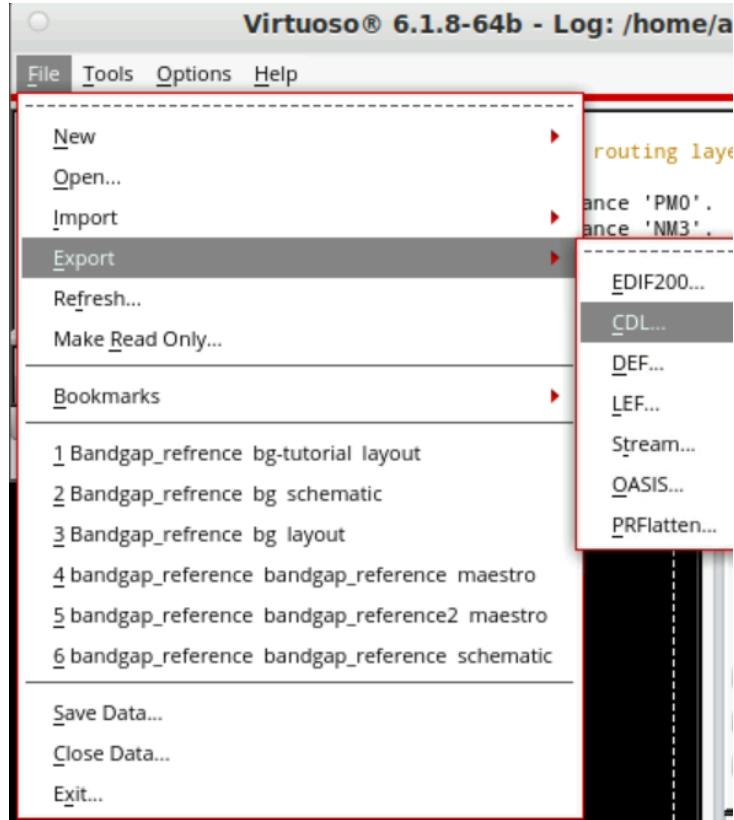


Figure 26: Export Spice Netlist

Since Cadence currently does not support LVS recognition for BJTs in this flow, I replaced the BJT with a PMOS device for the purpose of LVS verification. As a result, the name of the top cell used in the following steps is `bg-replace2`. This does not affect the LVS procedure itself.

```
pegasus -lvs -dp 12 -license_dp_continue -automatch -check_schematic -rc_data  
-ui_data -source_cdl netlist2 -gds bg_replace2.gds -source_top_cell  
bg_replace2 -layout_top_cell bg_replace2 ./sky130_release_0.0.4/Sky130_LVS/  
sky130.lvs.pvl
```

After that, we can view the LVS results. We can also open the LVS report to inspect more detailed information about the comparison.

Figure 27: Run LVS

```
#####
# Run Result : MATCH #
# Run Summary : [INFO] ERC Results: Empty #
# : [INFO] Extraction Clean #
# #
# ERC Summary File : result.sum #
# Extraction Report File : bg_replace2.lvsrpt #
# Comparison Report File : bg_replace2.lvsrpt.cls #
#
#####
INFO: Creating cross reference database ...
INFO: Manager summary: CPU(s): 0 Elapsed(s): 1 Peak memory(MB): 117.35
INFO: Creating cross reference database completed. Sun Jun 1 16:09:21 2025
INFO: Checking in all SoftShare licenses.

Pegasus finished normally. 2025-06-01 16:09:21
```

Figure 28: LVS MATCH Result

```

Open -> bg_replace2.lvsprt.cls
bg_replace2.lvsprt.cls
bg_replace2.lvsprt.cls

=====
# CELL COMPARISON
#
# MATCH <>>> bg_replace2 <><> bg_replace2
#



===== [bg_replace2] =====
STATISTICS
===== [bg_replace2] =====
Original Reduced
Cell | lay : sch | lay : sch
-----+-----+-----+
MP [4 pins] | 3 : 3 | 3 : 3
MP[PFET_01W_LVT) | 3 : 3 | 3 : 3
MN [4 pins] | 11 : 11 | 10 : 10
MN[NFET_01W_LVT) | 11 : 11 | 10 : 10
R [3 pins] | 3 : 3 | 3 : 3
R(RES_HIGH_P0_0P35) | 3 : 3 | 3 : 3
-----+-----+-----+
Total | 17 : 17 | 16 : 16
===== [bg_replace2] =====
Pins | : | 4 : 4
Nets | : | 10 : 10
===== [bg_replace2] =====
DEVICES REMOVED DURING REDUCTION
===== [bg_replace2] =====
Deleted Nets
Cell | Parallel Series Deleted Nets
     | lay : sch | lay : sch | lay : sch
-----+-----+-----+-----+
MN [4 pins] | - : - | 1 : 1 | 1 : 1
MN[NFET_01W_LVT) | - : - | 1 : 1 | 1 : 1
-----+-----+-----+-----+
===== [bg_replace2] =====
INITIAL CORRESPONDENCES
===== [bg_replace2] =====
Type | Name
Pin | En GND VBG VDD
===== [bg_replace2] =====
# END OF REPORT
#
```

Figure 29: LVS MATCH Report

4 PEX and Extracted Simulation

Using a text editor of your choice, create a file called quantus.ccl in cadence that contains the following contents:

```
extract -selection "all" -type "rc_decoupled"
input_db -type pegasus \
    -directory_name ../cadence \
    -run_name "bg_replace2"
output_setup \
    -file_name "bg_replace2.post.sp" \
    -net_name_space "LAYOUT" \
    -temporary_directory_name "bg_replace2"
process_technology \
    -technology_directory "sky130_release_0.0.4/quantus/extraction/typical"
```

Then, run the following code:

```
quantus -cmd quantus.ccl
```

The result should be like this:

```
eda-1 [471] ~/cadence > quantus -cmd quantus.ccl

Cadence Quantus Extraction - 64-bit Parasitic Extractor - Version
22.1.1-p041 Mon Apr 17 07:53:34 PDT 2023
-----
                                         Copyright 2023 Cadence Design Systems,
Inc.

INFO (EXTQRCXLOG-128) : Quantus command line:
Started at: 2025-Jun-01 16:23:46 (2025-Jun-01 23:23:46 GMT)
Executable:
/share/instdsw/cadence/EXT221/tools/extraction/bin/64bit/quantus
Options:   -cmd quantus.ccl
Current working directory: /home/aa/users/cs199-cdt/cadence

INFO (EXTQRCXLOG-103) : The Command File Options for the current Quantus run are as follows:
distributed_processing \
    -multi_cpu 1
extract \
    -selection "all" \
    -type "rc decoupled"
input_db -type pegasus \
    -directory_name "/home/aa/users/cs199-cdt/cadence/../cadence" \
    -run_name "bg_replace2"
output_setup \
    -directory_name "/tmp/qrc_722730" \
    -file_name "bg_replace2.post.sp" \
    -net_name_space "LAYOUT" \
    -temporary_directory_name "bg_replace2"
process_technology \
    -technology_directory \
        "/home/aa/users/cs199-cdt/cadence/sky130_release_0.0.4/quantus/extraction/typical"

-----
Sun Jun 1 16:23:49 2025: BEGIN INPUT stage
```

Figure 30: Run PEX

We named the output file `bg_replace2.post.sp`, so all the extracted parasitic parameters can be found in this file.

```

Open ▾
bg_replace2.post.sp
~/cadence

*
*
*
*           LINUX          Sun Jun  1 16:24:10 2025
*
*
* PROGRAM  advgen
*
* Name       : advgen - Quantus - (64-bit)
* Version    : 22.1.1-p041
* Build Date : Mon Apr 17 07:36:05 PDT 2023
*
* HSPICE LIBRARY
*
* OPERATING TEMPERATURE 25
* ORC_TECH_DIR /home/aa/users/cs199-cdt/cadence/sky130_release_0.0.4/quantus/extraction/typical
*
*
*
*.SUBCKT bg_replace2 VBG En VDD GND
*
* caps2d version: 10
*
* TRANSISTOR CARDS
*
*
MX30/M0 14#2  2#5    VDD#11  VDD    pfet_01v8_lvt L=3.5e-07
+ W=1.1e-06
MX29/M0 2#26   2#3    VDD#8   VDD    pfet_01v8_lvt L=3.5e-07
+ W=1.1e-06
MX28/M0 5#14   2      VDD#1  VDD    pfet_01v8_lvt L=3.5e-07
+ W=4.4e-06
MX30/M0 2#22   5#5    13     GND   nfet_01v8_lvt L=1.5e-07
+ W=8.4e-07
MX35/M0 5#18   5#3    15     GND   nfet_01v8_lvt L=1.5e-07
+ W=3.36e-06
MX34/M0 15     En#5   3#3    GND   nfet_01v8_lvt L=1.5e-07
+ W=3.36e-06
MX33/M0 12#6   5      GND#7  GND   nfet_01v8_lvt L=1.5e-07
+ W=3.36e-06
MX32/M0 10     En#1   12#6  GND   nfet_01v8_lvt L=1.5e-07
+ W=3.36e-06
MX31/M0 14     En#11  VBG#1 GND   nfet_01v8_lvt L=1.5e-07
+ W=1.68e-06
MX27/M0 13     En#9   11    GND   nfet_01v8_lvt L=1.5e-07
+ W=4.4e-07
MX20/M0 2#19   12     GND#3  GND   nfet_01v8_lvt L=1.5e-07
+ W=3.36e-06
MX22/M0 9      En#13  GND#25 GND   nfet_01v8_lvt L=1.5e-07
+ W=8.4e-07
MX21/M0 8      En#7   GND#19 GND   nfet_01v8_lvt L=1.5e-07
+ W=8.4e-07
MX20/M0 3#2   En#3   GND#13 GND   nfet_01v8_lvt L=1.5e-07
+ W=8.4e-07

```

Figure 31: PEX Report

For extracted simulation, we can write a testbench based on the specific analysis requirements:

```

simulator lang=spice

.lib "sky130_release_0.0.4/models/sky130.lib.spice" tt

.include "bg_replace2.post.sp"

VDD (VDD 0) dc 3.3
VSS (GND 0) dc 0
VEn (En 0) dc 2.0

RL (VBG 0) resistor r=100k

Xbg (VBG En VDD GND) bg_replace2

.dc TEMP -40 125 5

.print DC V(VBG)

```

The simulation output will be saved in the file `pex_temp_sweep.print`.