Name :- SHERIN SEBASTIAN
ASUID:-1222858338

EEE 591

LAB #04

1. Full adder schematic and sizing
    a. Explain the sizing criteria used

Length is chosen as 30nm.

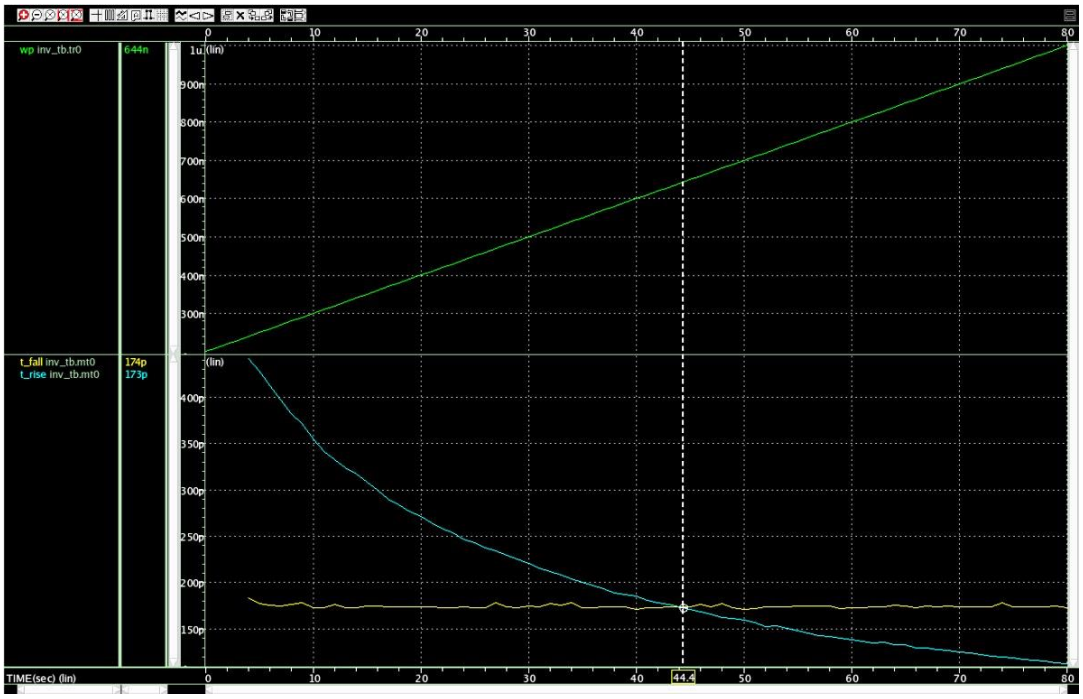
Width of NMOS = 420nm. (Wn = 420nm).

Width of PMOS (wp) = 644nm.

Raising Time and Falling Time is equal. Chosen wp such as Tr = Tf.

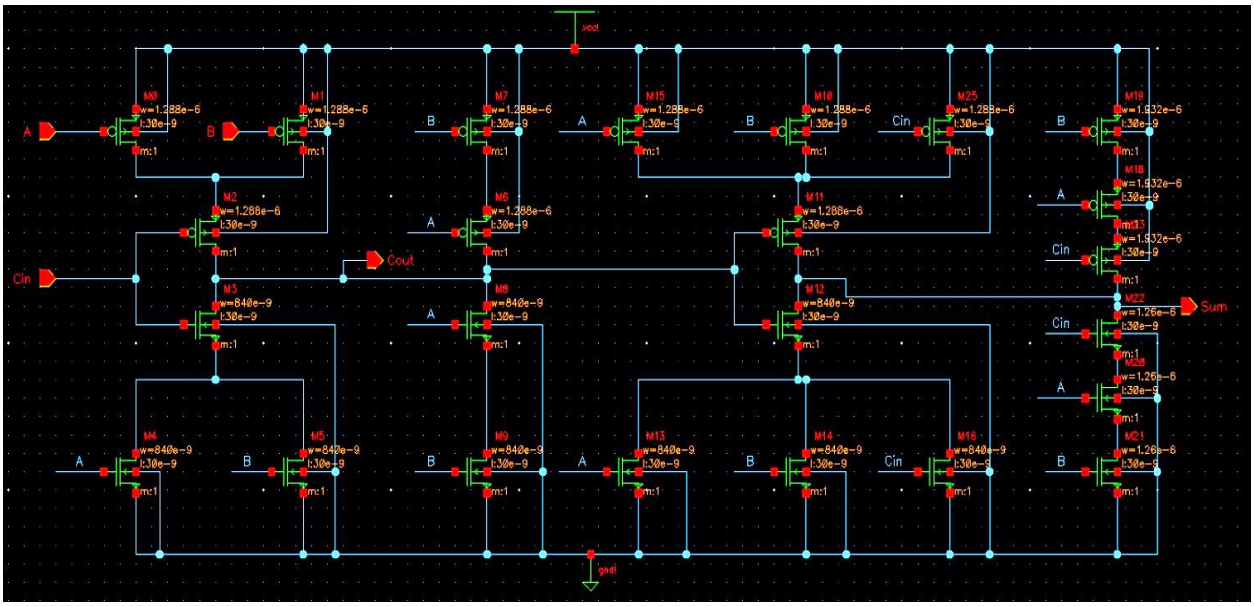
L = 30nm;

For Unit Inverter: Wn = 420nm & Wp = 644nm.



Name :- SHERIN SEBASTIAN
ASUID:-1222858338

FULL BIT ADDER: TRANSISTOR SIZING



Name :- SHERIN SEBASTIAN
ASUID:-1222858338

Sizing

PDN

$$R_{PDN} = R_{N\,inv}$$

$$\frac{2}{\mu_N W_N} = \frac{1}{\mu_N W_{n\,inv}}$$

$$\frac{2}{W_N} = \frac{1}{W_{N\,inv}}$$

$$W_N = 2 W_{N\,inv}$$

$$= 2(420\,nm)$$

$$\boxed{W_N = 840\,nm}$$

PUN

$$R_{PUN} = R_{p\,inv}$$

$$2R_p = R_{p\,inv}$$

$$\frac{2}{\mu_p W_p} = \frac{1}{\mu_p W_{p\,inv}}$$

$$\frac{2}{W_p} = \frac{1}{W_{p\,inv}}$$

$$W_p = 2 W_{p\,inv}$$

$$= 2(644\,nm)$$

$$\boxed{W_p = 1.288\,\mu m}$$

PDN

$$R_{PDN} = R_{N\,inv}$$

$$3R_N = R_{n\,inv}$$

$$\frac{3}{W_n} = \frac{1}{W_{n\,inv}}$$

$$W_n = 3 W_{n\,inv}$$

$$= 3(420\,nm)$$

$$\boxed{W_n = 1.26\,\mu m}$$

PUN

$$R_{PUN} = R_{p\,inv}$$

$$\frac{3}{W_p} = \frac{1}{W_{p\,inv}}$$

$$W_p = 3 W_{p\,inv}$$

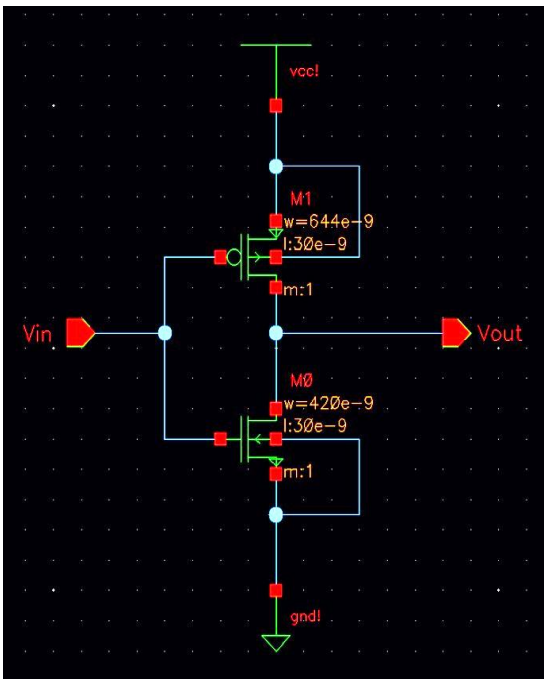
$$= 3(6.44\,nm)$$

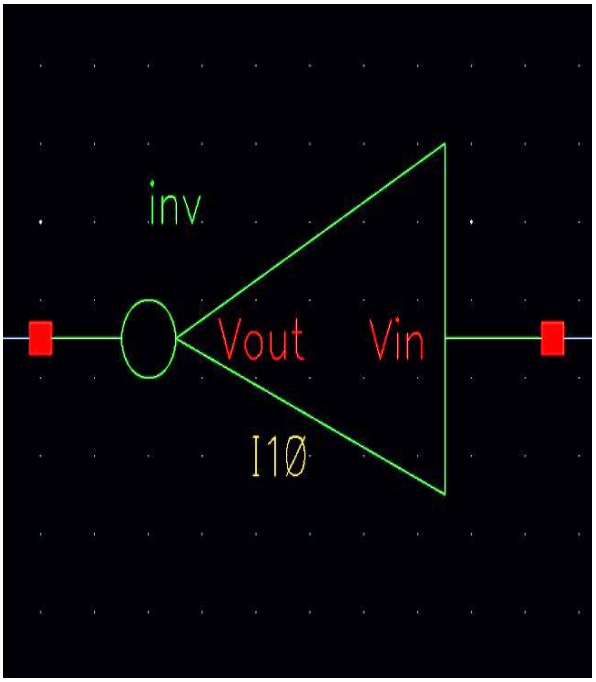
$$\boxed{W_p = 1.932\,\mu m}$$

Name :- SHERIN SEBASTIAN
ASUID:-1222858338

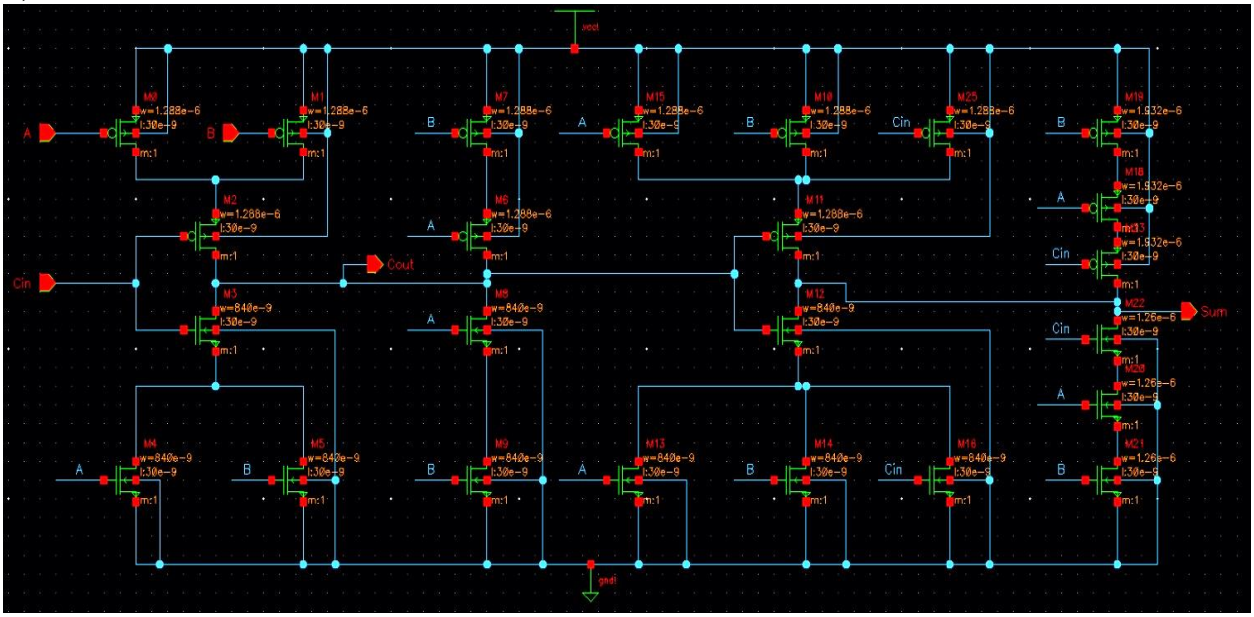
b. Provide the sizes (W/L) of all your transistors

1)INVERTER

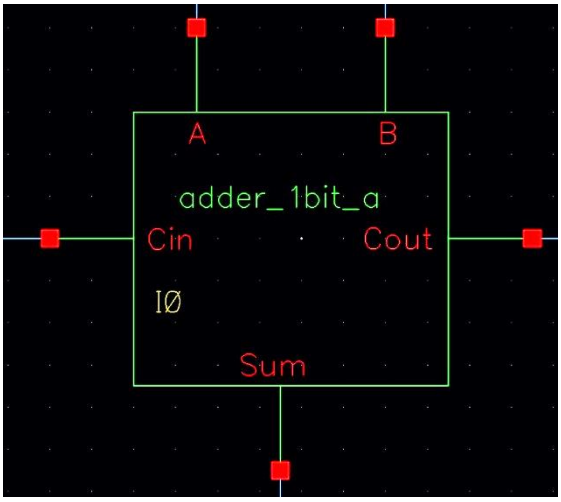




2)ONE BIT ADDER

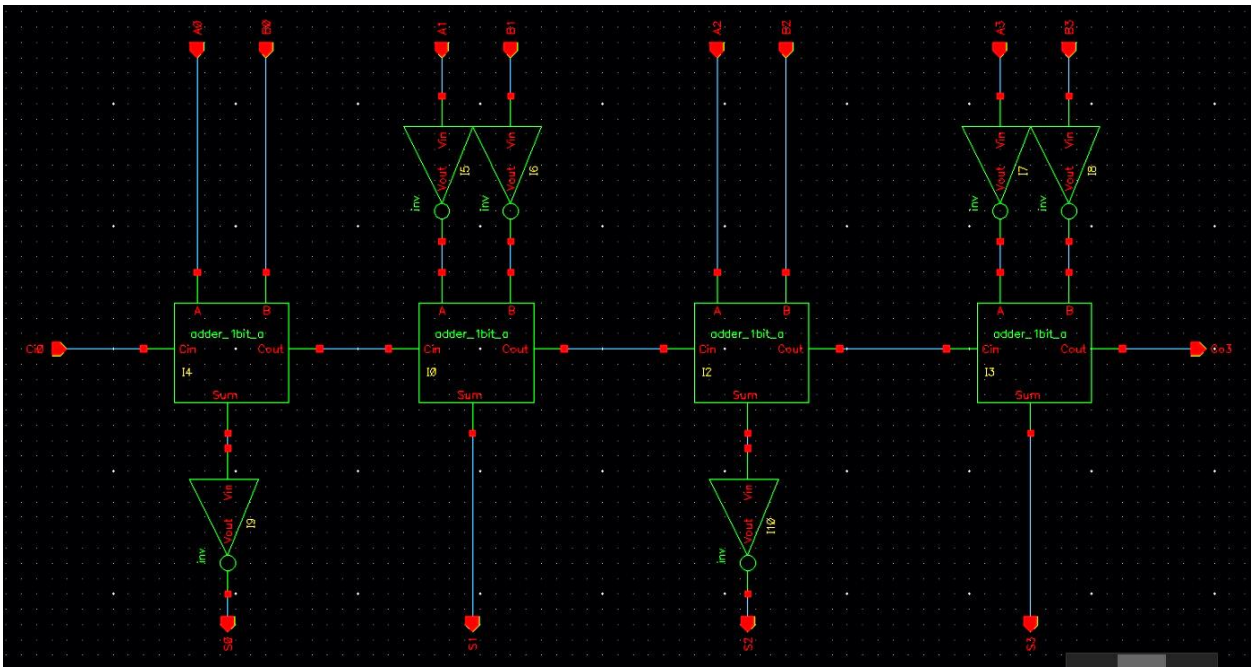


Name :- SHERIN SEBASTIAN
ASUID:-1222858338



c. Provide the schematic of your 4-bit design

MIRROR CIRCUIT ADDER

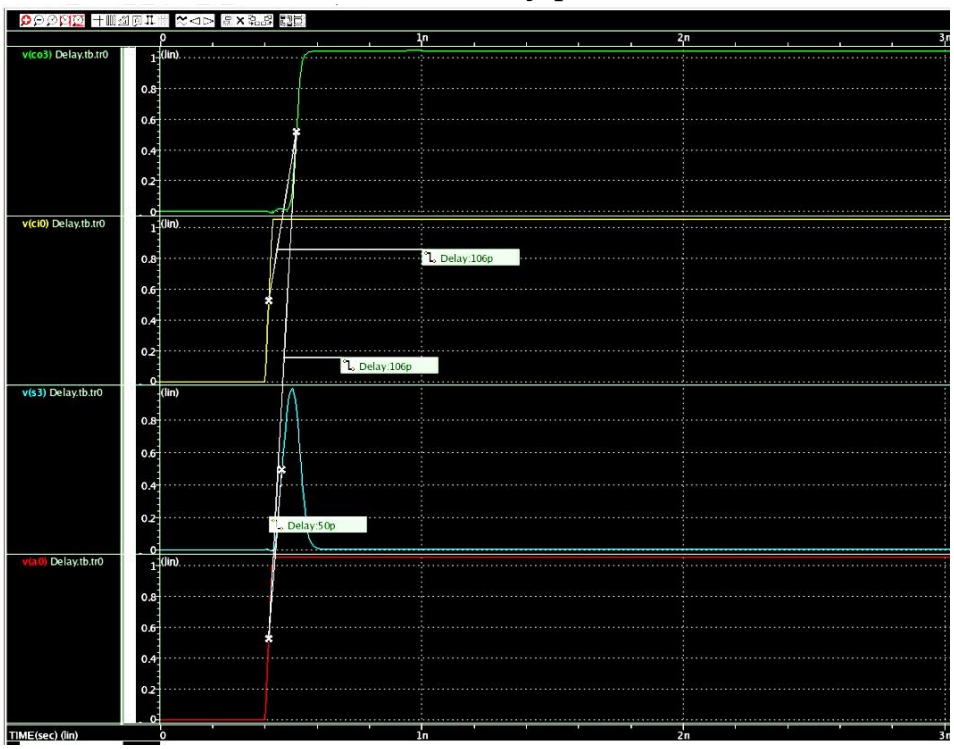


d. Provide any scaling you choose to do for the 4-bit design and justification for the choice
There is no scaling used. Every calculation of width and length depends on the one bit adder for 4 the bit adder.

2. Simulation results

Name :- SHERIN SEBASTIAN
ASUID:-1222858338

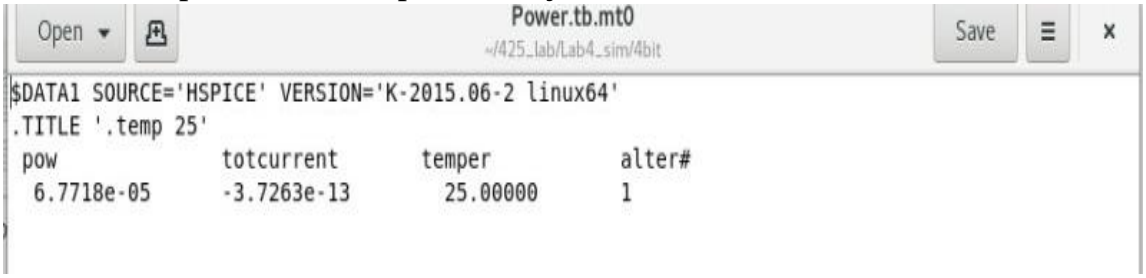
a. Include the worst case delay plots



50% transition time from simulation transient graph.

1. **Sum(S3)** with respect to **A0**	**50ps**
2. **Carry Out (Co3)** with respect to **A0**	**106ps**
3. **Carry Out (Co3)** with respect to **Carry Out (Ci0)**	**106ps**

b. Include the power consumption analysis results

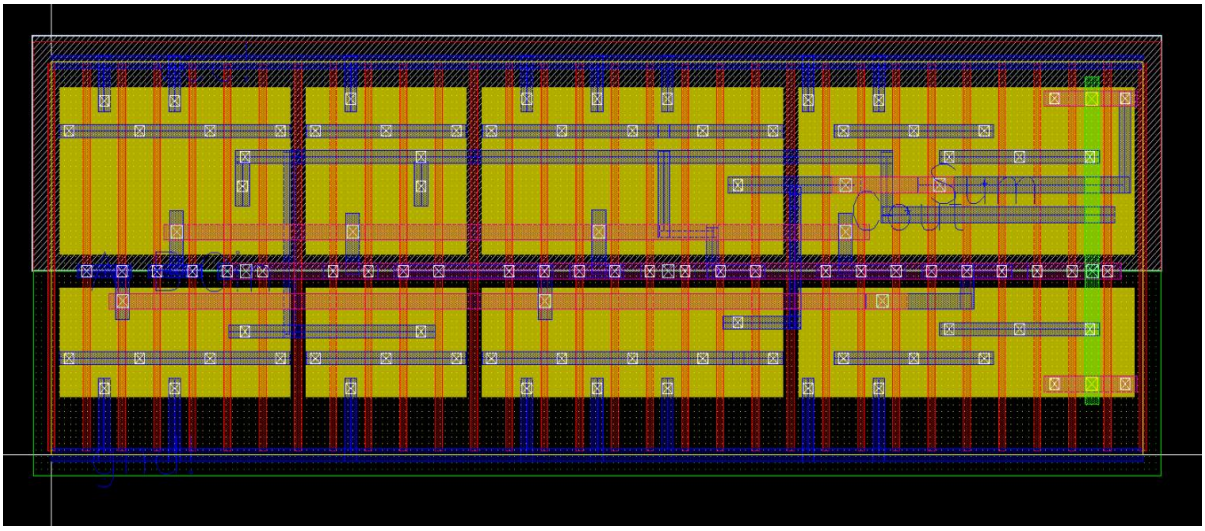


Power = 67.718uW

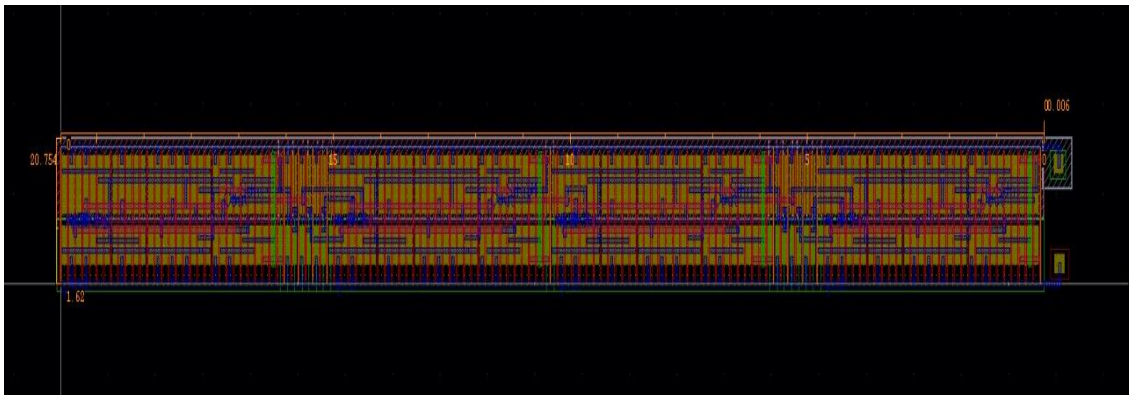
3. Include confirmation of
   a. Layout & DRC Pass

Name :- SHERIN SEBASTIAN
ASUID:-1222858338

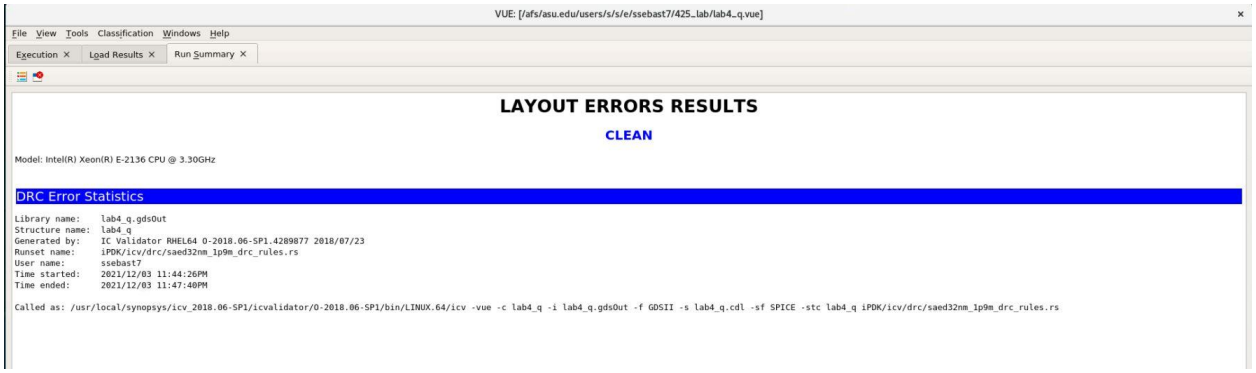
LAYOUT OF 1-BIT ADDER



LAYOUT OF 4 BIT ADDER

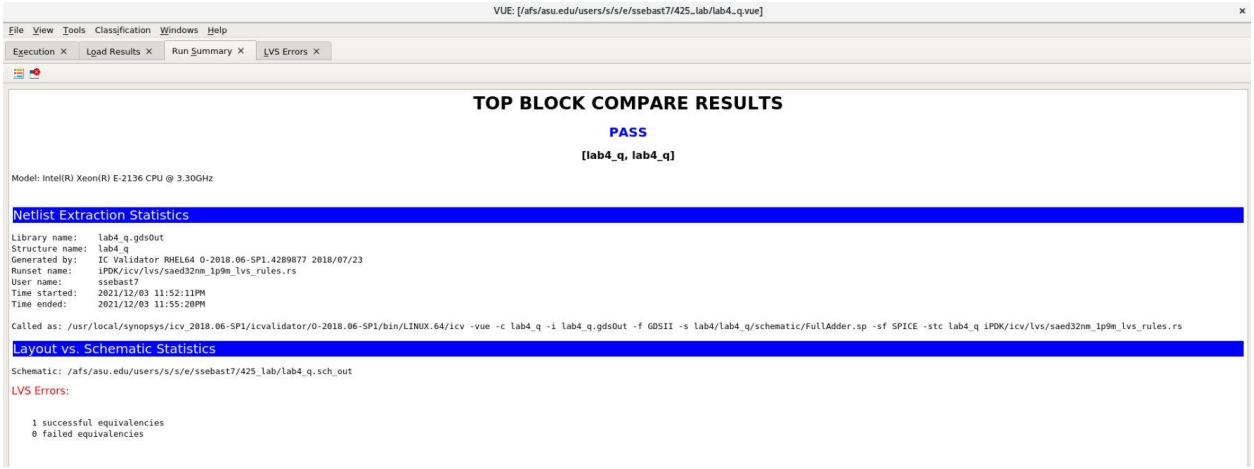


DRC

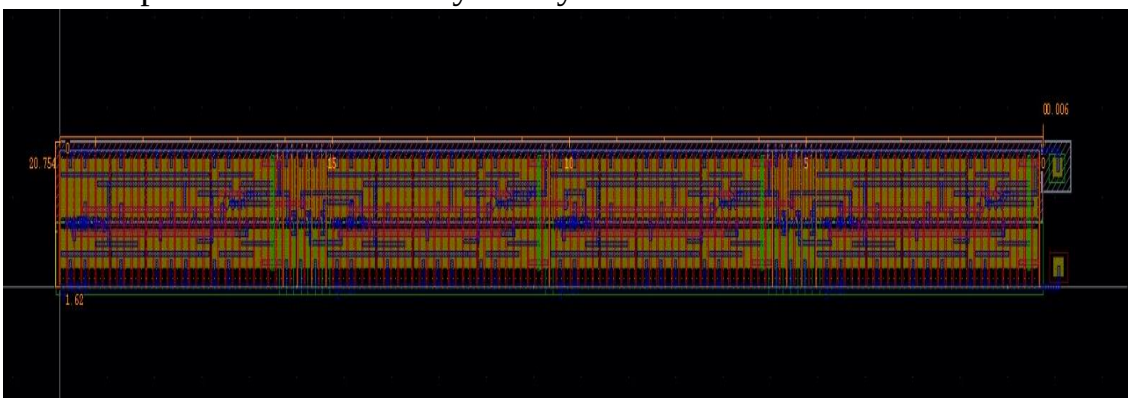


b. Layout & LVS Pass
LVS

Name :- SHERIN SEBASTIAN
ASUID:-1222858338



4. Report the total area of your layout



Width = 20.754um
Height = 1.62um
Area = Width*Height = 20.754um * 1.62um = 33.6214 um^2
Area = 33.6214 um^2

5. Report your overall score as outlined in the lab document

Score=(400ps/delay)+(100uW/power)+(150um^2/area)
Delay = 50ps
Power = 66.718uW
Area = 33.6214 um^2
Score= 8 + 1.49 + 4.4614
Score = 13.9514

Name :- SHERIN SEBASTIAN
ASUID:-1222858338