ELEC 301

Mini-Project 3 Report

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1. Introduction

In this mini project, we explore the following multi-transistor amplifiers: cascaded, cascaded, and the differential amplifier. We examine biassing these amplifiers to satisfy specifications and explore some of their applications, including as repeaters and as AM modulators. All these amplifiers were simulated using the LTSpice software.

2. Mini Project

Part 1

We are given some specifications: maximum value of R_{out} = 2.5kΩ + 250Ω, minimum value of R_{in} = 3.5kΩ, a minimum gain $|A_m|$= 50 V/V, and a maximum low cut-in frequency of 1200Hz. Some value we have are V_{cc} = 20V, base capacitance C_B = 200μF. We also used the 2N3904 transistor, which has V_{BE} = 0.65V [1] and β = 300.

Since $R_C = R_{out}$, R_C = 2.5kΩ, and using the standard resistor values in [2], R_C for our cascode amplifier will be 2.4kΩ, which is within the specifications provided.

Using the ¼ rule from equations 1 to 5, we get the values of the voltages.

$$V_{C2} = \frac{3}{4}V_{CC} = 15\ V \tag{1}$$

$$V_{E2} = V_{C1} = \frac{1}{2}V_{CC} = 10\ V \tag{2}$$

$$V_{E1} = \frac{1}{4}V_{CC} = 5\ V \tag{3}$$

$$V_{B2} = V_{E2} + V_{BE} = 10.65\ V \tag{4}$$

$$V_{B1} = V_{E1} + V_{BE} = 5.65\ V \tag{5}$$

From these voltages, we can solve for the currents from equations 6 to 10.

$$I_{C2} = \frac{V_{CC} - V_{C2}}{R_C} = 2.0833\ mA \tag{6}$$

$$I_{B2} = \frac{1}{\beta} \times I_{C2} = 6.9444\ \mu A \quad (7)$$

$$I_{E2} = I_{C1} = I_{C2} + I_{B2} = 2.0903\ mA \quad (8)$$

$$I_{B1} = \frac{1}{\beta} \times I_{C1} = 18.0555\ \mu A \quad (9)$$

$$I_{E1} = I_{B1} + I_{C1} = 2.1083\ mA \quad (10)$$

Using the ¼ rule, we get the following currents through equations 11, 12, and 13.

$$I_1 = 0.1\ I_{E1} = 0.2108\ mA \quad (11)$$

$$I_2 = I_1 - I_{B2} = 0.2038\ mA \quad (12)$$

$$I_3 = I_2 - I_{B1} = 0.1858\ mA \quad (13)$$

We get the resistance values in equations 14 to 17, with standard resistances beside the calculated values.

$$R_E = \frac{V_{E1}}{I_{E1}} = 2372\Omega \approx 2.4\ k\Omega \quad (14)$$

$$R_{B1} = \frac{V_{CC} - V_{B2}}{I_1} = 44347\Omega \approx 43\text{k}\Omega \quad (15)$$

$$R_{B2} = \frac{V_{B2} - V_{B1}}{I_2} = 24523\Omega \approx 24k\Omega \quad (16)$$

$$R_{B3} = \frac{V_{B1}}{I_3} = 30403\Omega \approx 30k\Omega \quad (17)$$

The small signal transconductance for transistors Q1 and Q2, respectively, are 81.4167mS and 83.3333 mS while the small signal resistance r_π for Q1 and Q2, respectively, are 3588Ω and 3600Ω. Their general formula can be found in equations 18 and 19. We use 3.6kΩ resistors for the simulation for both $r_{\pi 1}$ and $r_{\pi 2}$.

We then check the input resistance through equation 18 and find that we still need 655Ω to satisfy the minimum R_{in}. So, we add a resistance R_x (680Ω) next to source resistance R_s.

$$R_{in} = R_{B2} \,||\, R_{B3} \,||\, r_{\pi 1} = 2845\Omega \tag{18}$$

$$g_m = \frac{I_C}{V_T} \tag{19}$$

$$r_\pi = \frac{\beta}{g_m} \tag{20}$$

From [3], we know that C_{C1} shorts first, hence we use the open-circuit time constant test on C_{C1} and the short-circuit time constant test on C_E. This gives us equations 21 and 22.

$$\tau_{C_{C1}}^{OC} = C_{C1} \times \left(\left(R_S + R_x\right) + R_{B2} || \, R_{B3} \,||\, \left(r_{\pi 1} + (1+\beta) \times R_E\right)\right) = C_{C1} \times 14.05k\Omega \tag{21}$$

$$\tau_{C_E}^{SC} = C_E \times \left(R_E || \left(\frac{1}{1+\beta}\right) \times \left(r_{\pi 1} + \left(R_{B3} || R_{B2} \,||\, (R_S + R_x)\right)\right)\right) = C_E \times 14.14\Omega \tag{22}$$

From the above equations, we see that C_E 'sees' a smaller resistance, so it will be the dominant pole. A zero can be found through equation 23. We account for this when calculating the cut-in frequency, and through this, we use equation 24 to compute for C_E.

Using [2], we set the value of C_E to be 57µF, with a 10µF and a 47µF capacitors in parallel to each other in practice. We also set C_{C1} and C_{C2} to be 57µF, also with a 10µF and a 47µF capacitors in parallel. The simulated circuit can be found in figure 1.

$$\omega_{LZ} = \frac{1}{R_E C_E} = 7.1536\ rad/s \tag{23}$$

$$\omega_{L3dB} = 1200 = \sqrt{\left(\frac{1}{\tau_{C_E}^{SC}}\right)^2 - 2(\omega_{LZ})^2} \rightarrow\ C_E = 58.9445\ \mu F \tag{24}$$

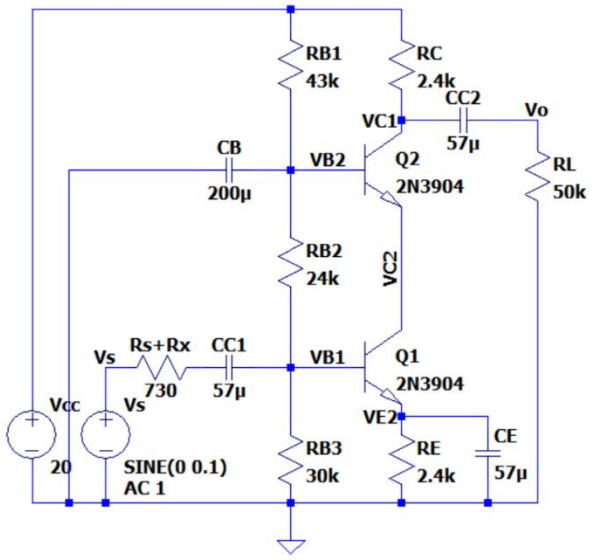

Figure 1. The simulated circuit for part 1.

1A.

The D.C. operating point values of the circuit in figure 1 are given in table 1.

	I_B	I_C	I_E	V_B	V_C	V_E
Q2	6.944µA	2.084mA	2.090mA	6.143V	10.69V	5.467V
Q1	18.056µA	2.090mA	2.108mA	11.366V	14.568V	10.69V

Table 1. D.C. operating point values for the two transistors in figure 1.

1B.

To calculate the high-frequency pole, we use equations 25 to 30.

$$C_\pi = 2 \times CJE + TF \times g_m = 9.237pF \tag{25}$$

$$C_\mu = \frac{CJC}{(1 + \frac{V_{CB}}{VJC})^{MJC}} = 2.014pF \tag{26}$$

$$\omega_{HP1} = \frac{1}{(C_\pi + 2C_\mu)(r_\pi || R_{B2} || R_{B3} || (R_S + R_X))} = 129.763Mrad/s \tag{27}$$

$$\omega_{HP2} = \frac{1}{C_\mu (R_C || R_L)} = 216.816Mrad/s \tag{28}$$

$$\omega_{HP3} = \frac{1}{(C_\pi + 2C_\mu)(\frac{r_{\pi 2}}{1+\beta})} = 6.303Grad/s \quad (29)$$

$$\omega_{H3dB} = \frac{1}{\sqrt{(\frac{1}{\omega_{HP1}})^2 + (\frac{1}{\omega_{HP2}})^2 + (\frac{1}{\omega_{HP3}})^2}} = 111.33Mrad/s \rightarrow 17.7MHz \quad (30)$$

The low frequency pole can be approximated by equation 31.

$$\omega_{L3dB} = \frac{1}{\tau_{C_E}^{SC}} = 1240.98rad/s \rightarrow 197.51Hz \quad (31)$$

The calculated and simulated values from figure 2 are seen in table 2.

	f_{L3dB}	f_{H3dB}
Calculated	197.51 Hz	17.7 MHz
Simulated	217.73 Hz	6.899 MHz

Table 2. The calculated vs simulated poles for the circuit in figure 1.

The calculated and simulated low-frequency poles are close to each other. However, the high frequency poles are further away. This might be due to approximations made in the calculations of the high-frequency poles. Analogous differences in values for the high frequency pole can be seen in [3].

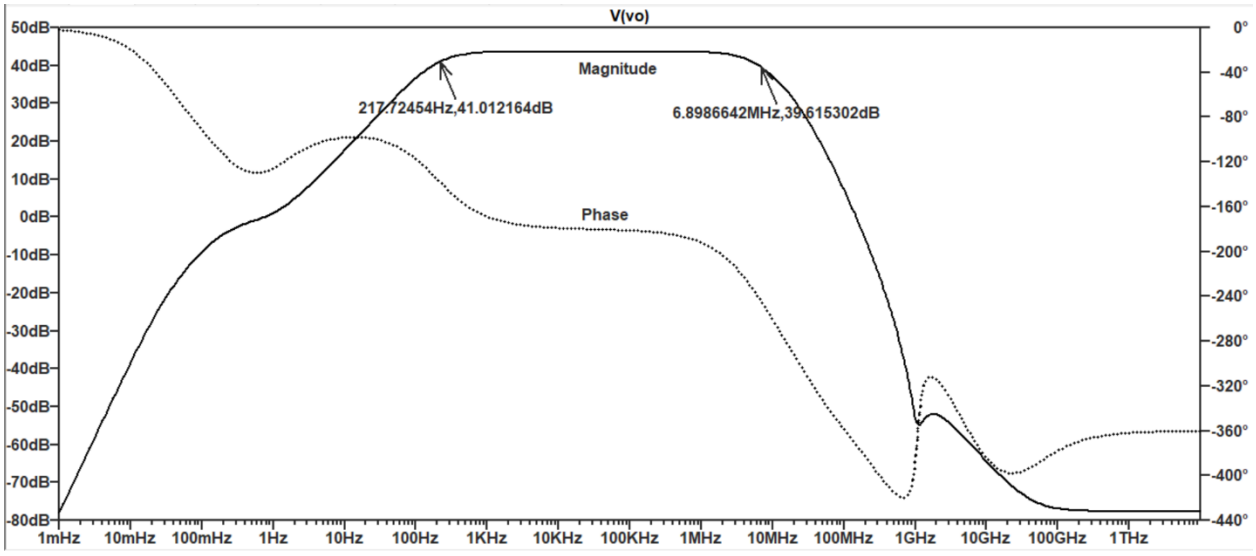

Figure 2. The Bode plot of the circuit in figure 1.

1C.

We pick the midband frequency to be 24.361kHz, the geometric mean of the simulated values in table 2. To vary the amplitude, we use transient analysis, applying a sinusoid to the input.

From figure 3, we can approximate the start of the non-linear part of the curve to be at 50mV.

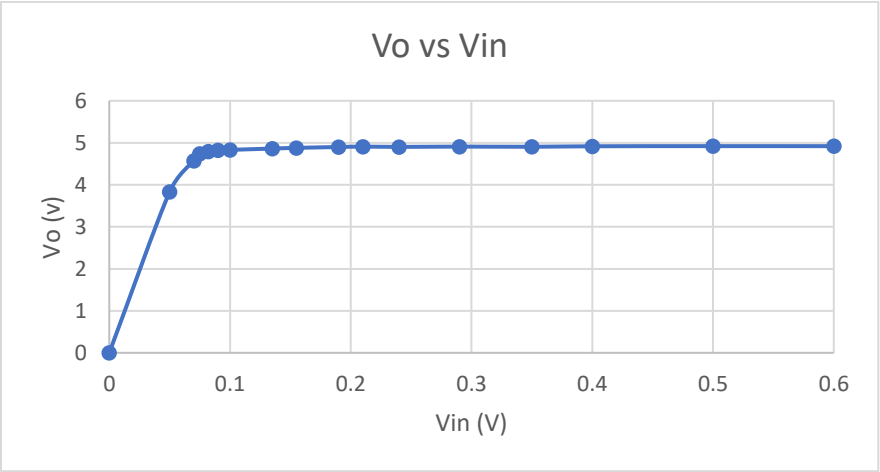

Figure 3. Voltage transfer curve for part 1C.

1D.

The calculated and measured input and output impedances are seen in table 3. We see that the values of the impedances are not far off.

	R_{in}	R_{out}
Measured	3.659kΩ	2.527kΩ
Calculated	3.510kΩ	2.4kΩ

Table 3. Measured and calculated impedances for part 1D.

In this part, we biassed a cascode amplifier using the 1/4 rule using β to be 300 as in [4] and within the range in [1]. We compare this calculation to the simulated circuit of figure 1 and adjusted the impedances through addition of a resistor in series to the base capacitor to attain the desired input impedance.

Part 2

2A.

Through simplifications in equation 25, we get an approximation of the formula for R_i. And using equations of the second 1/3 rule seen in [3] and [4], we get the values in table 4.

$$R_i = \frac{r_\pi}{1+\beta} || R_{E1} = \frac{\beta}{1+\beta}\frac{V_T}{I_{C1}} || \frac{V_{E1}}{I_{E1}} = \frac{V_T}{I_{E1}} || \frac{V_{E1}}{I_{E1}} \approx \frac{V_T}{I_{E1}} = 50\Omega \quad (25)$$

To calculate for the values of R_{E2} and R_{C1}, we use equation 26, with further substitutions of values coming from equations 27 to 29.

$$R_{out} = 50\Omega = \frac{R_{C1} + r_{\pi 2}}{1+\beta} || R_{E2} \quad (26)$$

$$r_{\pi 2} = \frac{\beta \times V_T}{I_{C2}} \quad (27)$$

$$R_{C1} = \frac{V_{CC} - V_{C1}}{I_{C1} + I_{B2}} \quad (28)$$

$$I_{B2} = \frac{V_{E2}}{R_{E2}} \quad (29)$$

We use the low-frequency small signal model in figure 4 to determine the capacitances. Using the open and short circuit tests, we get equations 30 and 31.

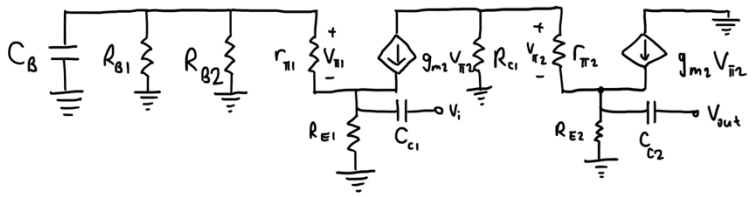

Figure 4. The low-frequency small signal model of the cascading amplifier

I_{B1}	I_{E1}	I_{C1}	R_{B1}	R_{B2}	R_{E1}	R_{E2}	R_{C1}
4.950μA	0.5mA	0.495mA	187kΩ	125kΩ	10kΩ	281Ω	6.066kΩ

Table 4. Current and resistance values for the cascaded amplifier.

$$\tau_{C_{C2}} = C_{C2} \times \left(\frac{R_{C1} + r_{\pi 2}}{1+\beta} \;||\; R_{E2}\right) = C_{C2} \times 50\Omega \quad (30)$$

$$\tau_{C_{C1}} = C_{C1} \times \left(\frac{r_{\pi 1}}{1+\beta} \;||\; R_{E1}\right) = C_{C1} \times 49.75\Omega \approx C_{C1} \times 50\Omega \quad (31)$$

From equations 30 and 31, we treat C_{C1} and C_{C2} as the same. Equating this to the low-frequency cut-in at 1000Hz, we get equation 32, where C represents the values of C_{C1} and C_{C2}. To find C_B, we set the pole associated with C_B, originally at the location computed in equation 33, to be at least one decade below for a more accurate assumption, which is 444 rad/s. By solving equation 34, we get the maximum value of C_B at 32.221nF.

$$1000Hz \times 2\pi = \sqrt{2 \times \left(\frac{1}{C \times 50\Omega}\right)} \rightarrow C = 4.50\mu F = C_{C1} = C_{C2} \quad (32)$$

$$Pole\ for\ capacitor\ at\ \frac{1}{C \times 50\Omega} = 4.44\ rad/s \quad (33)$$

$$\omega_{C_B} = 444\frac{rad}{s} = [C_B \times (R_{B1} \;||\; R_{B2} \;||\; (r_\pi + (1+\beta) \times R_{E1}))]^{-1} \quad (34)$$

2B.

The standard resistor and capacitor values used for the circuit in figure 5 are provided in table 5.

C_{C1}	C_{C2}	C_B	R_{B1}	R_{B2}	R_{E1}	R_{E2}	R_{C1}
4.7µF	4.7µF	0.027µF	180kΩ	130kΩ	10kΩ	270Ω	6.2kΩ

Table 5. Standard resistor and capacitor values used for the circuit in figure 5.

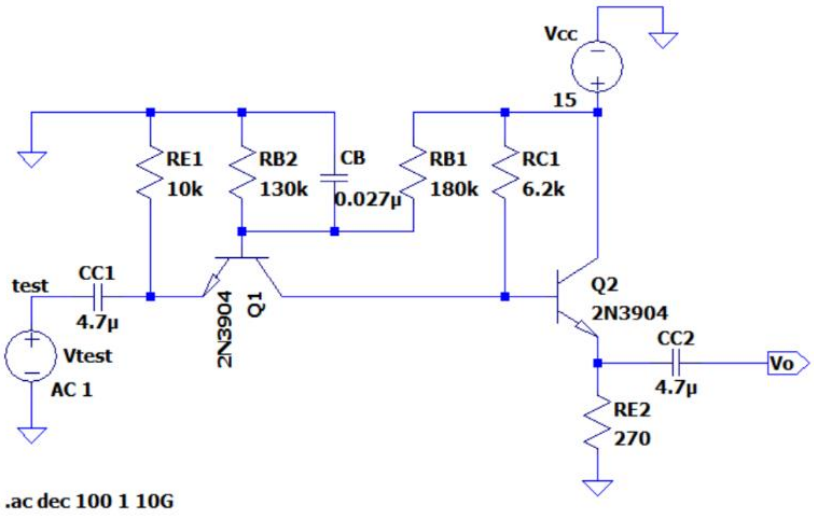

Figure 5. The simulated circuit for obtaining the midband.

From the Bode plot of the circuit in figure 5, we get the low frequency to be 1.4100kHz and the high frequency to be 4.2693MHz. We choose the geometric mean, 77.5868kHz, to be the midband frequency. Plotting V_{Test}/I_{Test}, we find the R_{in} value to be 56.5274Ω. Using a similar method, we find R_{out} to be 52.8639Ω. The R_{in} value does not satisfy our requirement for the input impedance, so we adjust R_{E1} to be 7.5kΩ. After this adjustment, we get R_{in} to be 53.9461Ω and R_{out} to be 51.2840Ω. Both impedances satisfy our requirements.

We use transient analysis to get the gain of the output signal, A_m, to be 118.2 V/V.

2C.

We simulate the circuit in figure 6. From figure 7, we find that the low-frequency cut-in is 936.911Hz and the high-frequency cut-off is 2.550MHz. As the cut-in frequency satisfies our specification that the low-frequency cut-in should be at or below 1000Hz, no readjustments need to be made.

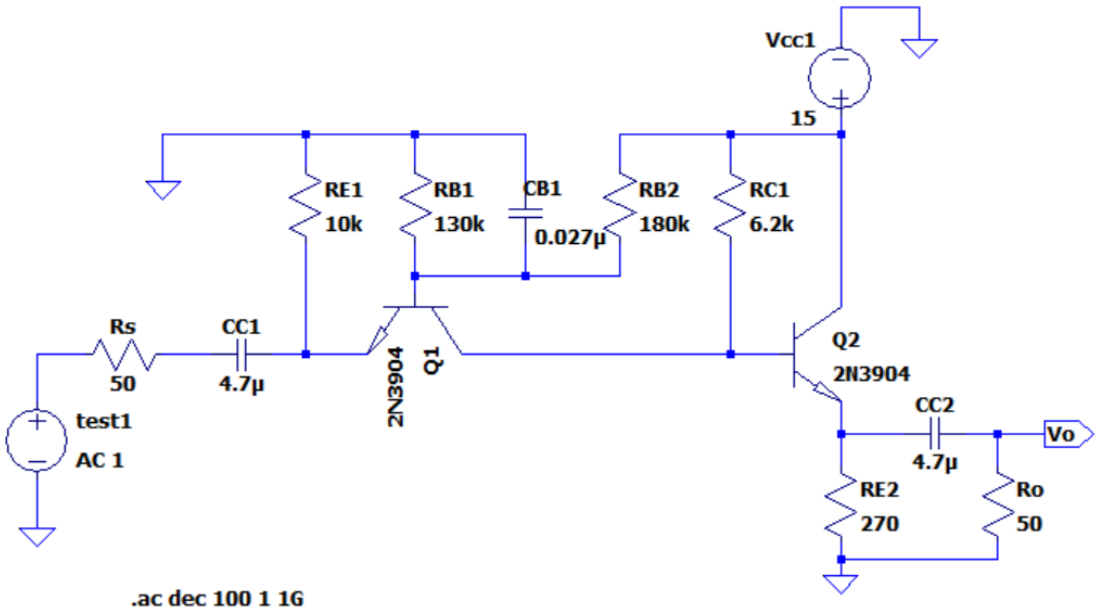

Figure 6. The simulated circuit for part 2c.

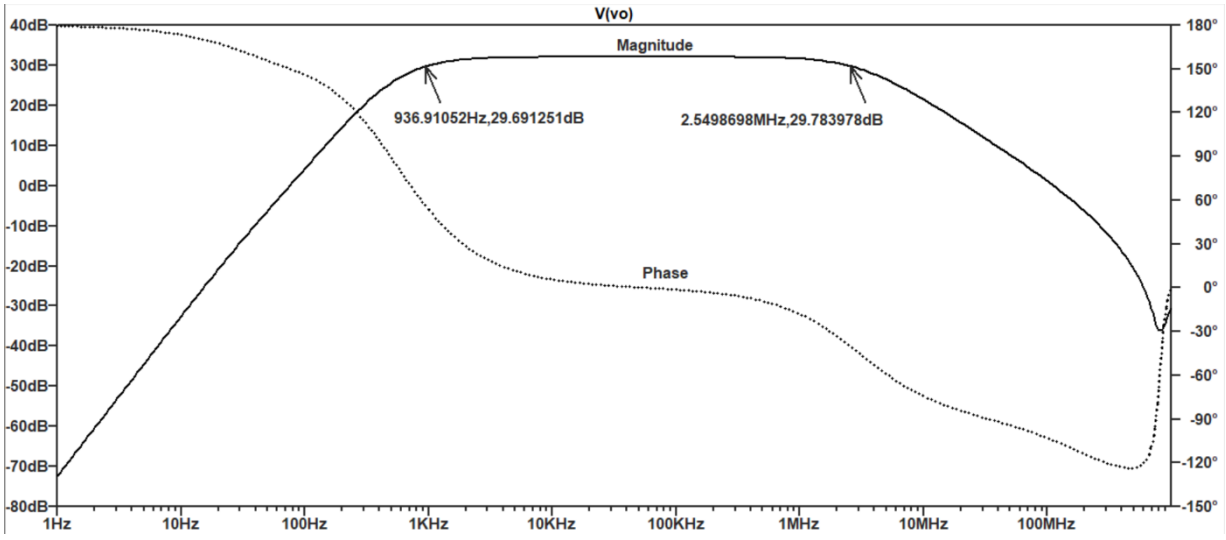

Figure 7. The Bode plot for the circuit in figure 6.

This part of the mini project shows that we can design and readjust components in a cascaded amplifier to get specifications that we need and ensure that we can get the performance that we look for in these amplifiers.

Part 3

3A.

The differential amplifier pair for this part of the mini project is seen in figure 8, and the Bode plot can be found in figure 9. To get the gain of the circuit, we use equation 35, with the voltages being the peak-to-peak values obtained as seen in figure 10.

$$A_D = \frac{V_o}{V_i} = \frac{10.969V}{399.769\mu V} = 27438\ V/V \tag{35}$$

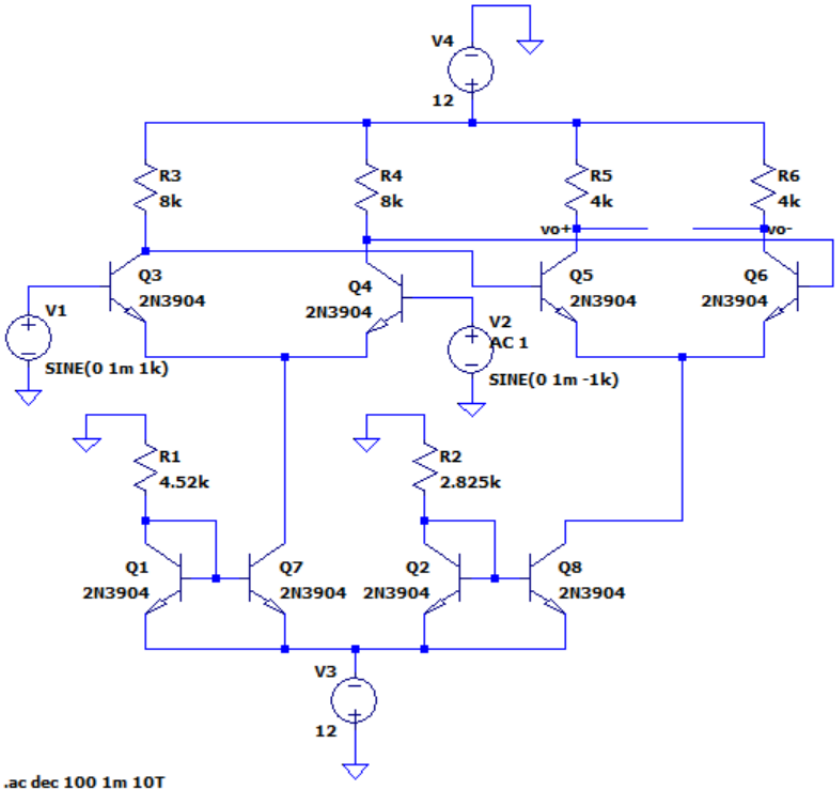

Figure 8. Simulated circuit for part 3A.

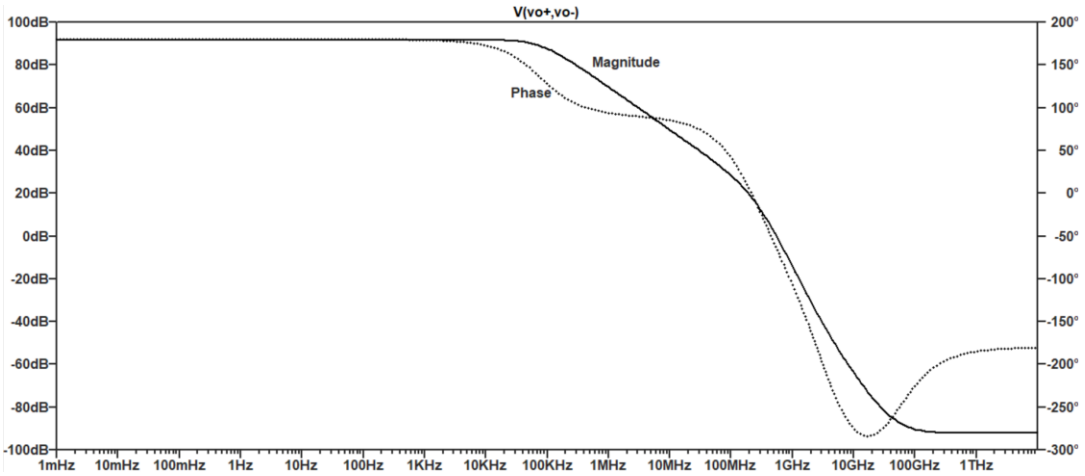

Figure 9. Bode plot of the circuit in figure 8.

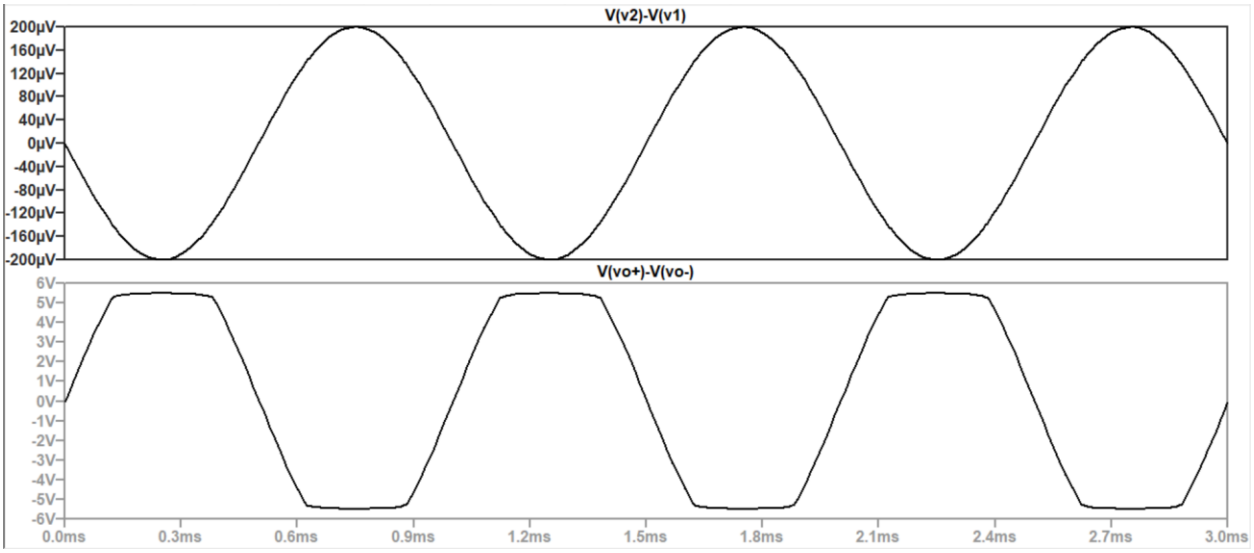

Figure 10. The input and output voltage waveforms for part 3C.

3B.

To get the differential input impedance, we set the amplitude of the sinusoidal sources to be 0.1mV. We take the peak to peak voltage value and the current peak to peak test value, 16.657µA, to get the impedance R_{in} = 24.013kΩ.

For the output impedance, we short the input terminals and apply a test voltage source to our output. We plot the peak-to-peak voltage against the current to get the output impedance R_o to be 103.283Ω.

3C.

The Bode plot for this part is found in figure 11. Using a similar methodology as in part 3A, but using figure 12, we get the gain A_{cm} in equation 25. The common mode rejection ratio (CMRR) is calculated in equation 36, using the A_D value obtained in part 3A.

$$A_{CM} = \frac{39.420\mu V}{188.864\mu V} = 0.2087216 \tag{35}$$

$$CMRR = 20\log\left(\frac{A_D}{A_{CM}}\right) = 102.376dB \tag{36}$$

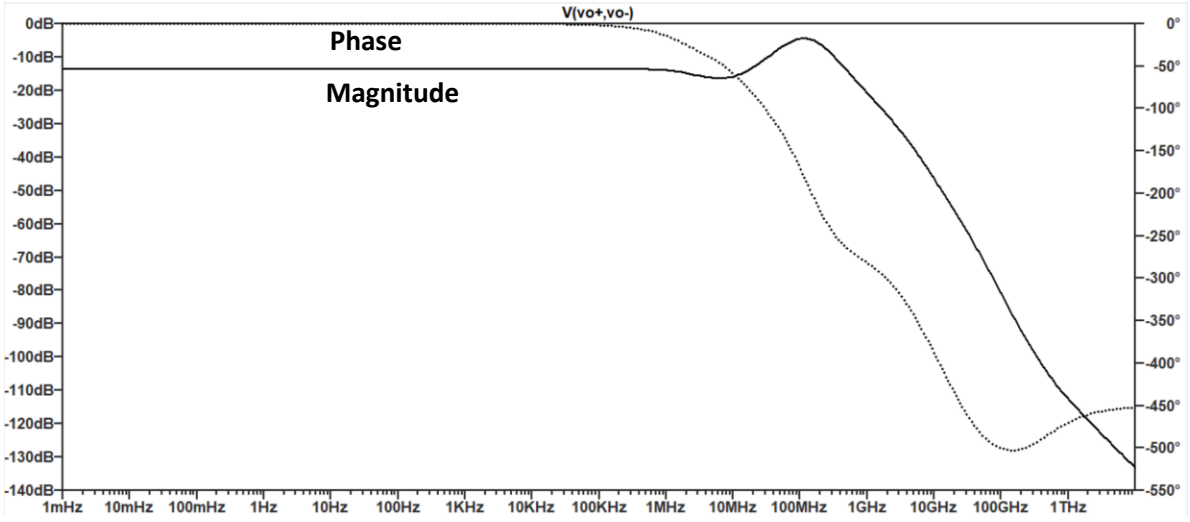

Figure 11. The Bode plot for part 3C.

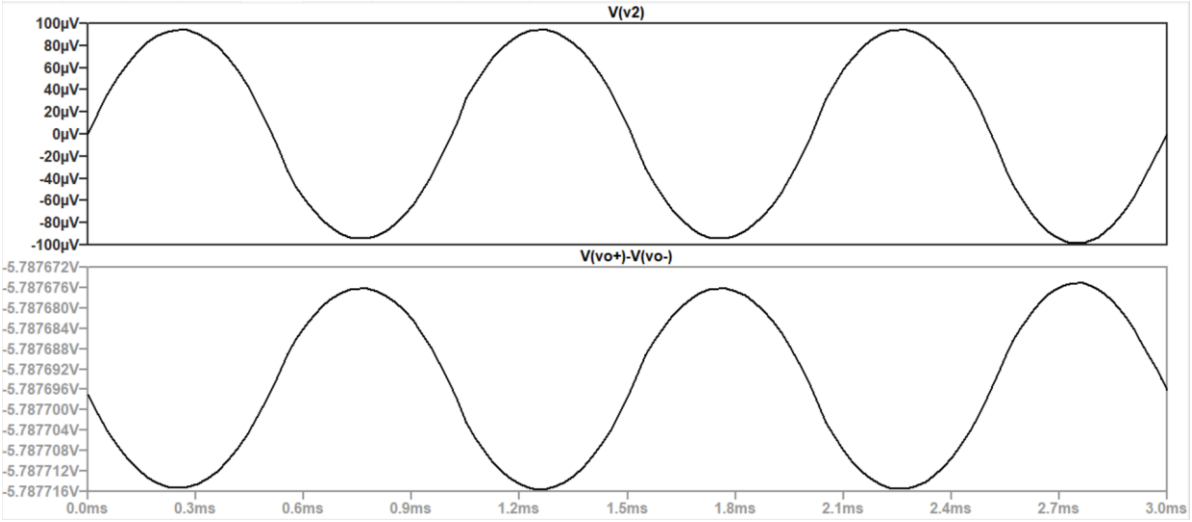

Figure 12. The input and output voltage waveforms for part 3C.

3D.

The CMRR of the circuit in figure 1 of [5] was calculated to be 122dB. This is higher, and more desirable due to a higher rejection of common mode signals, than the circuit that we have in part 3C, which was partly expected given that the calculated values are closer to the 'ideal' values. The main difference between the two circuits are that β is 100 in [5] while β is measured to be 300 from [3].

3E.

Using equation 35, but with the peak-to-peak amplitude of the input voltage to be 188.997μV and the output voltage to be 39.447μV as seen in figure 13, we get A_{CM} to be 0.2087176.

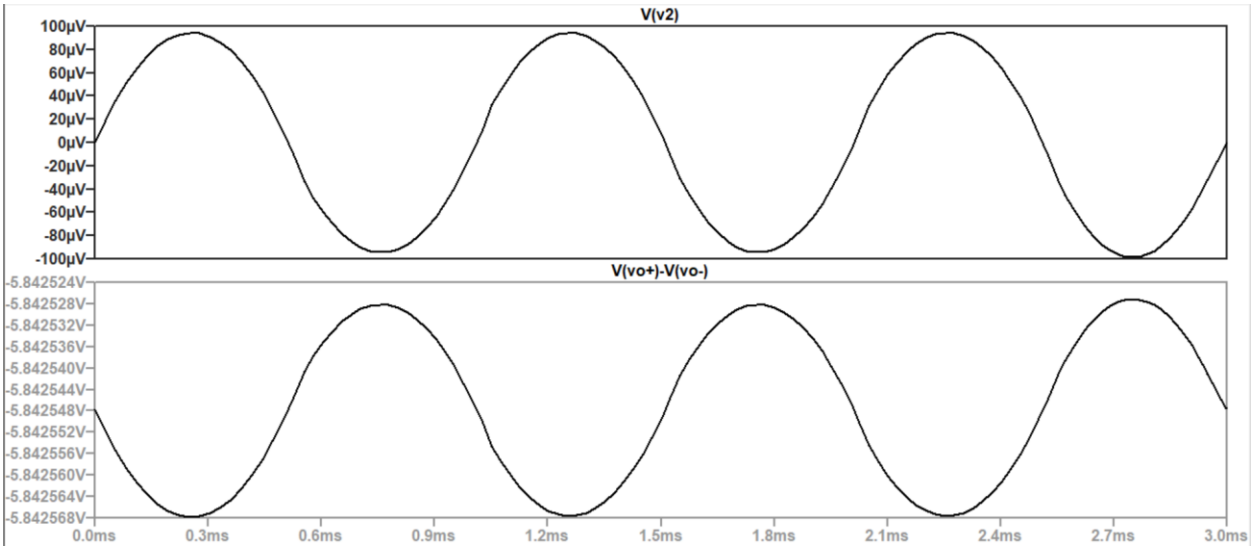

Figure 13. The input and output voltage waveforms for part 3E.

3F.

The CMRR for parts 3C and 3F are almost similar, indicating that modifying the impedances of the 4kΩ collector resistors by 0.1% does not change the CMRR significantly.

Part 4

4A.

The modulator circuit that was simulated can be seen in figure 14.

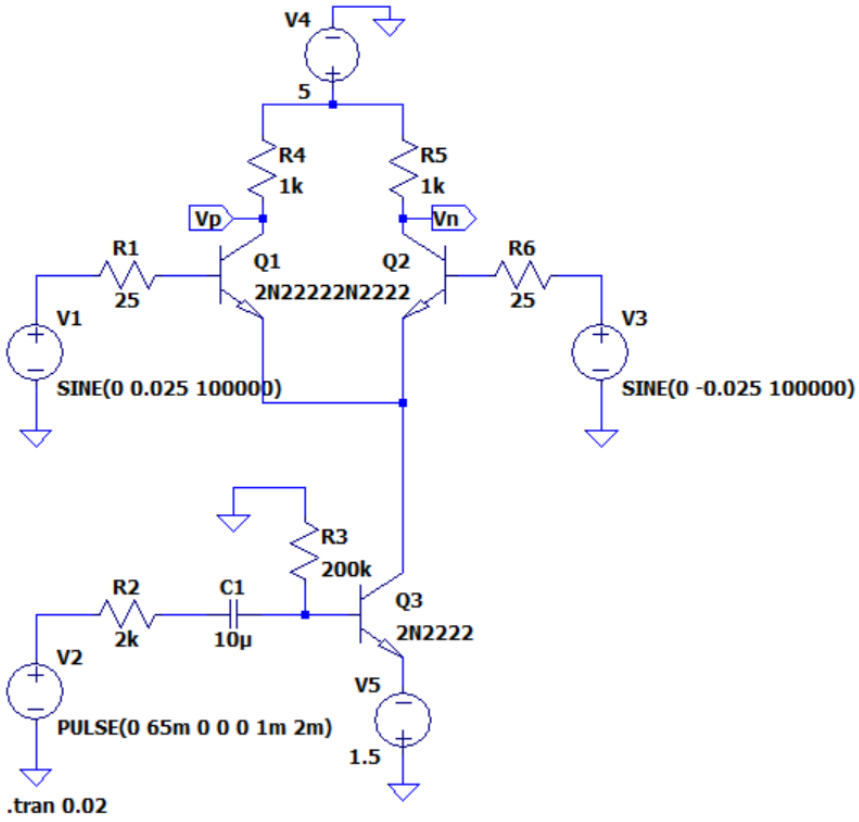

Figure 14. The modulator circuit for part 4.

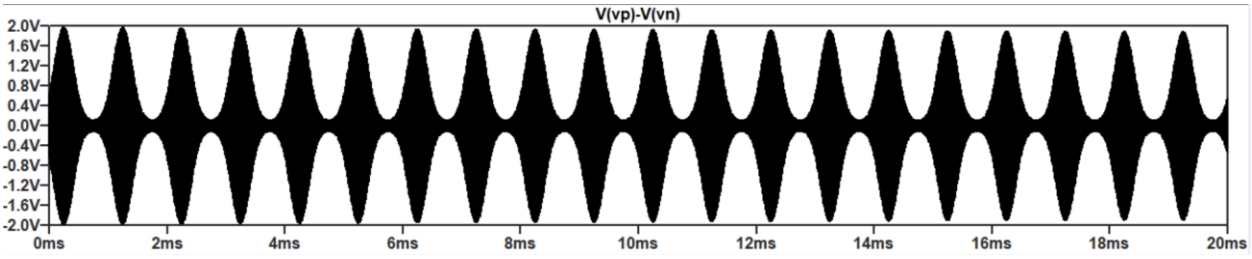

Figure 15. The output signal with 50mV V_P input.

4B.

Applying varying V_P values from 10mV to 90mV, we note that the output amplitude also increases as the input amplitude increases. Distortion becomes perceptible when the amplitude goes beyond $40mV_p$. As the input amplitude goes higher, more distortion will be perceptible. The input signal with the least distorted envelop is expected to be close to $40mV_p$. Various V_P values were simulated, with the results seen from figures 16 to 19.

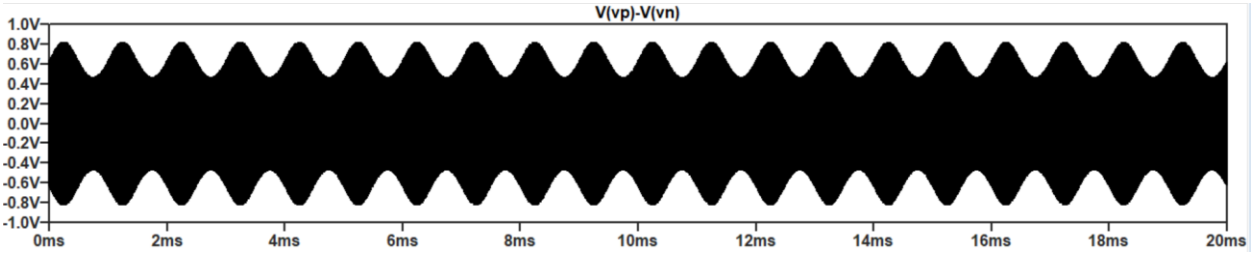

Figure 16. The output signal with 10mV V_P input.

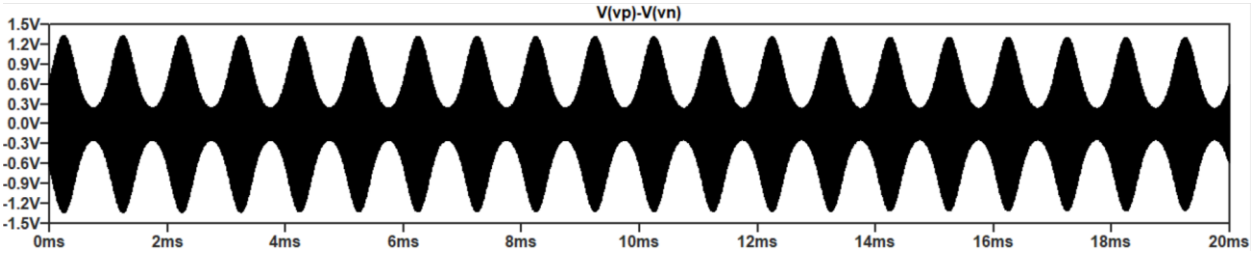

Figure 17. The output signal with 30mV V_P input.

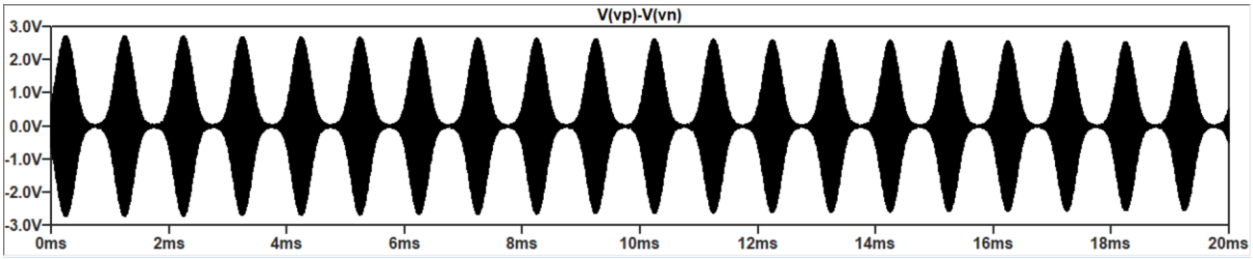

Figure 18. The output signal with 70mV V_P input.

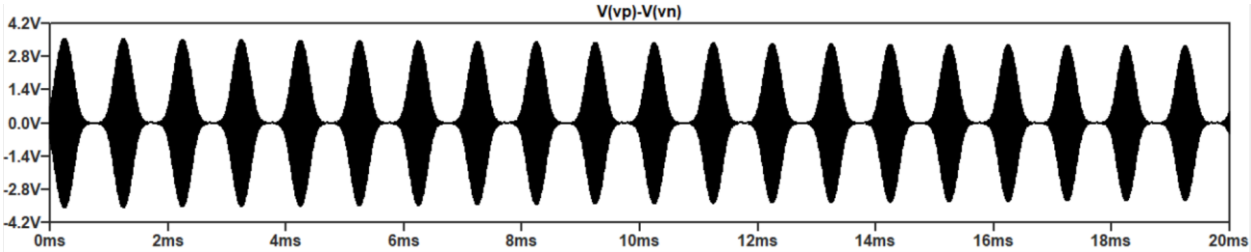

Figure 19. The output signal with 90mV V_P input.

4C.

For this part, a square wave input was used instead of sinusoidal waves. Despite this, the observations of this part remain the same as in part 4B. An example of the output signal can be seen in figure 20.

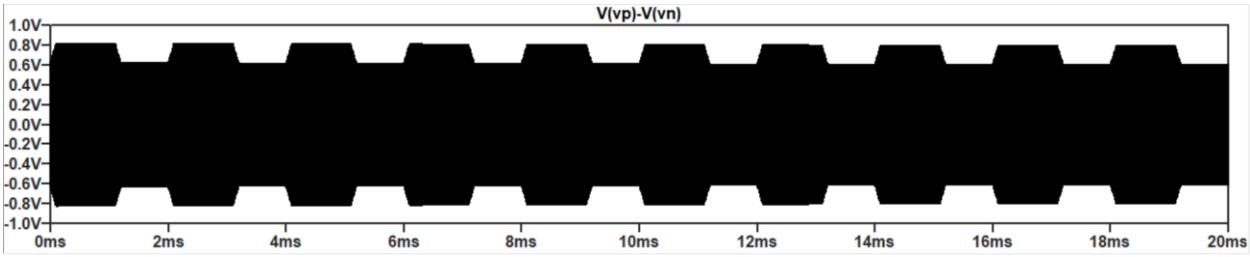

Figure 20. The output signal with 10mV V_P input, square wave.

An AM modulator works by combines the high-frequency carrier signal to the low-frequency input signal. This input signal is fed into a component, typically a transistor, which then acts as a constant current source when properly biassed. In figure 14, transistors Q1 and Q2 receives the carrier signals concurrently at a 180^o phase difference. Due to the nature of sinusoidal waves, the output voltage will vary, and the varying current will modulate the carrier signals to convolute them to produce output signals that vary in amplitude reflective of the modulating input. As such, the AM wave will carry the frequencies of both carrier and input signals.

3. Conclusion

In this mini project, we explored biassing cascoded, cascaded, and differential amplifiers. We learned about applying the ¼ rule to the cascoded amplifier and adjusting the values of the components to match specifications. For cascaded amplifiers, we learnedd about their application as signal repeaters. We also learned about finding the CMRR of an amplifier and compare it with other CMRR values. Lastly, we learned about making a modulator and how it works.

4. References

[1] Onsemi 2N3903, 2N3904 Transistors Data Sheet

[2] ELEC 301 Standard Resistor and Capacitor Values Sheet

[3] ELEC 301 Mini Project 2

[4] ELEC 301 Course Notes

[5] ELEC 301 Problem Set 6

[6] LTSpice™ User Manual

[7] A. Sedra and K. Smith, "Microelectronic Circuits," 5th (or higher) Ed., Oxford University Press, New York.