14 to 18 marks

1/8/23

2] Logic Gate and Logic ~~Fam~~ Familys.

- Logic Gate :- It is an electronic circuit having one or more than 1 input and only one output.
- The relationship between input and output is based on ceirtain logic

- Truth table :- It is the table used to understand the operation of logic gate.
- Truth table consist of all posible combination of inputs and corresponding steps of output of logic gate

- boolean Expression :- The relation between input and output of gate can be expressed mathematically by using bolleon Expression

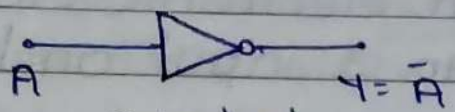
- Types of logic Gate :- (classification)

- Logic gate are classified into three types

A] Basic Gate
  i] NOT Gate
  ii] OR Gate
  iii] AND Gate
B] universal Gate
  i] NOR Gate
  ii] NAND Gate
c] special purpose Gate.
  i] EX-OR gate
  ii] EX-NOR gate

∴ (Ex = Explosive)

a] 1] NOT gate or (Inverter):-



Symbol

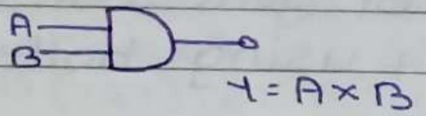
· Truth table.

Input A	output $Y = \bar{A}$
0	1
1	0

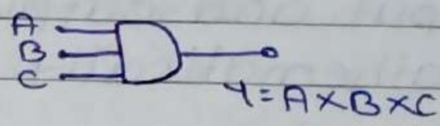
$\bar{0} = 1$
$\bar{1} = 0$

2/8/23

2] AND gate



2-input AND-Gate Symbol



3-input AND-Gate Symbol

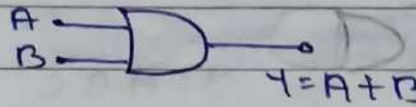
Truth table

input		output
A	B	Y = A×B
0	0	0
0	1	0
1	0	0
1	1	1

Truth table.

Input			output
A	B	C	Y = A×B×C
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

3] OR gate



Truth table

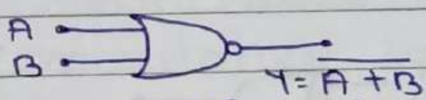
Input		output
A	B	$Y = A + B$
0	0	0
0	1	1
1	0	1
1	1	1

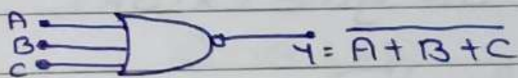
Truth table

input			output
A	B	C	$Y = A + B + C$
0	0	0	0
0	0	1	1
0	1	0	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

B]

14] NOR gate





2-input NOR gate symbol

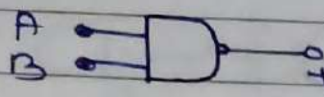
TT

Input		output
A	B	$Y = \overline{A + B}$
0	0	1
0	1	0
1	0	0
1	1	0

TT

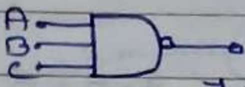
Input			output
A	B	C	$Y = \overline{A + B + C}$
0	0	0	1
0	0	1	0
0	1	0	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

2] NAND gate :-



$Y = \overline{A.B}$

2 input gate



$Y = \overline{A.B.C}$

3-input gate

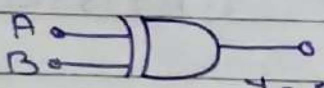
TT

input		output	
A	B	$Y = \overline{A.B}$	output
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

TT

input			output	
A	B	C	$Y = \overline{A.B.C}$	output
0	0	0	0	1
0	0	1	0	1
0	1	0	0	1
0	1	1	0	1
1	0	0	0	1
1	0	1	0	1
1	1	0	0	1
1	1	1	1	0

c] i] EX-OR gate (X-OR)



$Y = A \oplus B$

$= A.\overline{B} + \overline{A}.B$

2 input X-OR gate

$Y = A \oplus B \oplus C$

$= A.\overline{B}.\overline{C} + \overline{A}.B.\overline{C} + A.B.C$

3 input X-OR gate.

TT

input		output
A	B	$Y = A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

TT

input			output
A	B	C	$Y = A \oplus B \oplus C$
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

ii] Ex-NOR gate (X-NOR)

 $Y = \overline{A \oplus B}$  $Y = \overline{A \oplus B \oplus C}$

$= A\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}\bar{B}C + ABC$

TT

Input		output	
A	B	$A \oplus B$	$Y = \overline{A \oplus B}$
0	0	0	1
0	1	1	0
1	0	1	0
1	1	0	1

TT

input				output
A	B	C	$A \oplus B \oplus C$	$Y = \overline{A \oplus B \oplus C}$
0	0	0	0	1
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	0

* boolean laws :-

1] Commutative law

$A.B = B.A$

$A+B = B+A$

2] Associated law

$(A.B).C = A.(B.C)$

$(A+B)+C = A+(B+C)$

3] Distributive law

$A(B+C) = AB + AC$

4] AND Law

$A \times 0 = 0$

$A \times 1 = A$

$A \times A = A$

$A \times \bar{A} = 0$

5] OR-Law

$A + 0 = A$

$A + 1 = 1$

$A + A = A$

$A + \bar{A} = 1$

6] Inversion law

$\bar{\bar{A}} = A$

$\bar{\bar{B}} = B$

ex:- $\bar{\bar{0}} = \bar{1} = 0$

3|8|23

* De-Morgan's Theorem:-

1] Theorem-I :- Complement of ~~theorem~~ Product is equal to addition of complement

$$\overline{A \cdot B} = \bar{A} + \bar{B}$$

					L.H.S	R.H.S
A	B	$\bar{A}$	$\bar{B}$	AB	$\overline{A \cdot B}$	$\bar{A}+\bar{B}$
0	0	1	1	0	1	1
0	1	1	0	0	1	1
1	0	0	1	0	1	1
1	1	0	0	1	0	0

$\therefore \overline{A \cdot B} = \bar{A} + \bar{B}$

2] Theorem-II :- Complement of sum is equal to product of complement

$$\overline{A+B} = \bar{A} \times \bar{B}$$

A	B	$\bar{A}$	$\bar{B}$	$A+B$	$\overline{A+B}$	$\bar{A} \times \bar{B}$
0	0	1	1	0	1	1
0	1	1	0	1	0	0
1	0	0	1	1	0	0
1	1	0	0	1	0	0

* Principle of Duality:-

it's states that in two value boolean Algebra the Dual of an algebric expression can be obtain by interchanging ~~or~~ OR and AND operator and by replasing 1 by 0 and 0 by 1

According to principle of duality the following conversion are posible in given boolean expression.

1) change each AND operation to OR operation
2) change each OR operation to AND operation
3] complement any 1 OR 0 appear in the expression.

- duality theorem is useful in creating new expression from given boolean Expression

1) $A+\bar{A}.B = A$

→ L.H.S $A + A.B$

$A(1+B)$

$= A * 1 \quad \therefore \{1+B=1$

$= A$

$=$ R.H.S

2] $(A+B)(A+C) = A+BC$

→ LHS: $(A+B)(A+C)$

$= A.A + A.C + B.A + B.C$

$= \boxed{A + A.C} + BA + BC \quad \{A.A = A$

$= A + AB + BC \quad \therefore \{A + AC = A$

$= A + BC \quad \{A + AB = A$

$=$ R.H.S

3] $\bar{A} + AB = \bar{A} + B$

→ LHS $= \bar{A} + AB$

$= \boxed{\bar{A} \times 1} + AB$

$= \bar{A}(1+B) + AB \quad \{1 + B = 1$

$= \bar{A} + \bar{A}B + AB$

$= \bar{A} + B(\bar{A} + A)$

$= \bar{A} + B(1) \quad \therefore \{\bar{A} + A = 1$

$= \bar{A} + B$

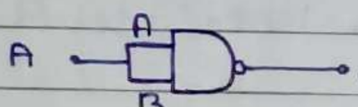
$=$ R.H.S

4/8/23

* Universal gate :- NAND gate and NOR gate are called universal gate because it is posible to implement any boolean expression by using only NAND gate and only NOR gate hence user can build any combination circuit by using only NAND gate or only NOR gate. hence it is not necessary or user to make stop of other gates than NAND gate or NOR gate

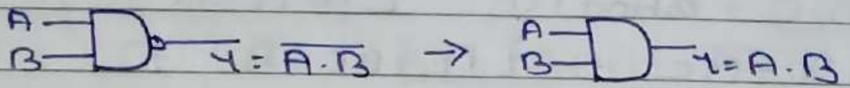
- NAND gate as universal gate:-

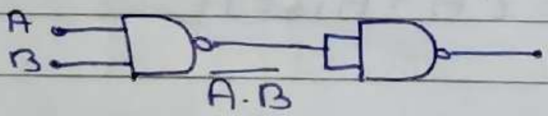
1) NOT gate using NAND gate



$$Y = \overline{A.B}$$
$$= \overline{A.A}$$
$$= \overline{A} \quad .. \{ A.A = A$$

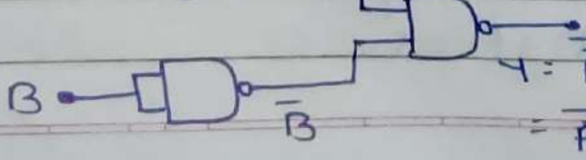
2] AND gate using NAND gate





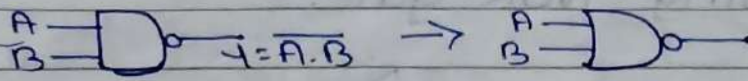
$$Y = \overline{\overline{A.B}}$$
$$Y = A.B$$

3] OR gate using NAND gate

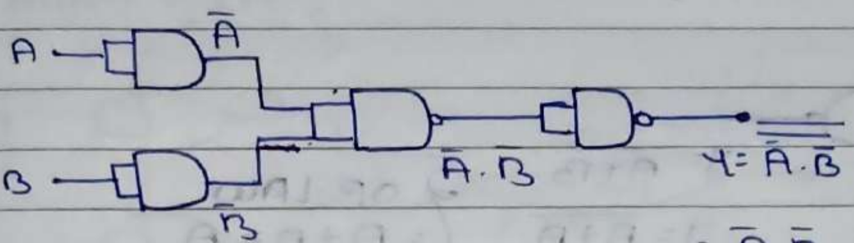


$$Y = \overline{\overline{A} \times \overline{B}}$$ By D'Morgon's theorem
$$= \overline{\overline{A+B}} \quad .. \{ \overline{A} \times \overline{B} = \overline{A+B}$$
$$= A+B$$

4] NOR gate using NAND gate



$Y=\overline{A\cdot B} \rightarrow Y=\overline{A+B}$

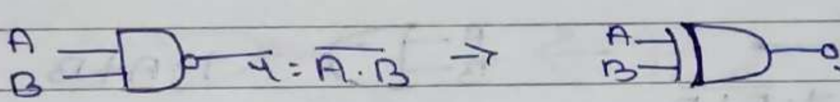


$Y=\overline{\overline{\bar{A}\cdot\bar{B}}}$

$=\bar{A}\cdot\bar{B}$

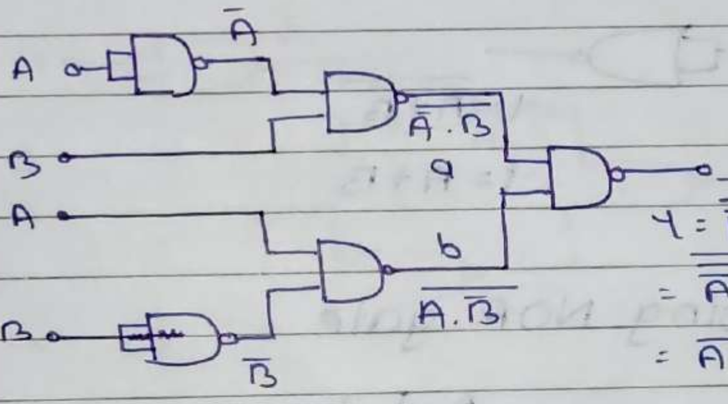
$=\overline{A+B}$

5] Ex-OR-gate using NAND gate.



$Y=\overline{A\cdot B} \rightarrow Y=A\oplus B$

$=\bar{A}B+A\bar{B}$

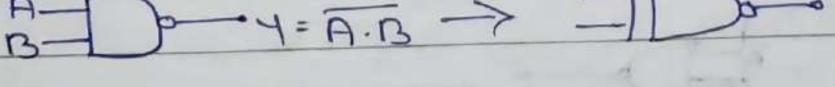


$Y=\overline{\overline{\bar{A}\cdot B}\times\overline{A\cdot\bar{B}}}$

$=\overline{\overline{\bar{A}\cdot B}}+\overline{\overline{A\cdot\bar{B}}}$

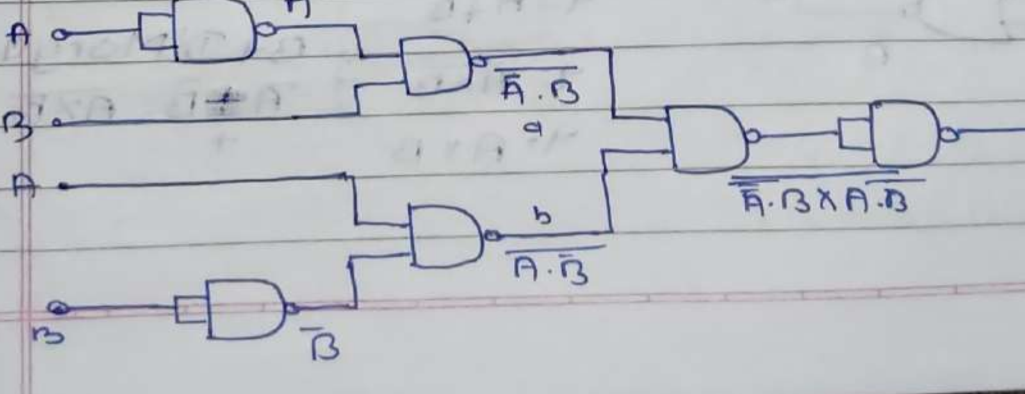
$=\bar{A}\cdot B+A\cdot\bar{B}$ ... {By d Morgan's theorem

6] Ex.NOR gate using NAND gate



$Y=\overline{A\cdot B} \rightarrow Y=\overline{A\oplus B}$

$=\overline{\bar{A}B+A\bar{B}}$



$Y=\overline{\overline{\overline{\bar{A}\cdot B}\times\overline{A\cdot\bar{B}}}}$

$=\overline{\overline{\bar{A}\cdot B}\times\overline{A\cdot\bar{B}}}$

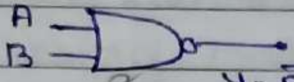
$=\overline{\bar{A}\cdot B+A\cdot\bar{B}}$

$=\overline{A\oplus B}$

5/8/23

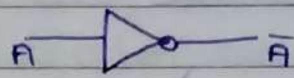
* NOR gate as universal gate

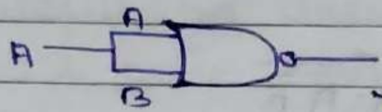
1) NOT gate using NOR gate.



$Y = \overline{A+B}$

$\rightarrow$



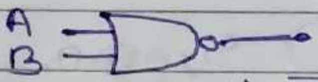


$Y = \overline{A+B}$

$Y = \overline{A+A}$ $\left\{ \begin{array}{l} \text{OR-LAW} \\ = A+A = A \end{array} \right.$

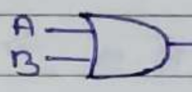
$Y = \overline{A}$

2] OR gate using NOR gate

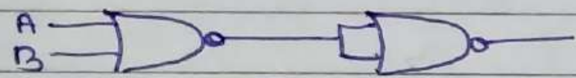


$Y = \overline{A+B}$

$\rightarrow$



$Y = A+B$



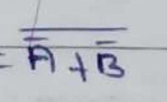
$\overline{A+B}$

$Y = \overline{\overline{A+B}}$

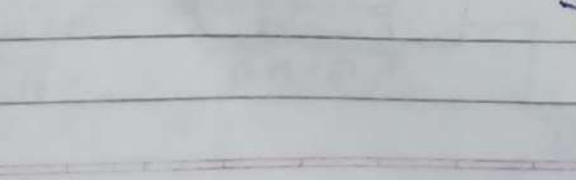
$Y = A+B$

3] AND gate using NOR gate

$Y = \overline{A+B}$



$Y = A.B$

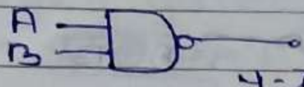


$Y = \overline{\overline{A}+\overline{B}}$

$Y = \overline{\overline{A \times B}}$ $\left\{ \begin{array}{l} \text{By D'Morgan's} \\ \overline{A} \underset{+}{} \overline{B} = \overline{A \times B} \end{array} \right.$

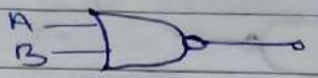
$Y = A \times B$

4] NAND using NOR gate.



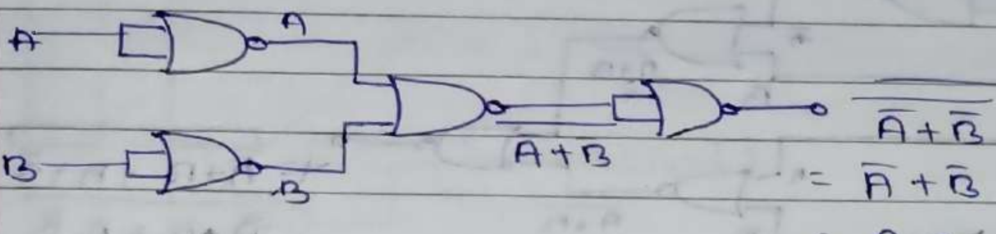
$Y = \cancel{\overline{A+B}}\ \overline{A.B}$

NAND gate



$Y = \overline{A+B}$

NOR gate

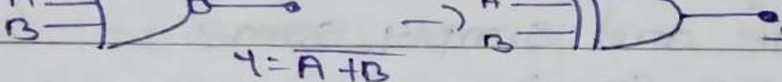


$\overline{\bar{A}+\bar{B}}$

$= \overline{\bar{A}+\bar{B}}$

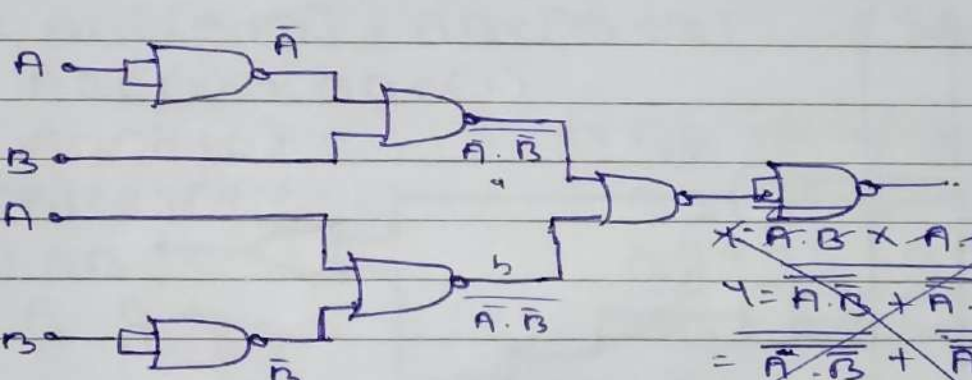
$= A.B$

5] Ex-OR gate using NOR. gate



$Y = \overline{A+B}$ → $Y = A \oplus B$

$= A\bar{B} + \bar{A}.B$



$\cancel{\overline{A.B} \times \overline{A.B}}$

$\cancel{Y = \overline{\overline{A.\bar{B}} + \overline{\bar{A}.B}}}$

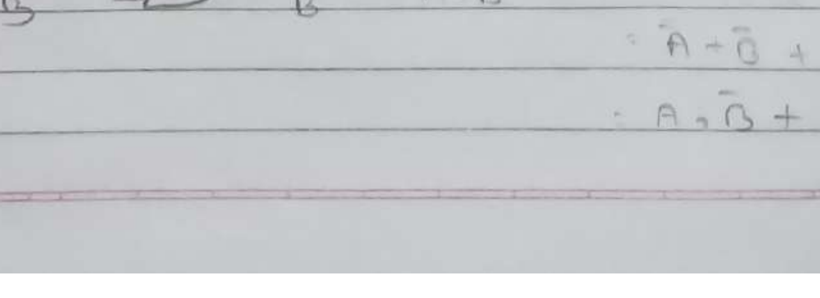
$\cancel{= \overline{\bar{\bar{A}}.\bar{B}} + \overline{\bar{A}.\bar{\bar{B}}}}$

$\cancel{= A.\bar{B} + \bar{A}.B}$ { By demorgan's theorem

$= Y = \overline{\overline{\bar{A}+B} + \overline{A+\bar{B}}}$

$= \bar{\bar{A}}+\bar{B} + \bar{A}+\bar{\bar{B}}$

$= A * \bar{B} + \bar{A} * B$

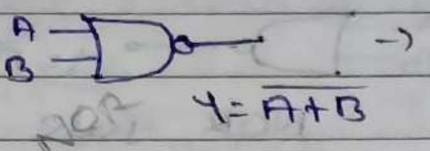


$Y = \overline{\overline{\bar{A}+B} + \overline{A+\bar{B}}}$

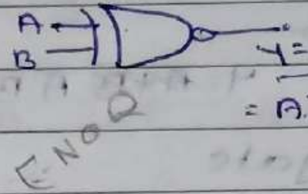
$= \bar{A}+\bar{B} + A+\bar{B}$

$= A.\bar{B} + \bar{A}.B$

Ex-NOR gate using NOR gate.

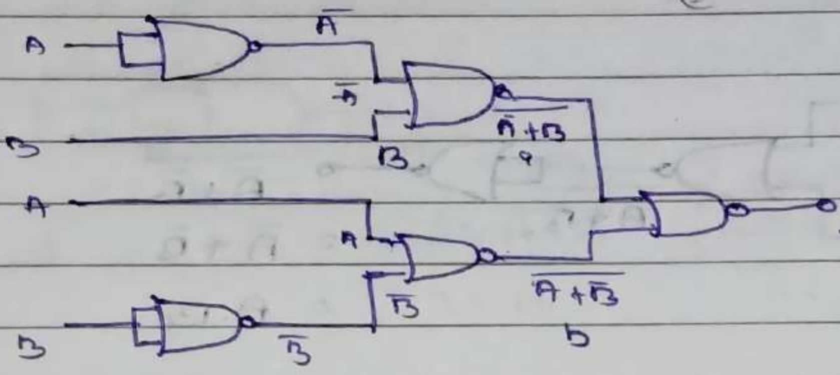


$Y = \overline{A+B}$ →



$Y = \overline{A \oplus B}$

$= \overline{A\cdot\bar{B} + \bar{A}\cdot B}$



$Y = \overline{\overline{\bar{A}+B} + \overline{A+\bar{B}}}$

$= \overline{\bar{\bar{A}} \cdot \bar{B} + \bar{A}\cdot\bar{\bar{B}}}$

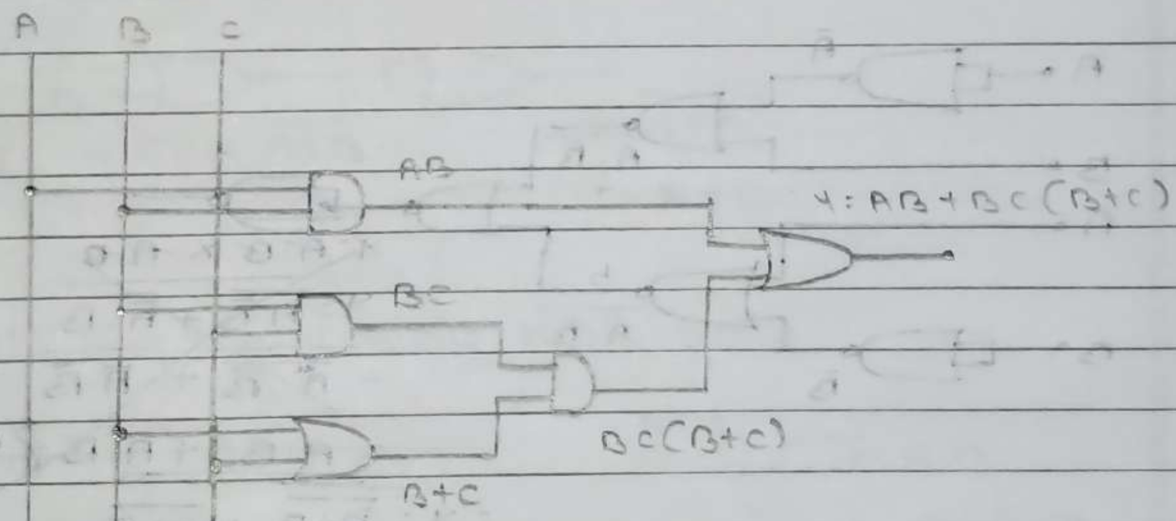
$= \overline{A\cdot\bar{B} + \bar{A}\cdot B}$

6/8/23

* Realize the given boolean Expression using basic gate and simply same

S-22 4 marks

- $Y = AB + BC(B+C)$



$Y = AB + BC(B+C)$

$= AB + BC\cdot B + BC\cdot C$ ... $\left\{ \begin{array}{l} B\cdot B = B \\ C\cdot C = C \end{array} \right.$

$= AB + BC + BC$ ... $\{ BC + BC = BC$

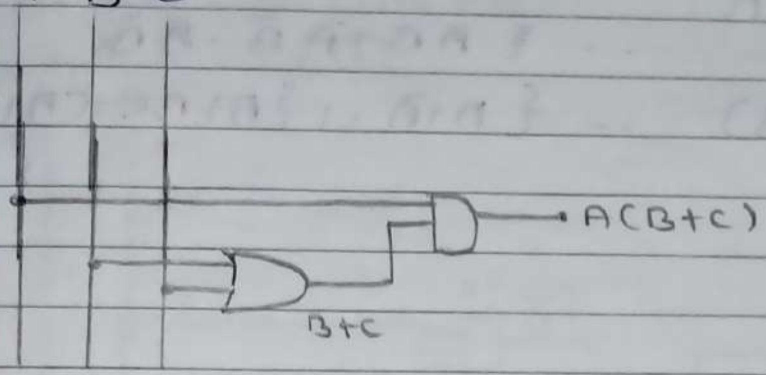
$= AB + BC$

$= B(A+C)$

2] Sketch the given boolean expresion using one AND gate and one OR gate only.

- $Y = AB + AC$

$= A(B+C)$



3] Smiply the Following boolean Expresion and implement using logic gate. W-19

$Y = AB\bar{C}\bar{D} + AB\bar{C}D + ABC\bar{D} + ABCD$

$= AB\bar{C}[\bar{D}+D] + ABC[\bar{D}+D] \quad \ldots \{\bar{D}+D = 1$

$= AB\bar{C}(1) + ABC(1)$

$= AB(\bar{C}+C)$

$= AB \times 1$

$Y = AB$

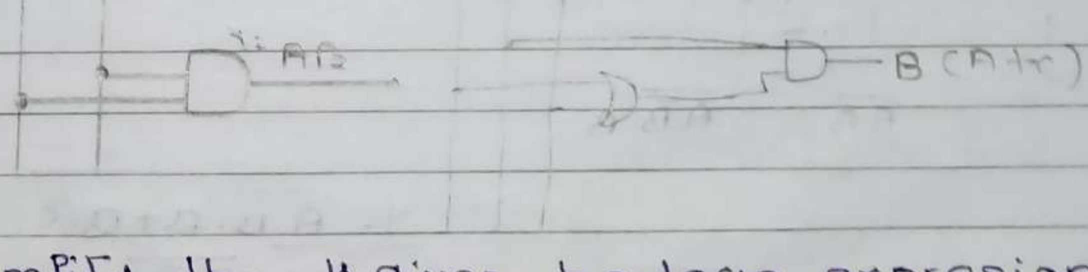
$Y = AB + BC(B+C)$

$AB + BC.B + BC.C$

$AB + BC + BC$

$AB + BC$

$B(A+C)$



4] Simpify the given boolean expresion and realize it.

- $Y = A + B\bar{A}\bar{B}C + \bar{A}.\bar{B}.\bar{C} + ABC + \bar{A}\bar{B}$

$Y = A + \bar{A}\bar{B}C + \bar{A}.\bar{B}.\bar{C} + ABC + \bar{A}\bar{B}$

$A + ABC + \bar{A}\bar{B}C + \bar{A}.\bar{B}.\bar{C} + \bar{A}.\bar{B}$

$= A(1+BC) + \bar{A}.\bar{B}(C+\bar{C}) + \bar{A}.\bar{B}$

$= A(1) + \bar{A}.\bar{B}(1) + \bar{A}.\bar{B}$ $\quad \left\{ \begin{array}{l} 1+BC = 1 \\ C+\bar{C} = 1 \end{array} \right.$

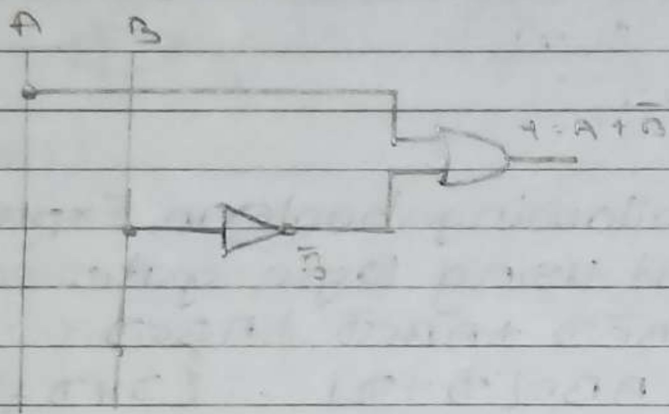
$= A + \bar{A}.\bar{B} + \bar{A}.\bar{B}$

$= A + \bar{A}.\bar{B}$ $\quad .. \{ \bar{A}\bar{B} + \bar{A}\bar{B} = \bar{A}\bar{B}$

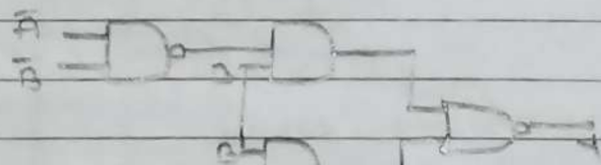
$(A+\bar{A}).(A+\bar{B})$ $\quad .. \{ A+\bar{A} = 1 \{ A+BC = (A+B)(A+C)$

$= 1(A+\bar{B})$

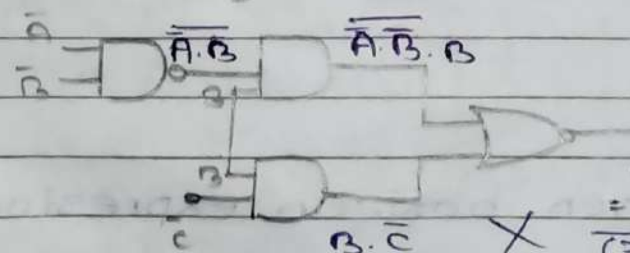
$Y = A+\bar{B}$



- For given Figure derived boolean expression of Y



→



$Y = \overline{\overline{\bar{A}.\bar{B}}.B + B.\bar{C}}$

$= \overline{\overline{\bar{A}.\bar{B}}B} . \overline{B.\bar{C}}$

$= (\bar{\bar{A}} + \bar{\bar{B}}) B . (\bar{B} + \bar{\bar{C}})$ $\quad .. \{ \overline{A.B} = \bar{A} + \bar{B}$

$Y =$

H.W reduce the following boolean expression

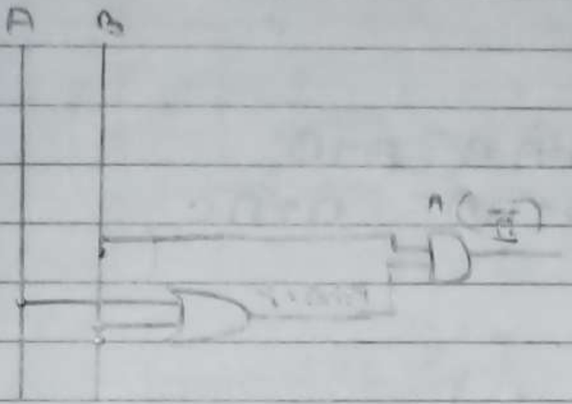
$Y = AB + \bar{A}B + A\bar{B} + \overline{AB}$

$Y = AB + \bar{A}B + A\bar{B} + \overline{AB}$ $\{\bar{A}\bar{B} \quad A.A$

$= B(A + \bar{A}) + A\bar{B} + A.A$ $\{A.A = A \quad \{A + \bar{A} = 1$

$= B(1) + A.\bar{B} + A$

$= B + A(\bar{B})$



Symplify given boolean expression and realize it using logic gate.

- $ABC + \bar{A}\bar{B}C + AB\bar{C} + ABC + \bar{A}\bar{B}\bar{C}$

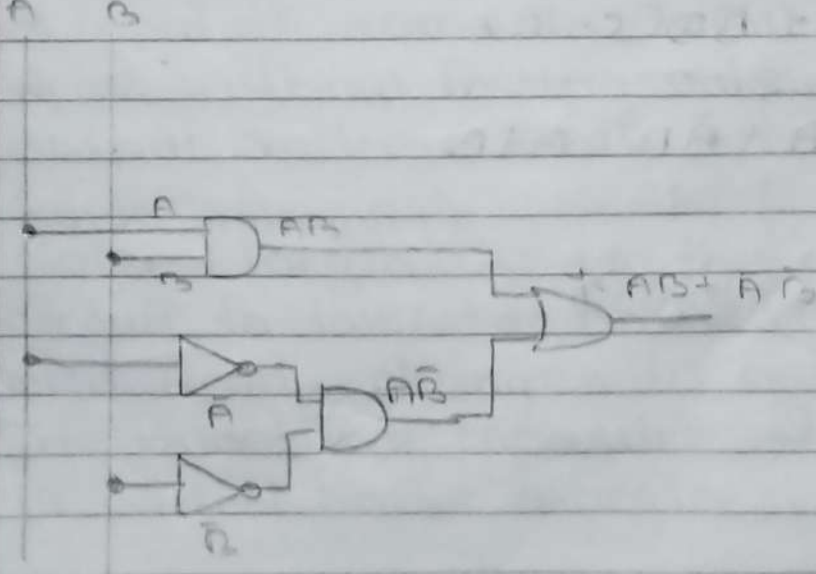
$\rightarrow ABC + ABC + AB\bar{C} + \bar{A}\bar{B}\bar{C}$

$ABC + AB\bar{C} + \bar{A}\bar{B}[C + \bar{C}]$ $\{ABC + ABC = ABC$

$AB[C + \bar{C}] + \bar{A}\bar{B}(1)$ $\therefore \{C + \bar{C} = 1$

$AB(1) + \bar{A}\bar{B}$

$AB + \bar{A}\bar{B}$



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$Y = \bar{A}\bar{B}C + B\bar{C} + \bar{A}BC + ABC$

$= \cancel{ABC + B\bar{C} + \bar{A}BC + \bar{A}\bar{B}C}$

$= \cancel{BC}$

$= \bar{A}\bar{B}C + B\bar{C} + \bar{A}BC + ABC$

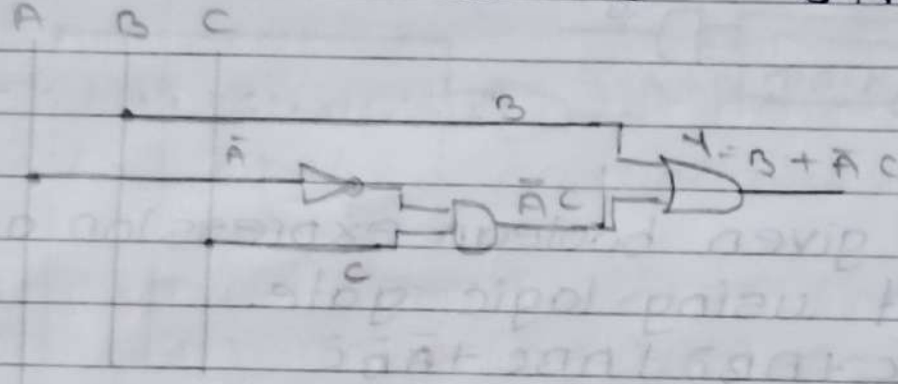
$= \bar{A}\bar{B}C + B\bar{C} + BC(\bar{A} + A)$

$= \bar{A}\bar{B}C + B\bar{C} + BC$

$= \bar{A}\bar{B}C + B(\bar{C} + C)$

$= \bar{A}\bar{B}C + B$

$= B + \bar{A}C$ $\quad \cdots \begin{cases} A + \bar{A}B = A + B \\ B + \bar{B}\bar{A}C = B + \bar{A}C \end{cases}$



- $Y = B\bar{C}\bar{D} + \bar{A}BD + ABD + BC\bar{D} + \bar{B}CD + \bar{A}\bar{B}\bar{C}D + A\bar{B}\bar{C}D$

$\to B\bar{C}\bar{D} + BC\bar{D} + \bar{A}BD + ABD + \bar{B}CD + \bar{A}\bar{B}\bar{C}D + A\bar{B}\bar{C}D$

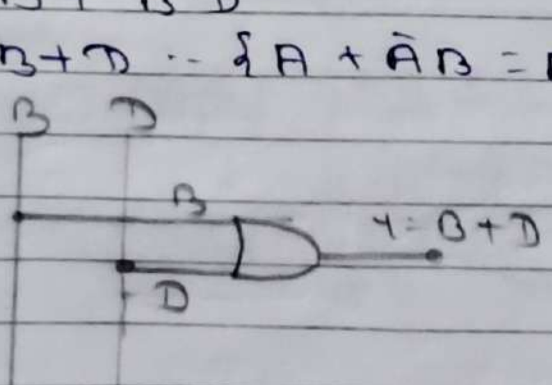
$= B\bar{D}(\bar{C} + C) + BD(\bar{A} + A) + \bar{B}CD + \bar{B}\bar{C}D(\bar{A} + A)$

$= B\bar{D} + BD + \bar{B}CD + \bar{B}\bar{C}D$

$= B(\bar{D} + D) + \bar{B}D(C + \bar{C})$

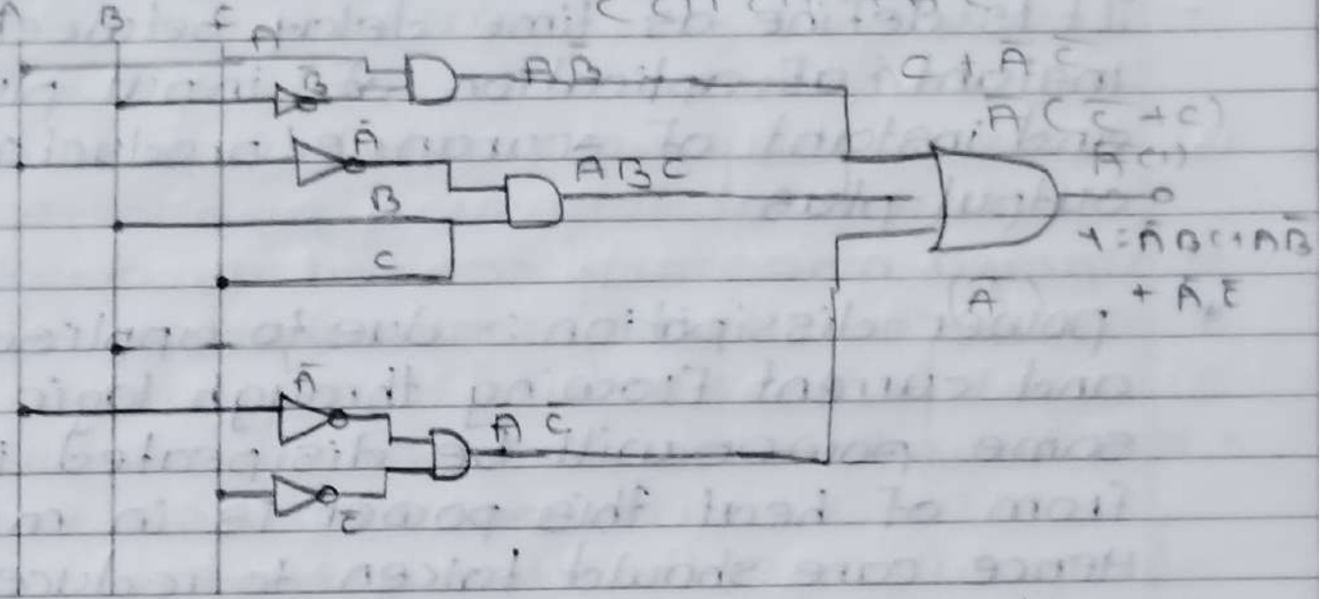
$= B + \bar{B}D$

$= B + D$ $\quad \cdots \{A + \bar{A}B = A + B$



unwanted signal
noise

• $Y = \bar{A}BC + A\bar{B} + \bar{A}\bar{C}$ $= C(\bar{A}+A)(\bar{B}+B) + \bar{A}\bar{C}$
$C(1)(1) + \bar{A}\bar{C}$
$C + \bar{A}\bar{C}$
$\bar{A}(\bar{C}+C)$
$\bar{A}(1)$



[IC] = integrated circuit

8/8/23 logic family's

- Various digital ICS available in market are on different types this types are known as family's.
- characteristics of digital IC
* i] fan-in:- It is define as the no of inputs a get as
  Ex:- three input get has fan in equal to 2 max
* ii] fan-out:- It is define as the max no of input of same IC family that get can drive without falling outside the specified output voltage limit.

(Noise immunity)
* Noise Margin:- It is the ability of logic circuit to tolerate noise without causing and it any changes in output.
- The quantitive measure of noise amidity margin is called noise margin

* prapogation deley (speed of operation)
- It is define as time delay between instant of aplication of input plus and instant of ocurance/production of output plus

* power dissipation :- due to applied voltage and current Flowing through logic IC some power will be disipeated in the from of heat this power is in m/W Hence care should taken to reduced power disipation taking place in IC to protect IC.

* Figure of merit :- It is the product of prapogation delay and power dissipation is called Figure of merit.

Figure of merit = prapogation delay x power dissipation.

Difference between TTL and CMOS logic family

	Parameter	TTL	CMOS
1]	Basic gate	NAND	NOR/NAND.
2]	prapogation delay	10 nanols / n/s	70 n/s
3]	Fan out	10	50
4]	power dissipation per gate	10 m/W	0.1 m/w.
5]	Speed power product (Figure of merit)	100 PJ (Piko Jule)	0.7 PJ

6]	Noise immunity	0.2V	5V

Questions.

W-22. 4-marks 1] Sketch the given boolean expresion using one AND gate and one OR gate only

$Y = AB + AC \quad A(B+C)$

4marks S-23 2] Realize the Following operation using only NOR gate AND, OR, NOT

3] Draw symbol truth table and logical output equation of OR and X-OR gate.

4] Write difference betⁿ TTL and CMOS logic familys. on the basis of Fanout, prapogation delay. power dessipation and Figure of merit.

S-22 5] State and prove D.Morgan's theorem.

6] Draw basic gates AND, OR, NOT using NAND gate only

7] realize the given boolean expresion using basic gate and symlify the same.

$Y = AB + BC(B+C)$

8] compare TTL and CMOS with Following points

Fan out, basic gate, prapogation delay and power deceplation.

W-19 9] Draw symbol truth table and logic eqⁿ of ex-OR gate

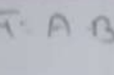
10] State d-Morgans theorem.

11] Simplify the Following boolean expresion and impliment using logic gate

$Y = AB\bar{C}\bar{D} + AB\bar{C}D + ABC\bar{D} + ABCD$

$= AB\bar{C}(\bar{D}+D) + ABC(\bar{D}+D)$

$= AB\bar{C}(1) + ABC(1) = AB(\bar{C}+C) = AB$



$Y: AB$

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12] realize the following expresion using only NAND gate,
OR, AND, NOT.
13] compare TTL and CMOS logic Family on the basis of Following point
basic gate, pd, Fan out, power d.
Noise imunity. and speed power product
S-19] 14] DiFine Fan in and Fan out of a gate
15] Draw logical symbol and x-OR and x-NOR gate
16] SimpliFy the Following and realize it.
$Y = A + \bar{A}\bar{B}C + \bar{A}\bar{B}\bar{C} + A\,BC + \bar{A}\bar{B}$
17] Explain the Following characteristic with respect
1) Noise margin, 2] Pd 3] SoF operation
4] Figure of merit.
18] state and Prove D. Morgan's theorem
19] Design basic logic gate using NAND and NOR gate.
6m
S-18) 20] Draw the Symbol of AND gate and OR gate
21] Draw the symbole truth table and logic expression of any one universal logic gate. write reason why it is called universal gate.
22] compare TTL and CMOS logic family's on the basis of
Pd, power d. Fanout. and basic gate
23] realize the basic logic gate by using NOR gate only.
24) State and prove D. Morgan's theorem.

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S.Q. 1] Compare TTL and CMOS on the basis of pd. Power d. Fan out & basic gate

2] realize the basic gate using only NAND gate 3D raw symbole truth table and logic expression or two input universal gate.

3] Reduce the Follow boolean expression

$Y = AB + \bar{A}B + A\bar{B} + \overline{AB}$