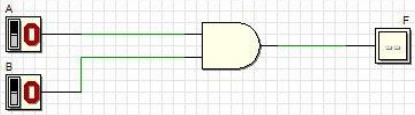
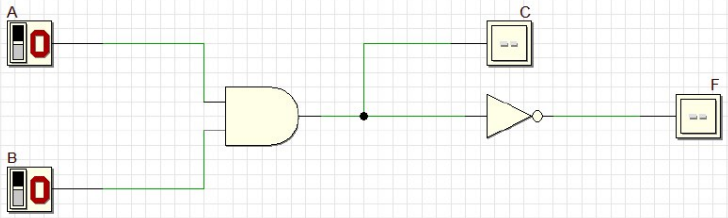
Digital logic lab
Session 2024/2025 Sem1
Aw Xu Yuen A24CS0052
Lai Shi Ni A24CS0298



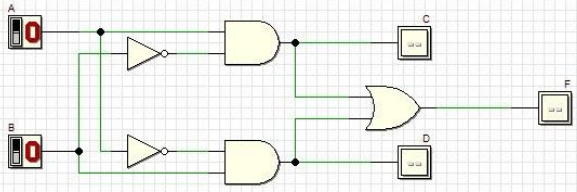
Part 1
Circuit 1

Input	Output
AB	F
0 0	0
0 1	0
1 0	0
1 1	1



Part 2
Circuit 2

A	B	C	F
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0



Part 3
Circuit 3

ABCD	F
0 0 0 0	0
0 1 0 1	1
1 0 1 0	1
1 1 0 0	0