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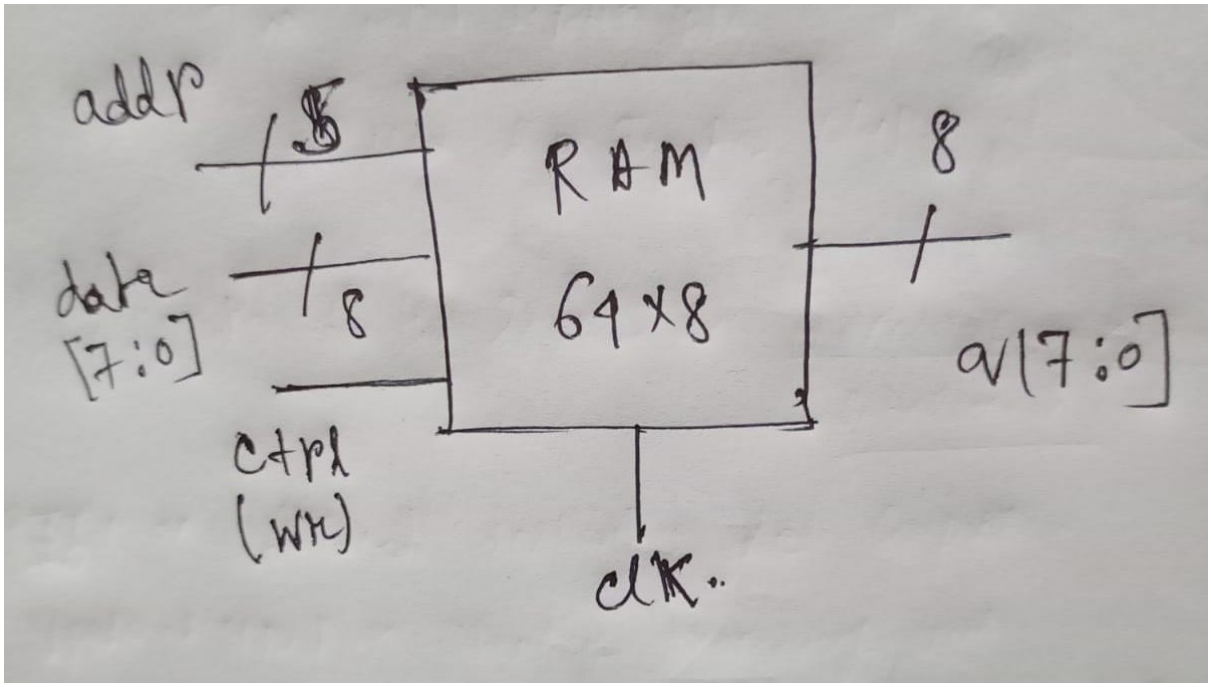
REG. NO.: **22PIMT03**

COURSE: **ICT**

DESIGN A SINGLE PORT AND DUAL PORT RAM

OBJECTIVE: Our aim is to design a Single Port RAM using Behavioural Modelling in Xilinx Vivado using Verilog code.

BLOCK DIAGRAM:



CODE SNIPPET:

```
1   `timescale 1ns / 1ps
2
3   module ram_singe_port(data,clk, addr, wr, q );
4   input [7:0] data;
5   input [5:0] addr;
6   input wr,clk ;
7   output reg [7:0] q;
8   reg [7:0]ram[63:0];
9   always @(posedge clk)
10  begin
11  if(wr)
12  ram[addr] <= data;
13  else
14  q <= ram[addr];
15  end
16
17
18  endmodule
```

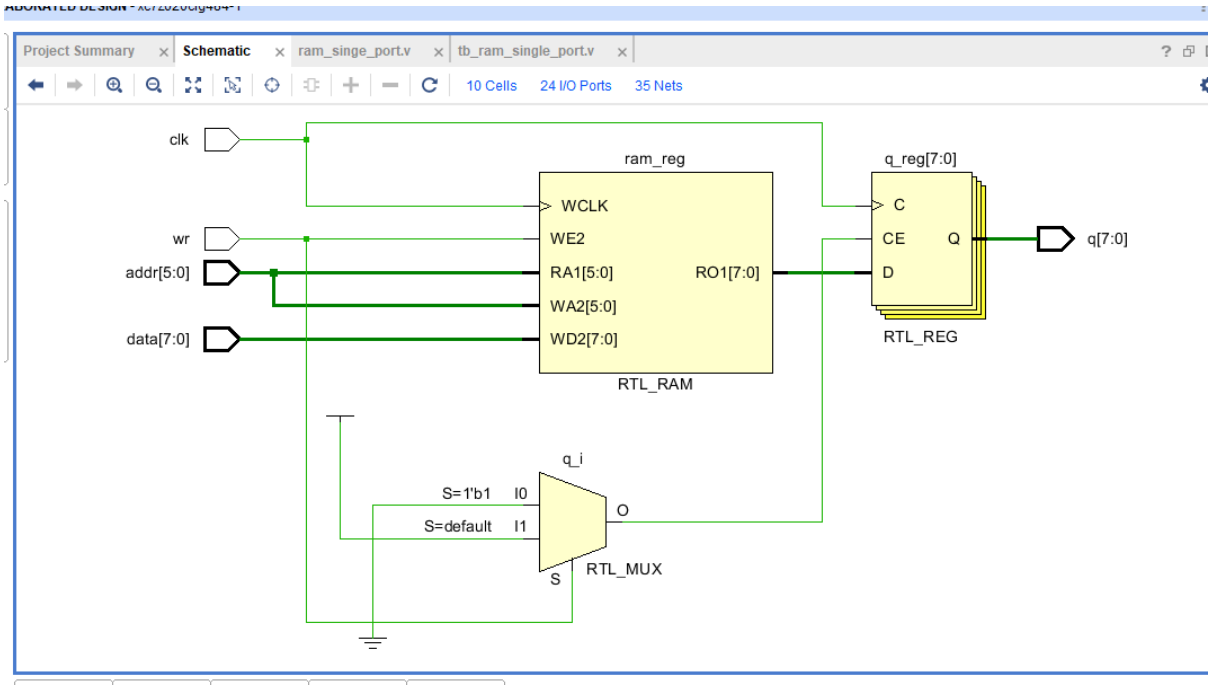
TESTBENCH:

ram_singe_port.v | tb_ram_single_port.v | Untitled 4

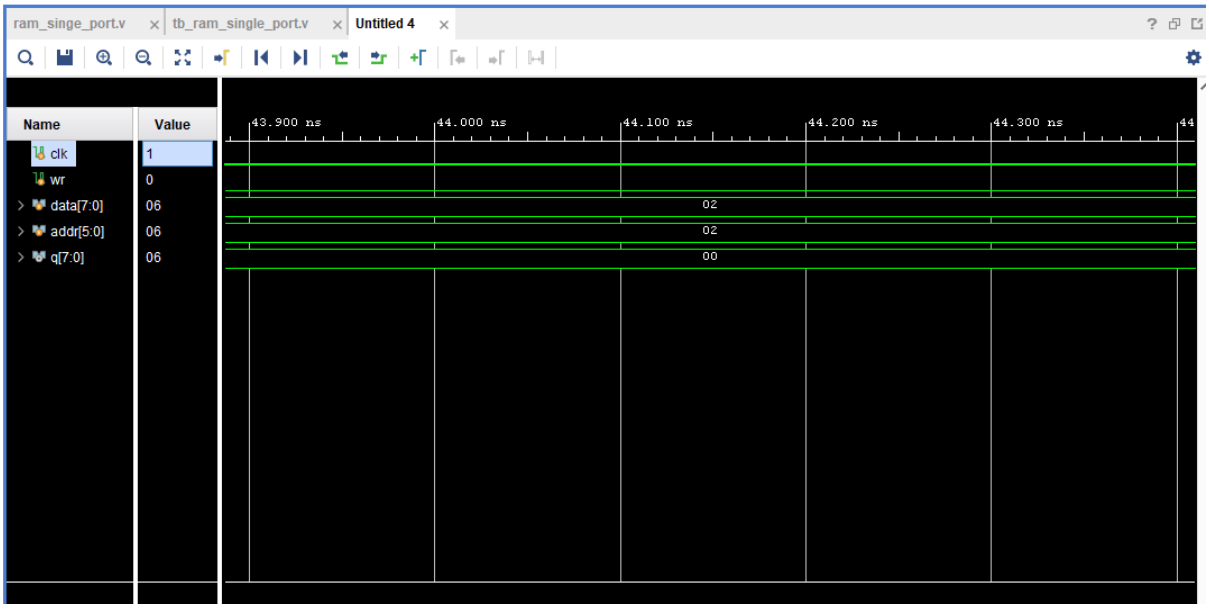
C:/Users/HP/Desktop/souvik_lab_report/Vivado/ram_shib/ram_shib.srcs/sim_1/new/tb_ram_single_port.v

```
4
5   reg clk=0, wr=0;
6   reg  [7:0]data=8'b00000000;
7   reg [5:0]addr=6'b000000;
8   wire [7:0]q;
9   ram_singe_port DUT (.data(data),.clk(clk), .addr(addr), .wr(wr), .q(q) );
10  always #5 clk=~clk;
11
12
13  initial begin
14
15  #10; data= 8'b00000000; addr=6'b000000; wr=1;
16  #10; addr=6'b000000; wr=0;
17  #10; data= 8'b00000010; addr=6'b000010; wr=1;
18  #10; addr=6'b000010; wr=0;
19  #10; data= 8'b00000100; addr=6'b000100; wr=1;
20  #10; addr=6'b000100; wr=0;
21  #10; data= 8'b00000110; addr=6'b000110; wr=1;
22  #10; addr=6'b000110; wr=0;
23  #10; $stop;
24
25
26  end
27
28  endmodule
```

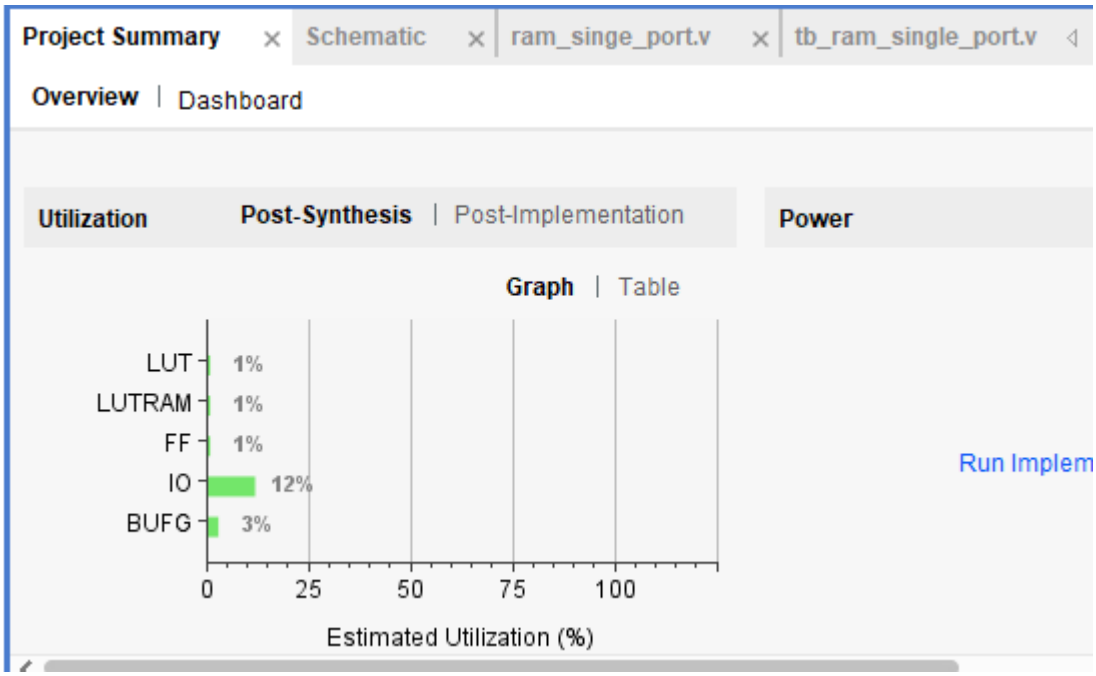
SCHEMATIC GENERATED:

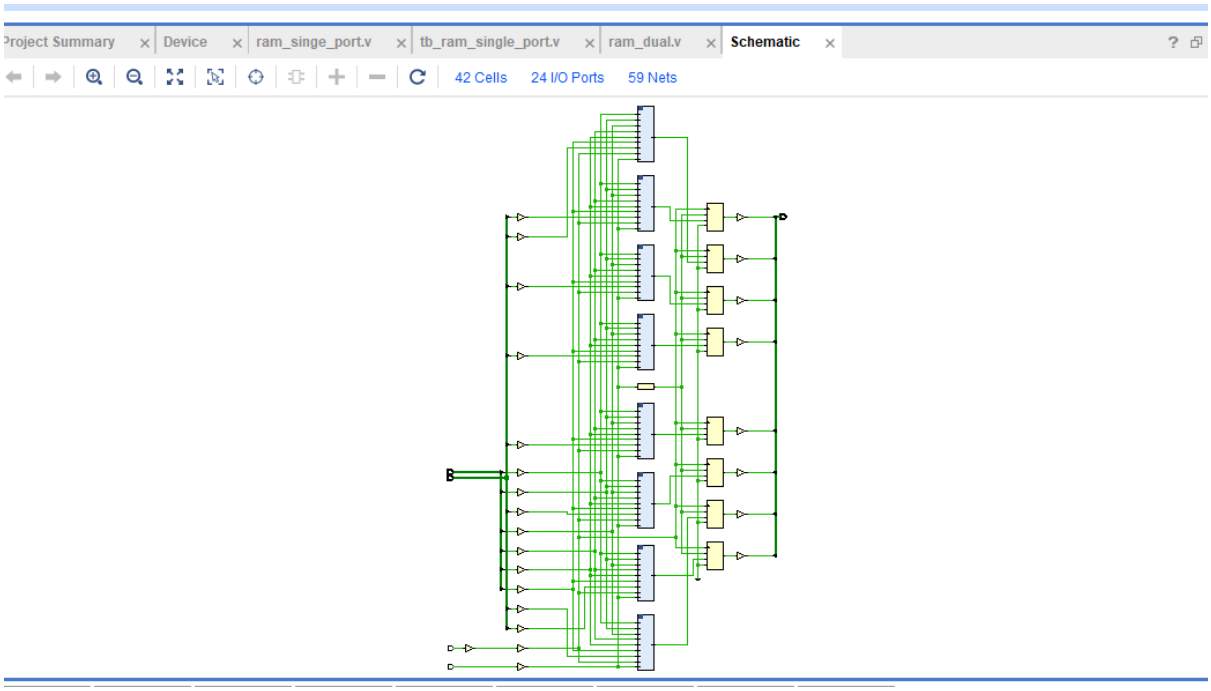


TIMING DIAGRAM:



SYNTHESIS: Running Synthesis for our design and inspecting the utilization reports, we get:



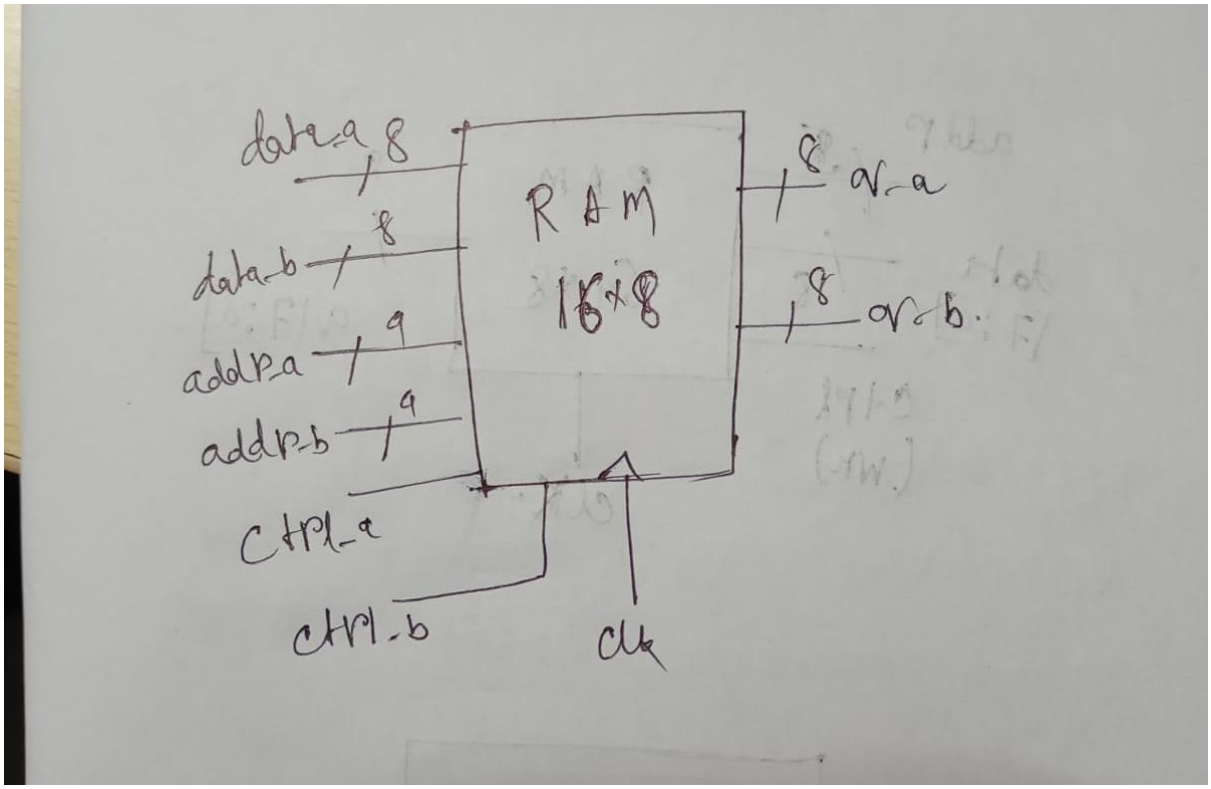


CONCLUSION: Single Port RAM of (64X8) memory size has been designed and simulated behaviourally using Xilinx Vivado and Utilization Reports and stats post synthesis were observed.

DESIGN A DUAL PORT RAM

OBJECTIVE: Our aim is to design a (16X8) Dual Port RAM using Behavioural Modelling in Xilinx Vivado using the Verilog code.

BLOCK DIAGRAM:



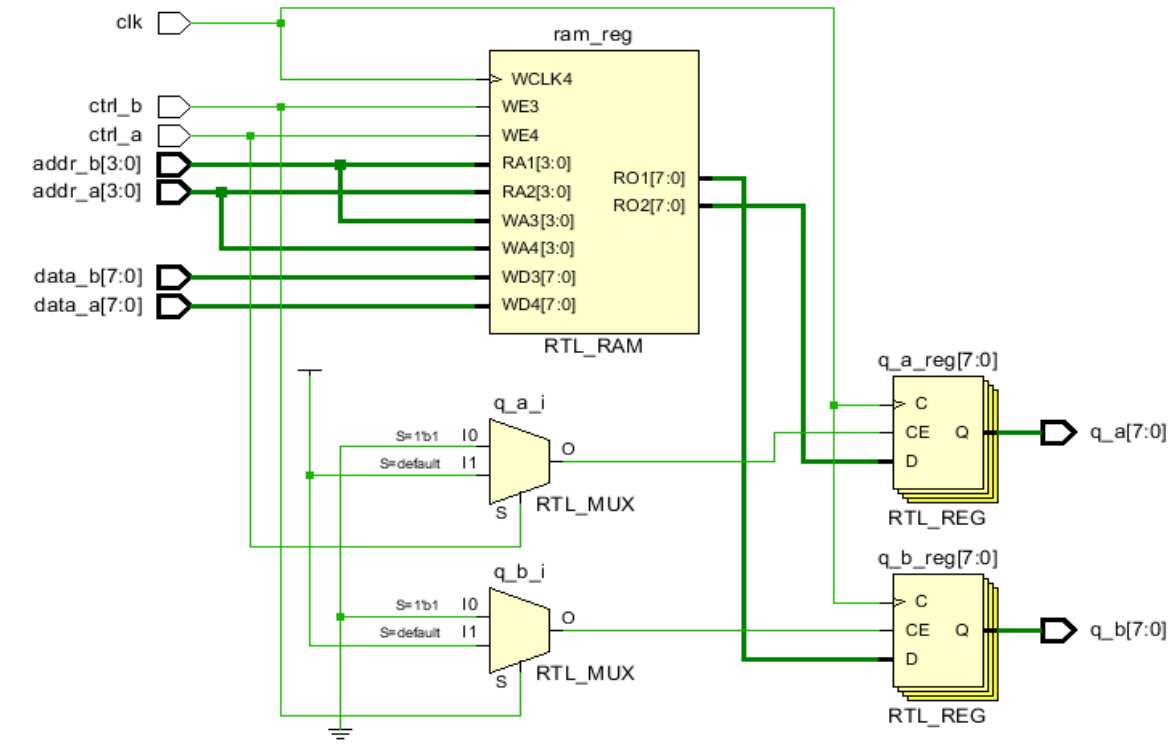
CODE:

```
`timescale 1ns / 1ps
module dpram16to8(clk,ctrl_a,ctrl_b,addr_a,addr_b,data_a,data_b,q_a,q_b);
    input clk, ctrl_a,ctrl_b;
    input [3:0] addr_a, addr_b;
    input [7:0] data_a,data_b;
    output reg [7:0] q_a, q_b;
    reg [7:0]ram[15:0];
    always @(posedge clk)
    begin
    if(ctrl_a)
    ram[addr_a]<=data_a;
    else
    q_a<=ram[addr_a];
    end
    always @(posedge clk)
    begin
    if(ctrl_b)
    ram[addr_b]<=data_b;
    else
    q_b<=ram[addr_b];
    end
endmodule
```

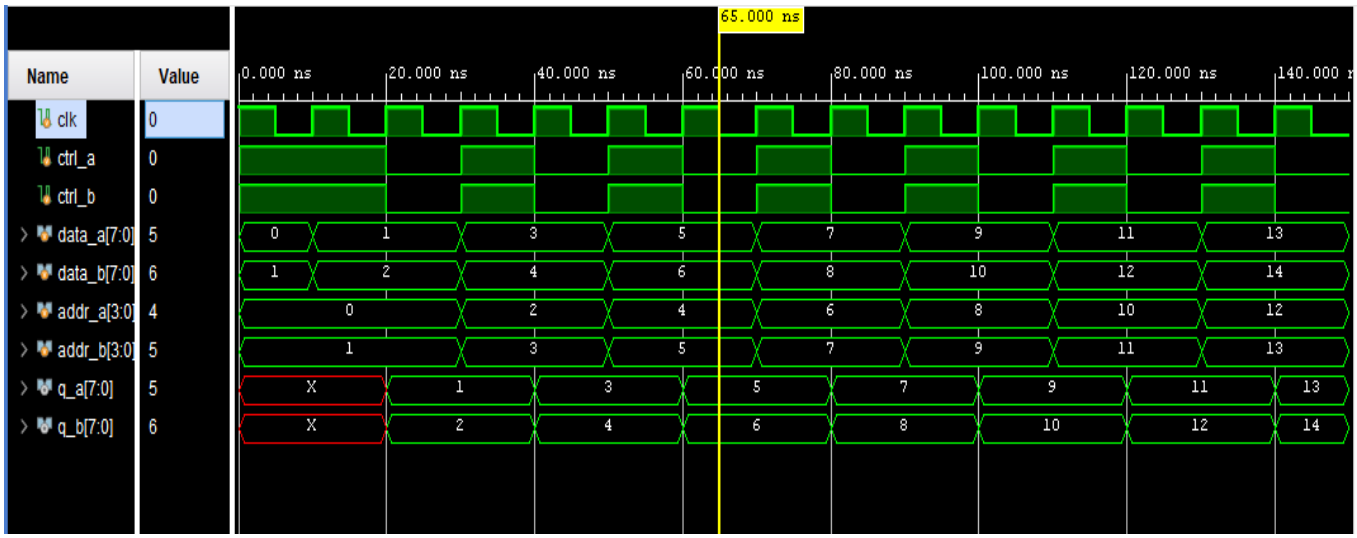
TESTBENCH:

```
`timescale 1ns / 1ps
module tb_dpram16to8();
reg clk =1,ctrl_a = 1,ctrl_b = 1;
reg [7:0] data_a = 8'b00000000, data_b = 8'b00000001;
reg [3:0] addr_a = 4'b0000, addr_b = 4'b0001;
wire [7:0] q_a,q_b;
dpram16to8 uut(.clk(clk),.ctrl_a(ctrl_a),.ctrl_b(ctrl_b),.addr_a(addr_a),.addr_b(addr_b),.data_a(data_a),.data_b(data_b),.q_a(q_a),.q_b(q_b));
always #5 clk =~clk;
initial begin
#10; data_a=8'd1;data_b = 8'd2;addr_a = 4'b0000;addr_b = 4'b0001;ctrl_a=1;ctrl_b = 1;
#10; addr_a = 4'b0000; addr_b = 4'b0001; ctrl_a = 0; ctrl_b = 0;
#10; data_a=8'd3;data_b = 8'd4;addr_a = 4'b0010;addr_b = 4'b0011;ctrl_a=1;ctrl_b = 1;
#10; addr_a = 4'b0010; addr_b = 4'b0011; ctrl_a = 0; ctrl_b = 0;
#10; data_a=8'd5;data_b = 8'd6;addr_a = 4'b0100;addr_b = 4'b0101;ctrl_a=1;ctrl_b = 1;
#10; addr_a = 4'b0100; addr_b = 4'b0101; ctrl_a = 0; ctrl_b = 0;
#10; data_a=8'd7;data_b = 8'd8;addr_a = 4'b0110;addr_b = 4'b0111;ctrl_a=1;ctrl_b = 1;
#10; addr_a = 4'b0110; addr_b = 4'b0111; ctrl_a = 0; ctrl_b = 0;
#10; data_a=8'd9;data_b = 8'd10;addr_a = 4'b1000;addr_b = 4'b1001;ctrl_a=1;ctrl_b = 1;
#10; addr_a = 4'b1000; addr_b = 4'b1001; ctrl_a = 0; ctrl_b = 0;
#10; data_a=8'd11;data_b = 8'd12;addr_a = 4'b1010;addr_b = 4'b1011;ctrl_a=1;ctrl_b = 1;
#10; addr_a = 4'b1010; addr_b = 4'b1011; ctrl_a = 0; ctrl_b = 0;
#10; data_a=8'd13;data_b = 8'd14;addr_a = 4'b1100;addr_b = 4'b1101;ctrl_a=1;ctrl_b = 1;
#10; addr_a = 4'b1100; addr_b = 4'b1101; ctrl_a = 0; ctrl_b = 0;
#10; $stop;
end
endmodule
```

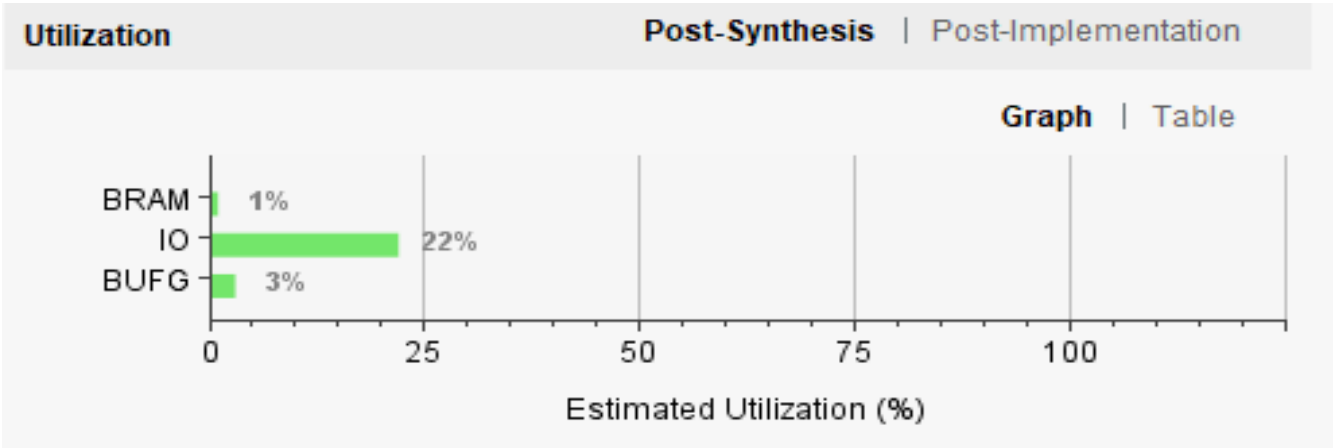
SCHEMATIC GENERATED:

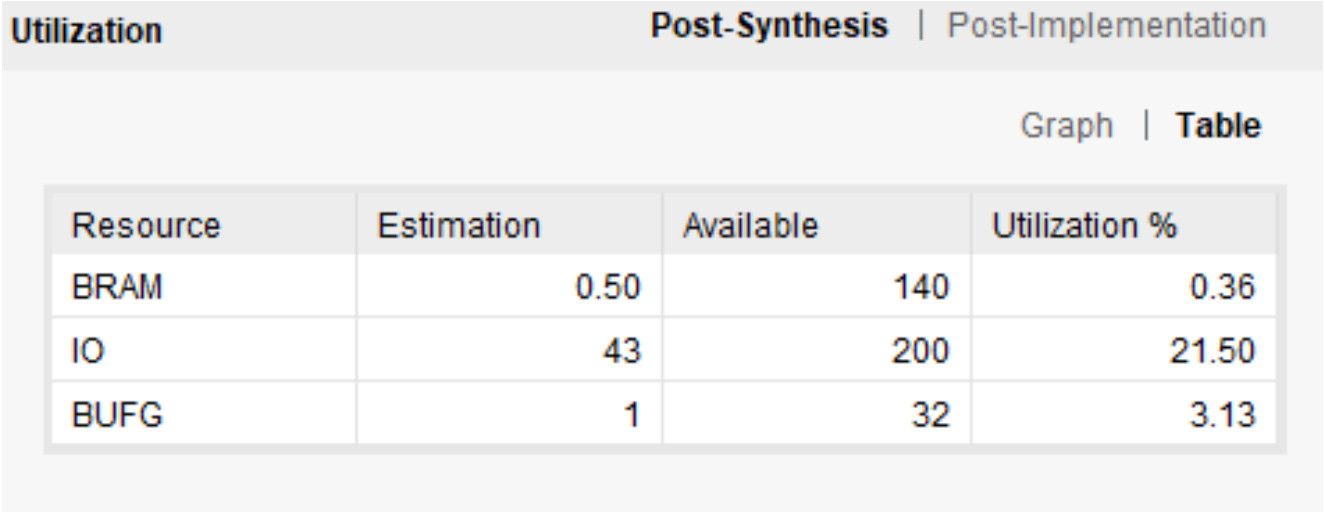


TIMING DIAGRAM:



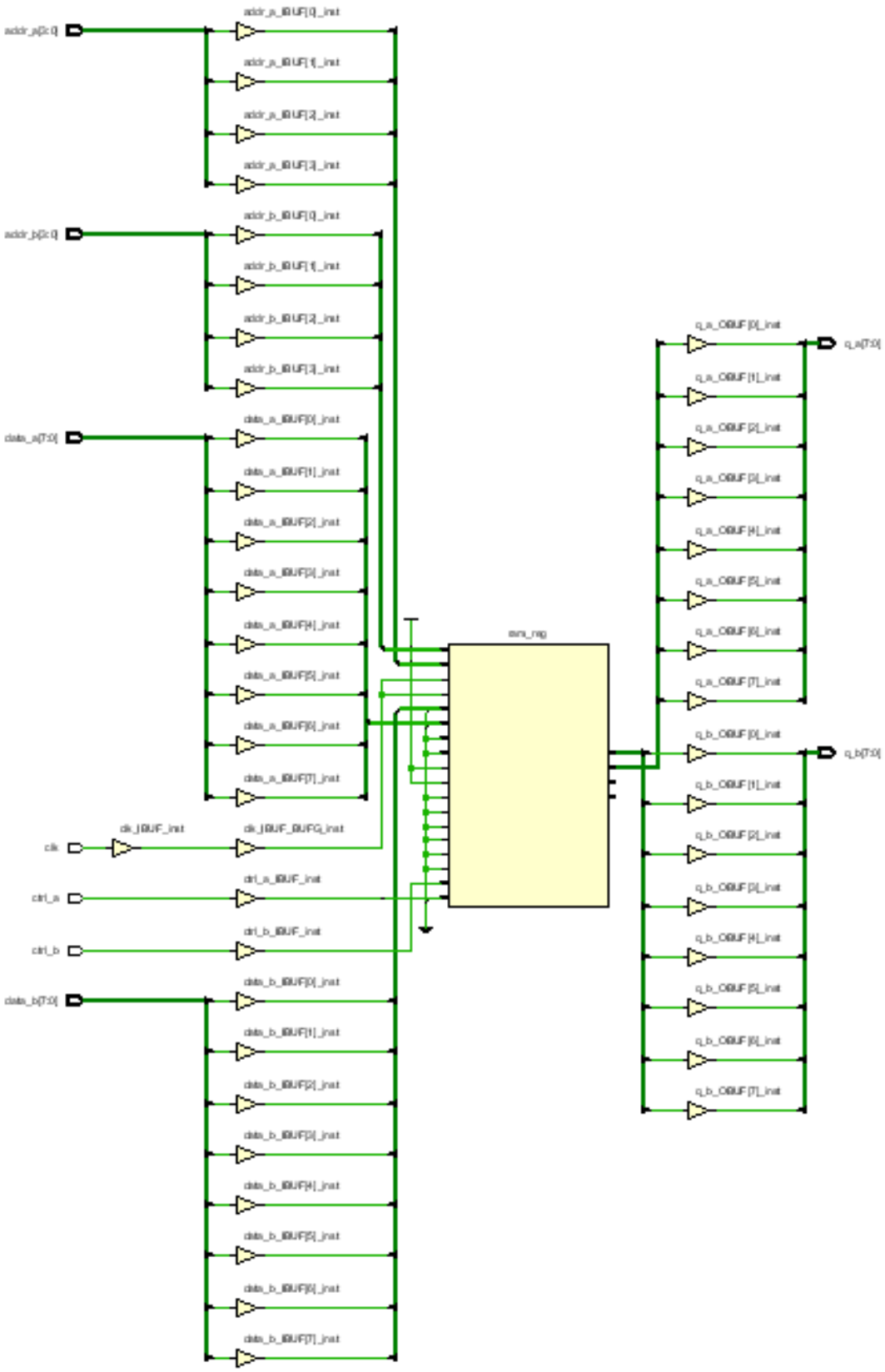
SYNTHESIS:





Resource	Estimation	Available	Utilization %
BRAM	0.50	140	0.36
IO	43	200	21.50
BUFG	1	32	3.13

Also, we observe that the Synthesized Design Schematic varies from our RTL Analysis Elaborated Design Schematic



CONCLUSION: Dual Port RAM of (16X8) memory size has been designed and simulated behaviourally using Xilinx Vivado and Utilization Reports and stats post synthesis were observed.