CS 2410

Computer Architecture

Spring 2022

Distributed: April 4th, 2022

Due: 11:59pm April 13th, 2022

Points: 100

1. (20 pts) Recall our discussion of MESI cache coherence protocol.

   What if a block was shared in two caches and is evicted from one of them. Should we detect this case and set the block to Exclusive in the other cache?

   Please answer the question and justify your answers.

2. (30 pts) Discuss the differences between cache coherence and memory consistency. Also provide examples to clarify the differences between these two concepts.

3. (50 pts) Assume $D cache is initially filled with **word** address 0, 1, 2, …15 memory data (referenced by the datapath in that order). That is, the cache is initially filled with 0-15 memory data. Below is the next sequence of data memory address references given as **word** addresses.

   17, 20, 18, 19, 4, 2, 21, 19, 49, 34, 17, 4

   a) Assuming a direct-mapped $D cache with one-word per cache block and a total size of 16 blocks, list if each reference is a hit or a miss. Show the state of the $D cache after the last reference. What is the hit rate for this reference string?

   b) Now, assuming a direct-mapped $D cache with two-word per block and a total size of 8 blocks, list if each reference is a hit or a miss. Show the state of the $D cache after the last reference. What is the hit rate for this reference string?

   c) Now, assuming a set-associative $D cache with two ways, two-word blocks and a total size of 8 blocks, list if each reference is a hit or a miss (assume LRU replacement). Show the state of the $D cache after the last reference. What is the hit rate for this reference string?