Write Data —16→
Write En →
clk →

D
0
1 —16→ d   q —16→ read Data
           dff
clk   (16 instances)
rst

rst →

=== x
=== z   err
—16→ reduction XOR   === x
                       === z

register

3 bit to 1-hot

regWriteEn

writeRegSel 3/ → 3:8 Decoder 8/ → [mux 1/0] 8/ → writeEn (of register)

8'h00

16/ writeData

writeEn →

writeData → 16/

clk →

rst →

read1RegSel → 3/

read2RegSel → 3/

register
(8 instances)

readData

err 8/

[15:0] readData [7:0]

reduction OR

16 bits × 8 /

readData [0] /16
readData [1] /16
readData [2] /16
readData [3] /16
readData [4] /16
readData [5] /16
readData [6] /16
readData [7] /16

[mux 0 1 2 3 4 5 6 7]

16/ → read1Data

16/ → read2Data

[mux 0 1 2 3 4 5 6 7]

writeEn → [=== x]
writeEn → [=== z]
read1RegSel → [∧] → [===x] [===z]
read2RegSel → [∧] → [===x] [===z]
writeRegSel → [∧] → [===x] [===z]

OR → err

to save space → OR

Note: [∧] is
Reduction XOR

regFile