DSD Exercise Report
Group 18

1. Gate-level simulation cycle time (ns): 0.45
2. Area (um^2): 2609.988548
3. AT score: 12592346.5
4. Screenshot of inferred memory devices in process:

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Inferred memory devices in process
        in routine GSIM line 215 in file
                '../../GSIM.v'.
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|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
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|       x_r_reg       | Flip-flop |  512  |  Y  | N  | Y  | N  | N  | N  | N  |
|       b_r_reg       | Flip-flop |  256  |  Y  | N  | Y  | N  | N  | N  | N  |
|     in_en_r_reg     | Flip-flop |   1   |  N  | N  | Y  | N  | N  | N  | N  |
|     count_r_reg     | Flip-flop |   4   |  Y  | N  | Y  | N  | N  | N  | N  |
|    count_r2_reg     | Flip-flop |   4   |  Y  | N  | Y  | N  | N  | N  | N  |
|     flip_r_reg      | Flip-flop |   1   |  N  | N  | N  | Y  | N  | N  | N  |
|   half_conv_r_reg   | Flip-flop |   1   |  N  | N  | Y  | N  | N  | N  | N  |
|     conv_r_reg      | Flip-flop |   1   |  N  | N  | Y  | N  | N  | N  | N  |
|   slow_mode_r_reg   | Flip-flop |   1   |  N  | N  | Y  | N  | N  | N  | N  |
|   out_valid_r_reg   | Flip-flop |   1   |  N  | N  | Y  | N  | N  | N  | N  |
|    prod_sum_reg     | Flip-flop |  38   |  Y  | N  | Y  | N  | N  | N  | N  |
================================================================================
```

5. Difference between 0.13$\boldsymbol{\mu m}$ technology and 16nm ADFP (ex: area, timing, ...):
The smaller feature size and FinFET structures of 16nm ADFP offer higher density than 130nm, enabling significantly smaller chip area. The delay is also relatively low because of short channels and FinFET switching speed.