

## Referances with Notes

### References with notes

- [1] R. Woods, J. McAllister, G. Lightbody and Y. Yi, FPGA-based implementation of signal processing systems, John Wiley & Sons, 2008.

- [2] N. H. E. Weste and D. Harris, CMOS VLSI design: a circuits and systems perspective, Pearson Education India, 2015.

Note: I have used reference number 1,2 for abstract as both gives an overview of VLSI technology focusing on circuit and discusses various techniques from basic level.

- [3] J. P. Uyemura, "Introduction to VLSI circuits and systems," 2002.

Note: I used this book from pg- 150-175 where it gives a detailed overview of the design flow in VLSI and elaborates on the verification processes necessary at each stage to ensure compliance with design requirements.

- [4] D. Thomas and P. Moorby, The Verilog® hardware description language, Springer Science & Business Media, 2008.

Note: From pg 320-345 this book covers advanced aspects of hardware description languages, including DPI and PSS, and their application in VLSI design.

- [5] C. Spear, SystemVerilog for verification: a guide to learning the testbench language features, Springer Science & Business Media, 2008.

Note: I used the from page 150-175. This reference provides insights into OVM and its application in constructing efficient testbenches.

- [6] R. S. Pressman, Software engineering: a practitioner's approach, Palgrave macmillan, 2005.

Note: This book from pg. 123-145 provides a detailed exploration of the V-Model, particularly its structured approach and application in various testing scenarios, including its strengths and limitations.

- [7] D. L. Perry, VHDL: programming by example, McGraw-Hill Education, 2002.

Note: I used it from pp. 50-75. Perry's work covers the VModel framework, detailing its application in managing the VLSI design process.

- [8] Z. Navabi, Digital design and implementation with field programmable devices, Springer Science & Business Media, 2004.

Note: I used it from pp. 85-110. This book provides an in-depth look at simulators, their role in dynamic verification, and their limitations in handling large designs.

[9] C. Mead and L. Conway, *Introduction to VLSI systems*, Addison-wesley Reading, MA, 1980.

[10] R. H. Katz, *Contemporary Logic Design The Benjamin*, Cummings, 1994.

[11] H. Kaeslin, *Digital integrated circuit design: from VLSI architectures to CMOS fabrication*, Cambridge University Press, 2008.

[12] J. L. Hennessy and D. A. Patterson, *Computer architecture: a quantitative approach*, Elsevier, 2011.

Note: This book offers insights into architectural design decisions based on system specifications, focusing on design techniques, function, performance, and size.

[13] O. Grumberg, E. M. Clarke and D. Peled, "Model checking," in *International Conference on Foundations of Software Technology and Theoretical Computer Science; Springer: Berlin/Heidelberg, Germany*, 1999.

Note: This source give details of formal verification in VLSI, using mathematical methods to prove the correctness of designs.

[14] M. D. Ciletti, *Advanced digital design with the Verilog HDL*, vol. 1, Prentice hall Upper Saddle River, 2003.

Note: From pp. 215-240. Ciletti's work explores the enhancements System Verilog brings to Verilog, particularly for verification and validation purposes

[15] J. Bergeron, *Writing testbenches using SystemVerilog*, Springer Science & Business Media, 2007.

Note: From 101-120. This book provides an in-depth discussion on UVM, focusing on its framework and class library for developing scalable and reusable testbenches.

[16] P. J. Ashenden, *The designer's guide to VHDL*, Morgan kaufmann, 2010.

[17] M. Abramovici, M. A. Breuer, A. D. Friedman and others, *Digital systems testing and testable design*, vol. 2, Computer science press New York, 1990.

Note: This source emphasizes the critical role of design verification at each stage of the VLSI design flow, addressing the need for thorough verification to ensure compliance with design specifications

[18] D. Kim, *FPGA-Accelerated Evaluation and Verification of RTL Designs*, University of California, Berkeley, 2019.

Note: This gives a implementation of RTL tools in a acase study

[19] M. Jaring, R. L. Krikhaar and J. Bosch, "Modeling variability and testability interaction in software product line engineering," in *Seventh International Conference on Composition-Based Software Systems (ICCBSS 2008)*, 2008.

Note: This gives an implementation of Vmodel in a case study.