

EECT/CE 6325 VLSI Design

Fall 2020

PROJECT #5:

D Flip-Flop

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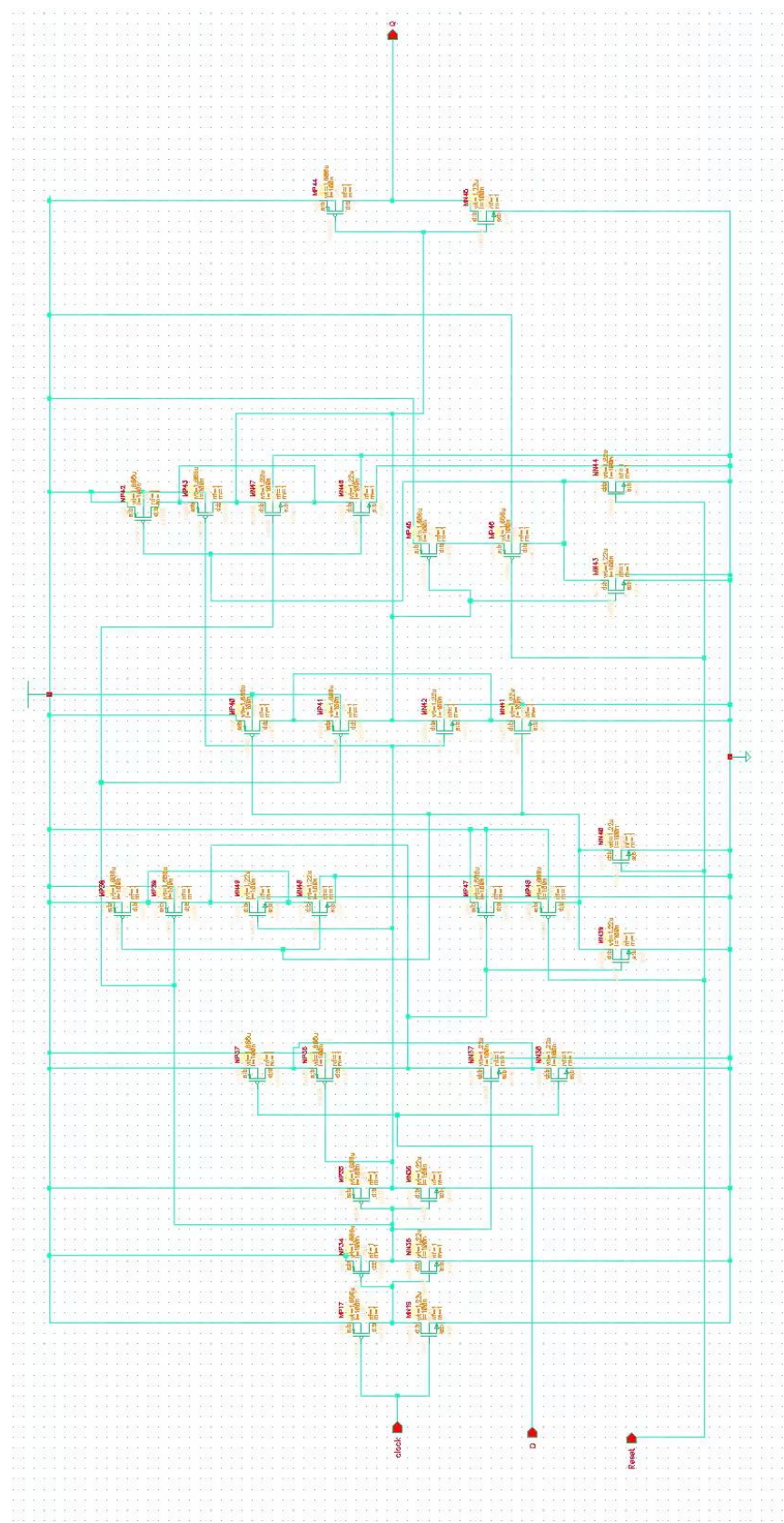
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Figure 1 D Flip-Flop layout

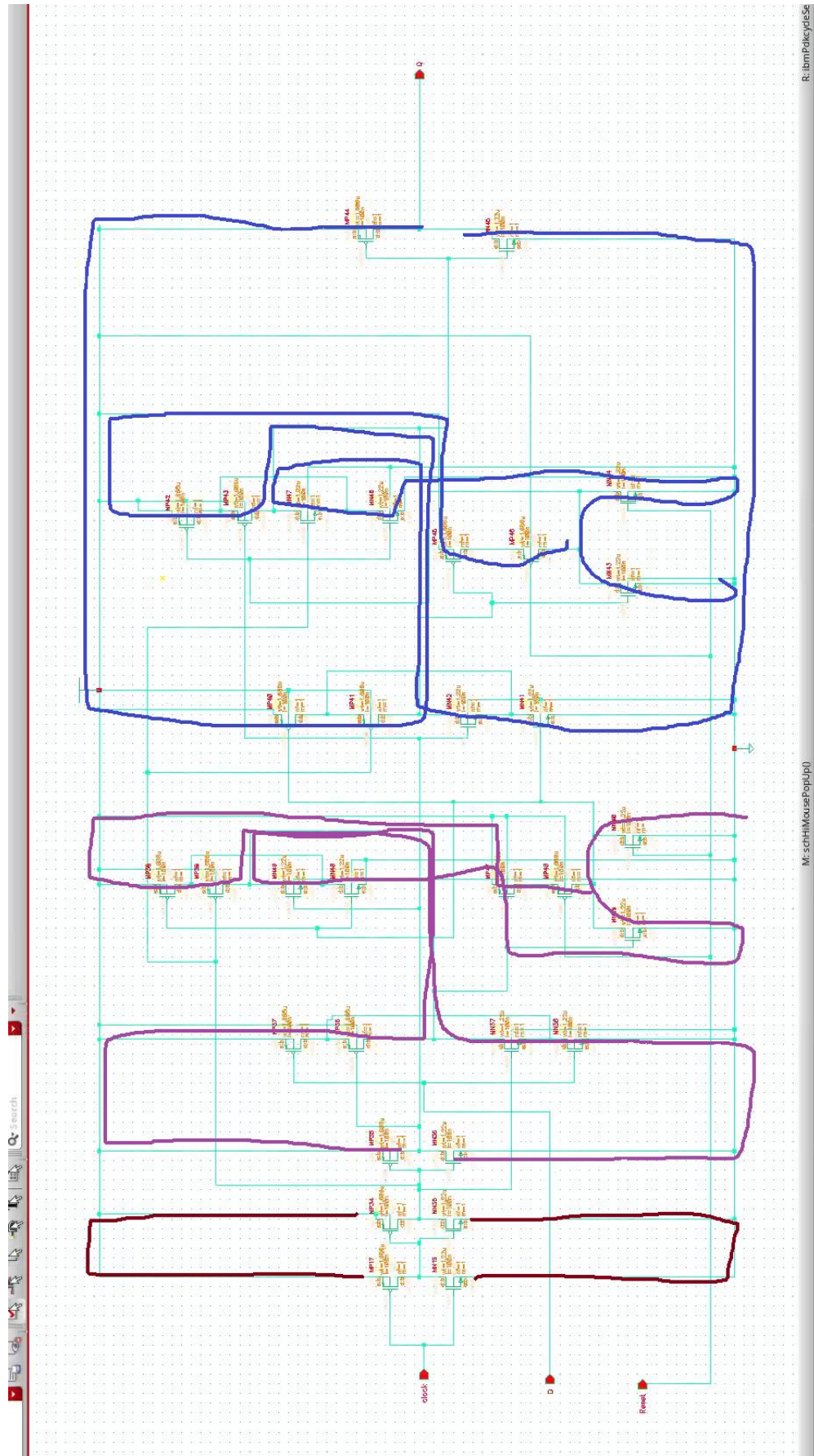
Number of Diffusion break in Layout =2

The diagram shows a hand-drawn circuit for a D flip-flop. At the bottom, a 'Clock' signal is connected to a chain of three inverters. The output of the third inverter is labeled with a clock symbol (a circle with a diagonal slash). The main circuit consists of several logic gates:
 

- An input 'D' is connected to a NAND gate. The other input of this NAND gate is connected to a clock symbol.
- The output of this NAND gate is connected to a NOR gate. The other input of the NOR gate is connected to a 'Reset' signal.
- The output of the NOR gate is connected to an inverter. The output of this inverter is connected to another NOR gate. The other input of this second NOR gate is connected to a clock symbol.
- The output of the second NOR gate is connected to a third NAND gate. The other input of this third NAND gate is connected to a clock symbol.
- The output of the third NAND gate is connected to a fourth NAND gate. The other input of this fourth NAND gate is connected to a clock symbol.
- The output of the fourth NAND gate is connected to a fifth NAND gate. The other input of this fifth NAND gate is connected to a clock symbol.
- The output of the fifth NAND gate is connected to a sixth NAND gate. The other input of this sixth NAND gate is connected to a clock symbol.
- The output of the sixth NAND gate is connected to a seventh NAND gate. The other input of this seventh NAND gate is connected to a clock symbol.
- The output of the seventh NAND gate is connected to an inverter. The output of this inverter is labeled 'Q'.







Euler paths

First trail :  $\text{clock} - \overline{\text{clock}}$

Second trail :  $\phi - D - \bar{\phi} - \text{out2} - \text{out1} - \text{reset}$

Third trail :  $\text{Reset} - \text{out4} - \bar{\phi} - \phi - \text{out2} - \text{out3}$

### 3.Hspice

Checking the functionality to pass “1”

\$example HSPICE setup file

\$transistor model

.include

"/proj/cad/library/mosis/GF65\_LPe/cmos10lpe\_CDS\_oa\_d1064\_11\_20160415/models/YI-SM00030/Hspice/models/design.inc"

.include DFF.pex.netlist

.global vdd! gnd!

.option post runlvl=5

xi GND! q VDD! clock d reset DFF

```
vdd vdd! gnd! 1.2v
```

```
vin clock gnd! pwl(0ns 0v 0.08ns 1.2v 1.5ns 1.2v 1.58ns 0v 3ns 0v 3.08ns 1.2v 4.5ns 1.2v 4.58ns  
0v 6ns 0v 6.08ns 1.2v 7.5ns 1.2v 7.58ns 0v 9ns 0v 9.08ns 1.2v 10.5ns 1.2v 10.58ns 0v 12ns 0v)
```

```
vin2 d gnd! pwl(0ns 0v t 0v 't+80ps' 1.2v)
```

```
vin3 reset gnd! 0v
```

```
cout q gnd! 90f
```

```
$transient analysis
```

```
.tr 0.001ns 12ns sweep t 4.4ns 4.5ns 1ps
```

```
.measure tran tsu trig v(d) val=0.6v rise=1 targ v(clock) val=0.6v fall=2
```

```
.measure tran tclktoq trig v(clock) val=0.6v fall=2 targ v(q) val=0.6v rise=1
```

```
.measure tran td param='tsu+tclktoq'
```

```
.end
```

## Checking the functionality to pass “0”

```
$example HSPICE setup file
```

```
$transistor model
```

```
.include
```

```
"/proj/cad/library/mosis/GF65_LPe/cmos10lpe_CDS_oa_dl064_11_20160415/models/YI-  
SM00030/Hspice/models/design.inc"
```

```
.include DFF.pex.netlist
```

```
.global vdd! gnd!
```

```
.option post runlvl=5
```

xi GND! q VDD! clock d reset DFF

vdd vdd! gnd! 1.2v

vin clock gnd! pwl(0ns 0v 0.08ns 1.2v 1.5ns 1.2v 1.58ns 0v 3ns 0v 3.08ns 1.2v 4.5ns 1.2v 4.58ns  
0v 6ns 0v 6.08ns 1.2v 7.5ns 1.2v 7.58ns 0v 9ns 0v 9.08ns 1.2v 10.5ns 1.2v 10.58ns 0v 12ns 0v)

vin2 d gnd! pwl(0ns 1.2v t 1.2v 't+80ps' 0v)

vin3 reset gnd! 0v

cout q gnd! 90f

\$transient analysis

.tr 0.001ns 12ns sweep t 4.4ns 4.5ns 1ps

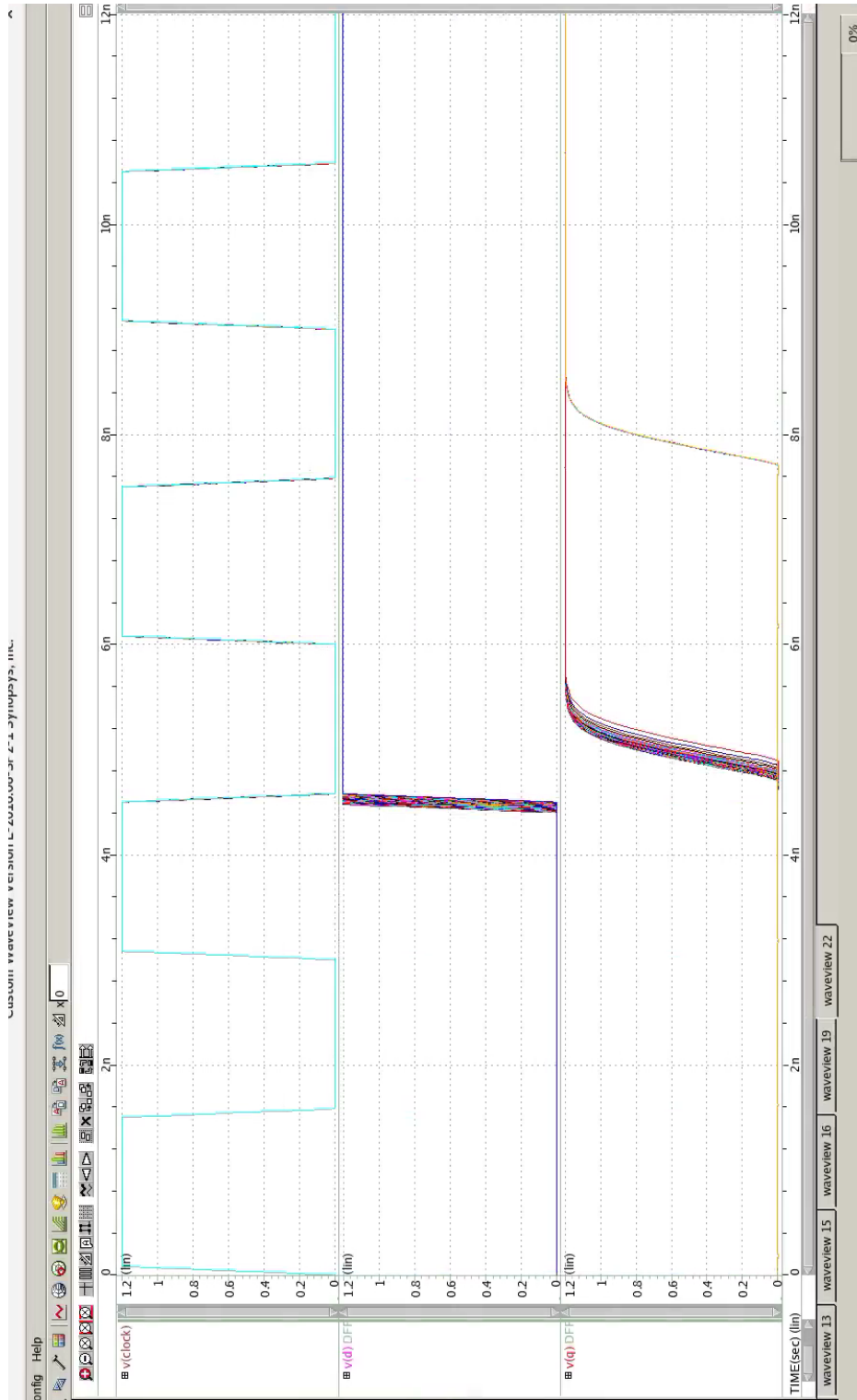
.measure tran tsu trig v(d) val=0.6v fall=1 targ v(clock) val=0.6v fall=2

.measure tran tclktoq trig v(clock) val=0.6v fall=2 targ v(q) val=0.6v fall=1

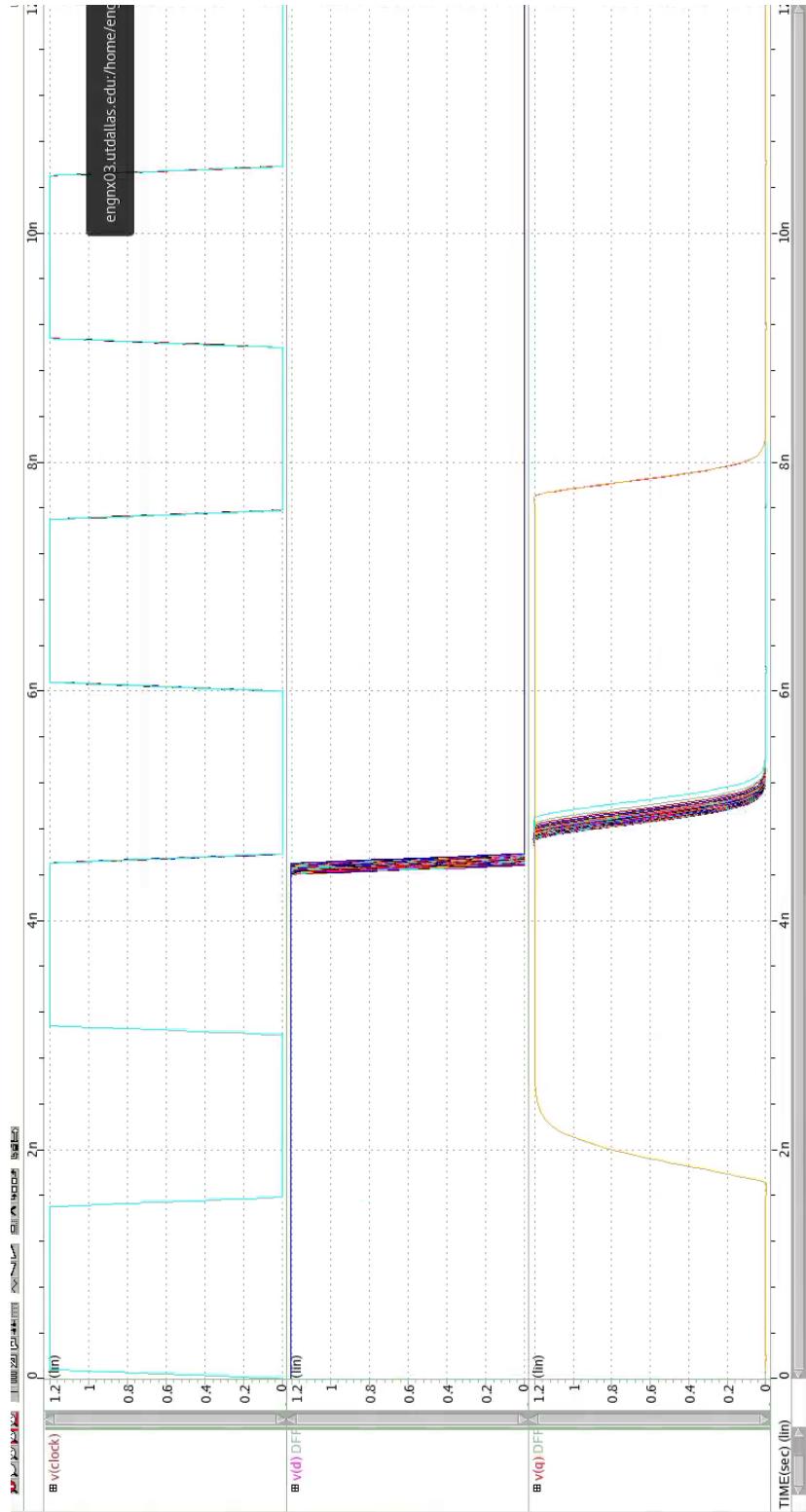
.measure tran td param='tsu+tclktoq'



## Passing “1”



Passing "0"



## 5.Measuring $T_{su\_opt}$ , $T_{su\_dd}$ , $T_{Clk \rightarrow Q}$ , $T_{delay}$ , $T_{hold}$

(1) Drop-dead setup time ( $T_{su\_dd}$ ):

How long before capturing edge that D must be stable

(2) Optimum setup time ( $T_{su\_opt}$ ):

$T_{delay}$  is given by  $T_{su} + T_{Clk \rightarrow Q}$ .  $T_{delay}$  is minimum is called optimum setup time ( $T_{su\_opt}$ )

(3) Hold time ( $T_{hold}$ ):

How long after capturing edge that D must be stable

(4) Clock to Q time ( $T_{Clk \rightarrow Q}$ )

How long after capturing edge does the new output appear

Passing “o”

Time	$T_{su}(0)$	$T_{Clk \rightarrow Q}(0)$	$T_{delay}(0)$	$T_{hold}(0)$
$T_{su\_opt}(0)$	30ps	354ps	384ps	
$T_{su\_dd}(0)$	2ps	517ps	519ps	20ps

DFF.sp			DFF.mt0
	25.0000	1	
4.484e-09	1.600e-11	3.780e-10	3.940e-10
	25.0000	1	
4.485e-09	1.500e-11	3.807e-10	3.957e-10
	25.0000	1	
4.486e-09	1.400e-11	3.837e-10	3.977e-10
	25.0000	1	
4.487e-09	1.300e-11	3.869e-10	3.999e-10
	25.0000	1	
4.488e-09	1.200e-11	3.904e-10	4.024e-10
	25.0000	1	
4.489e-09	1.100e-11	3.941e-10	4.051e-10
	25.0000	1	
4.490e-09	1.000e-11	3.984e-10	4.084e-10
	25.0000	1	
4.491e-09	9.000e-12	4.028e-10	4.118e-10
	25.0000	1	
4.492e-09	8.000e-12	4.083e-10	4.163e-10
	25.0000	1	
4.493e-09	7.000e-12	4.142e-10	4.212e-10
	25.0000	1	
4.494e-09	6.000e-12	4.223e-10	4.283e-10
	25.0000	1	
4.495e-09	5.000e-12	4.328e-10	4.378e-10
	25.0000	1	
4.496e-09	4.000e-12	4.474e-10	4.514e-10
	25.0000	1	
4.497e-09	3.000e-12	4.693e-10	4.723e-10
	25.0000	1	
4.498e-09	2.000e-12	5.174e-10	5.194e-10
	25.0000	1	
4.499e-09	1.000e-12	3.319e-09	3.320e-09
	25.0000	1	
4.500e-09	0.	3.319e-09	3.319e-09
	25.0000	1	

DFF.sp			DFF.mt0
4.463e-09	3.700e-11	3.484e-10	3.854e-10
	25.0000	1	
4.464e-09	3.600e-11	3.492e-10	3.852e-10
	25.0000	1	
4.465e-09	3.500e-11	3.501e-10	3.851e-10
	25.0000	1	
4.466e-09	3.400e-11	3.510e-10	3.850e-10
	25.0000	1	
4.467e-09	3.300e-11	3.519e-10	3.849e-10
	25.0000	1	
4.468e-09	3.200e-11	3.529e-10	3.849e-10
	25.0000	1	
4.469e-09	3.100e-11	3.539e-10	3.849e-10
	25.0000	1	
4.470e-09	3.000e-11	3.549e-10	3.849e-10
	25.0000	1	
4.471e-09	2.900e-11	3.560e-10	3.850e-10
	25.0000	1	
4.472e-09	2.800e-11	3.571e-10	3.851e-10
	25.0000	1	
4.473e-09	2.700e-11	3.583e-10	3.853e-10
	25.0000	1	
4.474e-09	2.600e-11	3.595e-10	3.855e-10
	25.0000	1	
4.475e-09	2.500e-11	3.608e-10	3.858e-10
	25.0000	1	
4.476e-09	2.400e-11	3.622e-10	3.862e-10
	25.0000	1	
4.477e-09	2.300e-11	3.636e-10	3.866e-10
	25.0000	1	
4.478e-09	2.200e-11	3.652e-10	3.872e-10
	25.0000	1	
4.479e-09	2.100e-11	3.670e-10	3.880e-10
	25.0000	1	
4.480e-09	2.000e-11	3.689e-10	3.889e-10

Passing “1”

Time	$T_{su}(1)$	$T_{Clk \rightarrow Q}(1)$	$T_{delay}(1)$	$T_{hold}(1)$
$T_{su_{opt}}(1)$	51ps	403ps	454ps	
$T_{su_{dd}}(1)$	20ps	570ps	590ps	2ps

Time	$T_{su}(1)$	$T_{Clk \rightarrow Q}(1)$	$T_{delay}(1)$
4.469e-09	3.100e-11	4.379e-10	4.689e-10
	25.0000	1	
4.470e-09	3.000e-11	4.415e-10	4.715e-10
	25.0000	1	
4.471e-09	2.900e-11	4.457e-10	4.747e-10
	25.0000	1	
4.472e-09	2.800e-11	4.504e-10	4.784e-10
	25.0000	1	
4.473e-09	2.700e-11	4.553e-10	4.823e-10
	25.0000	1	
4.474e-09	2.600e-11	4.614e-10	4.874e-10
	25.0000	1	
4.475e-09	2.500e-11	4.685e-10	4.935e-10
	25.0000	1	
4.476e-09	2.400e-11	4.777e-10	5.017e-10
	25.0000	1	
4.477e-09	2.300e-11	4.893e-10	5.123e-10
	25.0000	1	
4.478e-09	2.200e-11	5.041e-10	5.261e-10
	25.0000	1	
4.479e-09	2.100e-11	5.272e-10	5.482e-10
	25.0000	1	
4.480e-09	2.000e-11	5.704e-10	5.904e-10
	25.0000	1	
4.481e-09	1.900e-11	3.382e-09	3.401e-09
	25.0000	1	
4.482e-09	1.800e-11	3.382e-09	3.400e-09
	25.0000	1	
4.483e-09	1.700e-11	3.381e-09	3.398e-09
	25.0000	1	
4.484e-09	1.600e-11	3.381e-09	3.397e-09
	25.0000	1	
4.485e-09	1.500e-11	3.382e-09	3.397e-09
	25.0000	1	
4.486e-09	1.400e-11	3.382e-09	3.396e-09



	DFF.sp			DFF.mt0
	25.0000	1		
4.443e-09	5.700e-11	3.980e-10	4.550e-10	
	25.0000	1		
4.444e-09	5.600e-11	3.989e-10	4.549e-10	
	25.0000	1		
4.445e-09	5.500e-11	3.998e-10	4.548e-10	
	25.0000	1		
4.446e-09	5.400e-11	4.007e-10	4.547e-10	
	25.0000	1		
4.447e-09	5.300e-11	4.017e-10	4.547e-10	
	25.0000	1		
4.448e-09	5.200e-11	4.026e-10	4.546e-10	
	25.0000	1		
4.449e-09	5.100e-11	4.035e-10	4.545e-10	
	25.0000	1		
4.450e-09	5.000e-11	4.046e-10	4.546e-10	
	25.0000	1		
4.451e-09	4.900e-11	4.058e-10	4.548e-10	
	25.0000	1		
4.452e-09	4.800e-11	4.068e-10	4.548e-10	
	25.0000	1		
4.453e-09	4.700e-11	4.080e-10	4.550e-10	
	25.0000	1		
4.454e-09	4.600e-11	4.093e-10	4.553e-10	
	25.0000	1		
4.455e-09	4.500e-11	4.105e-10	4.555e-10	
	25.0000	1		
4.456e-09	4.400e-11	4.119e-10	4.559e-10	
	25.0000	1		
4.457e-09	4.300e-11	4.133e-10	4.563e-10	
	25.0000	1		
4.458e-09	4.200e-11	4.147e-10	4.567e-10	
	25.0000	1		
4.459e-09	4.100e-11	4.162e-10	4.572e-10	
	25.0000	1		