# EC316: Microprocessor Project

# Final Report Tic-Tac-Toe against the 8085 Microprocessor

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#### **Synopsis**

The primary objective of our project was to create a hardware implementation of the game 'Tic-Tac-Toe' with the facility of playing against the 8085 microprocessor. The microprocessor algorithmically analyses the state of the game and picks the most optimum move so as to ensure that it always wins or draws. To implement this we used the Minimax algorithm to determine the moves picked by the 8085. This project highlights the decision-making capability of microprocessors. Additionally, a separate mode for player-versus-player games is provided aswell.

Keywords: Minimax Algorithm, 8085 Microprocessor, Game Theory

Date: January 2018

# Acknowledgements

We would like to thank Professor Dhananjay V. Gadre for his guidance and support throughout this project. We would also like to thank the CEDT lab for providing us with facilities to fabricate our board and its members who provided us with valuable help throughout the fabrication process.

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#### 1 Introduction

#### 1.1 Motivation

Tic-Tac-Toe is a game which we have all played at some point in our life and its sheer simplicity contributes to its widespread adoption, making it one of the most popular pen and paper games. The EC-316 course provides the perfect platform to give our beloved game a concrete form. The notion of computer intelligence is one that has always intrigued us and we aim to demonstrate with our project how even a microprocessors from the 70's can be programmed to be unbeatable.

#### 1.2 Description

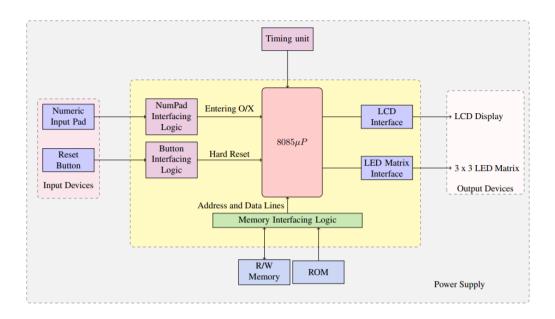


Figure 1: Block Diagram Representation of Proposed Model

Tic-Tac-Toe is a simple two-player game played in turns where each player places their mark on a 3x3 grid with the goal of having three consecutive marks in either the horizontal, vertical or diagonal direction. The game can end in three possible states of either winning, losing or drawing. We have constructed a hardware implementation of this popular game with the facility to play against either another player or the 8085 itself. We take user input using a re-purposed numeric keypad and instead of placing a mark, an LED of a specific colour is lit instead, representing either O or X. The state of

the game has been displayed using a 3x3 grid of bi-colour LEDs and a 16x2 character LCD is present to provide textual information about the game status. The block diagram representation of the proposed model is shown in Figure 1.

#### 1.3 Flow Chart of Operation

The detailed flowchart for the user-interface is given in Figure 2.

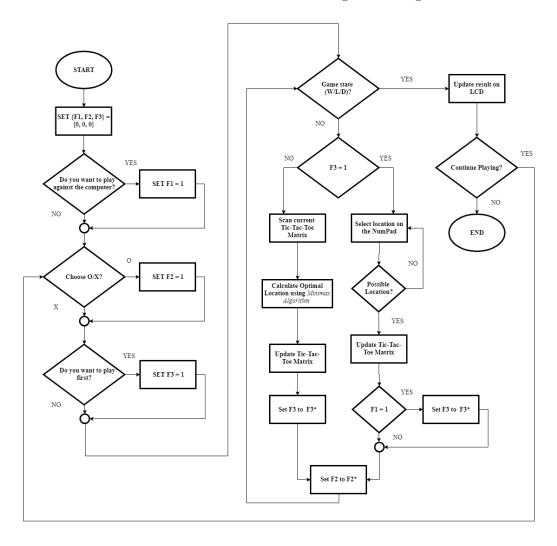


Figure 2: Flow Chart

- 2 Details of Hardware Implementation
- 2.1 Circuit Description

# 2.2 Schematic

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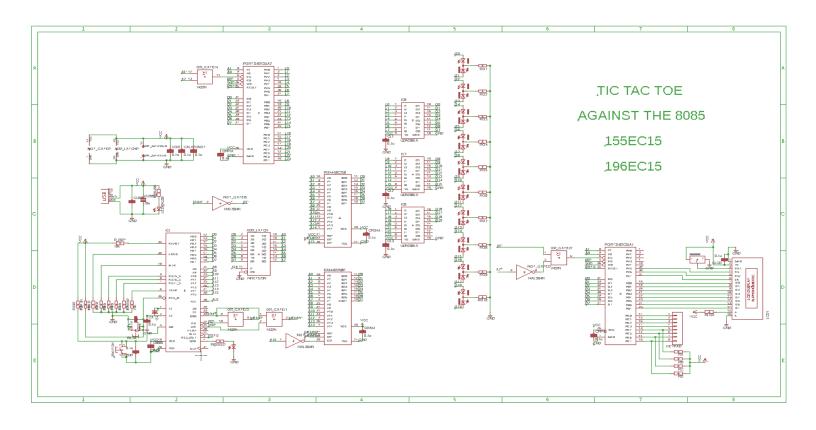


Figure 3: Schematic

Figure 4: Board Layout

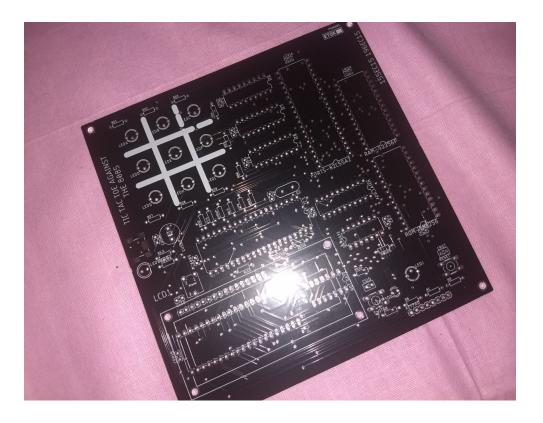


Figure 5: Printed Circuit Board

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### 2.5 Fabricated Board



Figure 6: Fabricated Board

### 2.6 Bill of Materials

Part	Value	Description
$ADD_LATCH$	74HCT573N	8-bit D latch BUS DRIVER
C8085	0.1u	CAPACITOR
CALAT	0.1u	CAPACITOR
CL1	0.1u	CAPACITOR
CL2	0.1u	CAPACITOR
CL3	0.1u 0.1u	CAPACITOR
CLCD	0.1u	CAPACITOR
CNOT	0.1u	CAPACITOR
COR	0.1u	CAPACITOR
CPPIA	0.1u 0.1u	CAPACITOR
CPPIB	0.1u 0.1u	CAPACITOR
CRAM	0.1u 0.1u	CAPACITOR
CROM	0.1u 0.1u	CAPACITOR
CRST	0.1u 0.1u	C2.5-3
CSID	0.1u 0.1u	C2.5-3
CUSBC	0.14	CAPACITOR
CUSBP	10u	5
CX	0.1u	CAPACITOR
HOLD	10k	RESISTOR
IC1	IOK	MICROCOMPUTER/PERIPHERAL DEVICE
IC6	UDN2981A	DRIVER ARRAY
IC7	UDN2981A	DRIVER ARRAY
IC8	UDN2981A	DRIVER ARRAY
INTR	10k	RESISTOR
KEYPAD	IOK	Header 8
LCD1		ALPHANUMERIC-LCD
LED@SOD		LED
LED@USB	LED5MM	ппр
LEDA	TLUV5300	Bicolor LED 5 mm Untinted Diffused Package
LEDB	TLUV5300	Bicolor LED 5 mm Untinted Diffused Package
LEDC	TLUV5300	Bicolor LED 5 mm Untinted Diffused Package
LEDD	TLUV5300	Bicolor LED 5 mm Untinted Diffused Package
LEDE	TLUV5300	Bicolor LED 5 mm Untinted Diffused Package
LEDF	TLUV5300	Bicolor LED 5 mm Untinted Diffused Package
LEDG	TLUV5300	Bicolor LED 5 mm Untinted Diffused Package
LEDH	TLUV5300	Bicolor LED 5 mm Untinted Diffused Package
LEDI	TLUV5300	Bicolor LED 5 mm Untinted Diffused Package
LEDJ	TLUV5300	Bicolor LED 5 mm Untinted Diffused Package
	TTO 1 0000	Diction and a min change and acrease

	$ NOT_GATE $ $OR_GATE$ $PORTS-82C55A1$ $PORTS-82C55A2$ $Q2$	74ALS04N 7432N	Hex INVERTER Quad 2-input OR gate MICROCOMPUTER/PERIPHERAL DEVICE MICROCOMPUTER/PERIPHERAL DEVICE Crystals
	R5.5	10k	RESISTOR
	R6.5	10k	RESISTOR
	R7.5	10k	RESISTOR
	R@SOD	-	RESISTOR
	R@USB		RESISTOR
	RA		RESISTOR
	RAM-62256P		MEMORY
	RB		RESISTOR
	RC		RESISTOR
	RD		RESISTOR
	RESET		OMRON SWITCH
	RLCD		RESISTOR
	RO1		RESISTOR
	RO2		RESISTOR
	RO3		RESISTOR
	RO4		RESISTOR
	RO5		RESISTOR
	RO6		RESISTOR
	RO7		RESISTOR
	RO8		RESISTOR
	RO9		RESISTOR
	RO10		RESISTOR
	ROM-58C256		MEMORY
	RSID	10k	RESISTOR
	RSTIN	10k	RESISTOR
	RTRAP	10k	RESISTOR
	$R_R DY$	10k	RESISTOR
	SWITCH		OMRON SWITCH
	U2	$PRESET_LR$	
_	X1	USBSMD	USB Connectors
	Table 1: My caption		

- 3 Details of Software Implementation
- 3.1 Understanding Minimax Algorithm

#### 3.2 Code Description

To implement tic-tac-toe, we have maintained a 3x3 board in RAM BOARD which provides various functions with the current state of the game. The game proceeds by alternatively calling functions corresponding to each player or a player and the AI depending on the mode selected. This process goes on until a terminal state is achieved, a terminal state being either victory or getting tied. Various menus have been constructed by using simple keypad input which uses polling to get user input. The LCD has been used to display various strings stored in the ROM depending on the situation. Two more sub-boards exist in RAM TBOARD, BMAP which store a transformed version of the main board state. These sub-boards have been used to update the LED matrix with the current state of the game. Finally, the AI component of our project has been implemented using the Minimax algorithm. The AI functions determine the most optimal move under the given situation recursively and update the state of the internal board. AIMOVE is the overall function which mimics a MAX function to determine the move to play and actually modifies the board. The MAX function iterates over empty positions and calls the MIN function for each position and similarly the MIN function iterates over the empty positions and calls the MAX function for each position. Internally, the AI is always represented as 01H while the player is represented as 0FEH. The head of both MAX and MIN functions contain a terminal state checker and information is moved between these functions using the accumulator. If a terminal state hasnt been achieved MAX iterates over empty spots placing 01H and calls MIN to evaluate the result. MAX picks the place which gives the best result for 01H. MIN works in a similar manner but looks for the case which gives the best result for 0FEH. As soon as an optimal position is detected by either MIN or MAX it immediately exits returning the value.

# 3.3 Code Layout

# 3.4 Assembly Code

CALL BLINKSOD
;—REDUNDANCY—;
MAINCODE: LXI SP,0FFFFH
CALL BLINKSOD
CALL BLINKSOD
MVIA,80H
OUT 03H
OUT 03H
MVI A,88H
OUT 83H
OUT 83H
CALL LCDINIT
CALL INIT_RAM
LXI H,STRING1
CALL LCDSTRINGDISP
CALL BLINKSODX5
LXI H,STRING11
CALL LCDSTRINGDISP
LXI H, STRING8
CALL LCDL2
PLOOP1: CALL KEYIN
CPI 0AH
JZ AIGAME
CPI 0BH
JZ PLAYERGAME

		JMP PLOOP1	PLAY1:	DCR B
	AIGAME:	LXI H, STRING9		MVI M,01H
	_	CALL LCDSTRINGDISP	PLAY2:	,
		LXI H, STRING10		CALL CWIN
		CALL LCDL2		CPI 01H
		CALL UPDATE2		JZ DUMMYPLAYERWIN
		MVI B,09H		CPI 0FEH
	COLOURM	ENULOOP: LXI H, COLOURFLAG		JZ DUMMYAIWIN
		CALL KEYIN	INVP:	LXI H, STRING3
		CPI 0AH		CALL LCDSTRINGDISP
		JNZ CSKIP1		CALL PLAYERMOVE
		MVI M,00H		MOV A, C
		JMP CSKIP2		CPI 0AAH
17	CSKIP1:	CPI 0BH		JZ INVP
		JNZ COLOURMENULOOP		CALL UPDATE2
		MVI M,01H		DCR B
	CSKIP2:	LXI H, STRING5		JZ DUMMYDRAW
		CALL LCDSTRINGDISP		CALL CFULL
		LXI H,STRING8		CPI 00H
		CALL LCDL2		JZ DUMMYDRAW
		LXI H,BOARD		CALL AIMOVE
	MENULOO	P:CALL KEYIN		CALL UPDATE2
		CPI 0BH		CALL CWIN
		JZ PLAY1		CPI 01H
		CPI 0AH		JZ DUMMYAIWIN
		JZ PLAY2		CPI 0FEH
		JNZ MENULOOP		JZ DUMMYPLAYERWIN

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(	$\mathbf{x}$

	;DRAW BLOCK:	DCR L
	CALL CFULL	JNZ AGAINPLAYER
	CPI 00H	POP H
	JZ DUMMYDRAW	JMP MAINCODE
	DCR B	DUMMYAIWIN:PUSH H
	JZ DUMMYDRAW	LXI H, STRING6
	JMP PLAY2	CALL LCDSTRINGDISP
	ENDOG: HLT	POP H
	DUMMYPLAYERWIN: PUSH H	PUSH H
	LXI H, STRING4	MVI L, 03H
	CALL LCDSTRINGDISP	CALL SETWPOS
	POP H	AGAINAI: CALL MODWIN
	PUSH H	CALL UPDATE2
×	MVI L, 03H	CALL DELAY100MS
	CALL SETWPOS	CALL DELAY100MS
	AGAINPLAYER: CALL MODWIN	CALL DELAY100MS
	CALL UPDATE2	CALL DELAY100MS
	CALL DELAY100MS	CALL CMODWIN
	CALL DELAY100MS	CALL UPDATE2
	CALL DELAY100MS	CALL DELAY100MS
	CALL DELAY100MS	CALL DELAY100MS
	CALL CMODWIN	CALL DELAY100MS
	CALL UPDATE2	CALL DELAY100MS
	CALL DELAY100MS	DCR L
	CALL DELAY100MS	JNZ AGAINAI
	CALL DELAY100MS	РОР Н
	CALL DELAY100MS	JMP MAINCODE

	,	
	AGAINDRAW: MVI A, 0AAH	LXI D,TBOARD
	OUT 00H	MOV A, C
	OUT 01H	CPI 01H
	OUT 02H	JZ INVERTBOARD
	CALL DELAY100MS	;COPY BOARD:
	CALL DELAY100MS	MVI B,09H
	CALL DELAY100MS	LOOPTXBOARD1:
19	CALL DELAY100MS	MOV A, M
	MVI A,055H	XCHG
	OUT 00H	MOV M, A
	OUT 01H	INX H
	OUT 02H	XCHG
	CALL DELAY100MS	INX H
	CALL DELAY100MS	DCR B
	CALL DELAY100MS	JNZ LOOPTXBOARD1
	CALL DELAY100MS	POP D
	DCR L	POP B

PUSH H

PUSH B

PUSH D

MOV C,M

POP H

RET INVERTBOARD:MOV A,M

POP PSW

LXI H,BOARD

LXI H, COLOURFLAG

DUMMYDRAW: PUSH H

POP H

PUSH H

MVI L, 03H

JNZ AGAINDRAW

JMP MAINCODE

POP H

TXBOARD: PUSH PSW

LXI H, STRING7

CALL LCDSTRINGDISP

	XCHG	MVI B, 09H
	CPI 0FEH	BAGAIN2:MOV A, M
	JNZ STX1	XCHG
	MVI M, 01H	CPI 0FEH
	JMP ILEND	JNZ NOTFE2
	STX1: CPI 01H	MVIA,02H
	JNZ STX2	NOTFE2: MOV M, A
	MVI M, 0FEH	INX H
	JMP ILEND	INX D
	STX2:MVI M,00H	XCHG
	ILEND: INX H	DCR B
	XCHG	JNZ BAGAIN2
	INX H	LXI H, BMAP
20	DCR B	MOV A, M
	JNZ INVERTBOARD	RRC
	POP D	RRC
	POP B	INX H
	POP H	MOV B,M
	POP PSW	ORA B
	RET	RRC
	UPDATE2: PUSH PSW	RRC
	PUSH H	INX H
	PUSH B	MOV B, M
	PUSH D	ORA B
	CALL TXBOARD	RRC
	LXI H,TBOARD	RRC
	LXI D,BMAP	INX H

	MOV B, M	RLC
	ORA B	INX H
	RRC	MOV A, M
	RRC	OUT 02H
	OUT 00H	POP D
	INX H	POP B
	MOV A, M	POP H
	RRC	POP PSW
	RRC	RET
	INX H	;——DELAY FUNCTIONS———
	MOV B, M	DELAY10MS: PUSH B
	ORA B	MVI C,09H
	RRC	D_L1: MVI B,0FFH
21	RRC	$D_LL2:$ $DCRB$
	INX H	$ m JNZ \ D\_L2$
	MOV B, M	DCR C
	ORA B	JNZ D_L1
	RRC	POP B
	RRC	RET
	INX H	DELAY100MS: PUSH B
	MOV B, M	MVI C,0AH
	ORA B	D100_L1:CALL DELAY10MS
	RRC	DCR C
	RRC	$JNZ D100_L1$
	OUT 01H	POP B
	MVI A, 02H	RET
	RLC	DELAY30MS: PUSH B

	MVI C,03H	BLINKSOD:
	D30_L1: CALL DELAY10MS	CALL SETSOD
	DCR C	CALL DELAY100MS
	JNZ D30_L1	CALL DELAY100MS
	POP B	CALL RESETSOD
	RET	CALL DELAY100MS
		CALL DELAY100MS
	DELAY1S: PUSH B	$\operatorname{RET}$
	MVI C,0AH	BLINKSODX5:
	D1S_L1: CALL DELAY100MS	CALL BLINKSOD
	DCR C	CALL BLINKSOD
	JNZ D1S_L1	CALL BLINKSOD
	POP B	CALL BLINKSOD
22	RET	CALL BLINKSOD
	;——MISC FUNCTIONS————	RET
	SETSOD:	BLINKSODX3:
	PUSH PSW	CALL BLINKSOD
	MVI A, 0C0H	CALL BLINKSOD
	$\operatorname{SIM}$	CALL BLINKSOD
	POP PSW	RET
	RET	;
	RESETSOD:	;KEYPAD FUNCTIONS-
	PUSH PSW	KEYIN: ;ACCUMULATOR RETURNS VALUE
	MVI A,040H	PUSH B
	SIM	MVI A,088H
	POP PSW	OUT 83H
	RET	CALL DELAY10MS

	OUT 83H	IN 82H
	;;PULSING SEQUENCE	ANI 0F0H;MASK
	KEYREP: ;; CALL BLINKSOD	CALL KCHECKP4
	CALL DELAY100MS	CPI 10H
	MVI A,00001110B	JNZ KEYFOUND
	OUT 82H	JZ KEYREP
	IN 82H	KEYFOUND: POP B
	ANI 0F0H;MASK	RET
	CALL KCHECKP1	KCHECKP1: ; A HAS INPUT SEQUENCE 4 BIT
	CPI 10H	CPI 11100000B
	JNZ KEYFOUND	$JNZ KS1_{-}1$
	MVI A,00001101B	MVIA,00H
	OUT 82H	RET
23	IN 82H	KS1_1: CPI 11010000B
	ANI 0F0H;MASK	$JNZ KS1_2$
	CALL KCHECKP2	MVIA,01H
	CPI 10H	RET
	JNZ KEYFOUND	KS1 <sub>-</sub> 2: CPI 10110000B
	MVI A,00001011B	$JNZ KS1_3$
	OUT 82H	MVIA,02H
	IN 82H	RET
	ANI 0F0H; MASK	KS1_3:CPI 01110000B
	CALL KCHECKP3	$ m JNZ\ KS1\_4$
	CPI 10H	MVIA,0AH
	JNZ KEYFOUND	RET
	MVI A,00000111B	$KS1_{-4}:MVIA,10H$
	OUT 82H	RET

		JNZ $KS3_2$
	KCHECKP2:; A HAS INPUT SEQUENCE 4 BIT	MVIA,07H
	CPI 11100000B	RET
	JNZ KS2_1	KS3_2:CPI 10110000B
	MVI A,03H	JNZ KS3_3
	RET	MVIA,08H
	KS2_1:CPI 11010000B	RET
	$JNZ KS2_2$	KS3_3:CPI 01110000B
	MVIA,04H	$JNZ KS3_4$
	RET	MVI A, 0CH
	KS2_2:CPI 10110000B	RET
	$JNZ KS2_3$	KS3_4:MVI A,10H
	MVIA,05H	RET
24	RET	
	KS2_3:CPI 01110000B	KCHECKP4: CPI 11100000B
	$JNZ KS2_4$	$JNZ KS4_1$
	MVIA,0BH	MVIA, 0EH
	RET	RET
	KS2_4:MVI A,10H	KS4_1:CPI 11010000B
	RET	$JNZ KS4_2$
		MVIA,09H
	KCHECKP3:; A HAS INPUT SEQUENCE 4 BIT	RET
	CPI 11100000B	KS4_2:CPI 10110000B
	$JNZ KS3_{-}1$	JNZ $KS4_{-}3$
	MVIA,06H	MVIA,0FH
	RET	RET
	KS3_1:CPI 11010000B	KS4_3:CPI 01110000B

RET
DELAY2: PUSH B
MVI B,0FFH
AG2:MVI C,0FFH
AG1:DCR C
JNZ AG1
DCR B
JNZ AG2
POP B
RET
LCDINIT: ; LCD INITIALISER
PUSH PSW
MVIA,38H
CALL CMD
MVIA,38H
CALL CMD
CALL DELAY
MVI A,01H
CALL CMD
MVIA,01H
CALL CMD
CALL DELAY2
MVI A,0CH
CALL CMD
MVIA,80H
CALL CMD

		POP PSW		PUSH B
		RET		PUSH D
	LCDSTRI	NGDISP: PUSH H		PUSH H
		CALL LCDINIT		LXI H, STRING2
	PRINT:M	IOV A,M		CALL LCDSTRINGDISP
		INX H		CALL DELAY100MS
		CPI 00H		LXI H,BOARD
		JZ STREND		MVI D,0FFH
		CALL DATA		MVI C,09H
		JMP PRINT	AILOOP:	MOV A, M
	LCD2:	MVI A,0C0H		CPI 00H
		CALL CMD		JNZ INVM
		RET		MVI M,01H
26	LCDL2:	PUSH H		CALL MIN
		CALL LCD2		CPI 01H
	PRINT2:	MOV A,M		JZ EXITA
		INX H		;NON WINNING CASES
		CPI 00H		CMP D
		JZ STREND		JNC SKAI
		CALL DATA		MOV D, A
		JMP PRINT2		MOV E,C
			SKAI:MV	И М,00Н
	STREND:	POP H	INVM: IN	XН
		RET		DCR C
	;AIMOVE	):		JNZ AILOOP
	AIMOVE:	CALL BLINKSOD		LXI H,BOARD
		PUSH PSW		MVI D,00H
				•

		MVI A,09H		CALL MAX
		SUB E		CPI 0FEH
		MOV E, A		JZ XITFE
		DAD D		CMP D
		MVI M, 01H		JNC MINSKP
	EXITA:	POP H		MOV D,A
		POP D		MVI M,00H
		POP B	MININV:	
		POP PSW		DCR C
		RET		JNZ MINL
	MIN: PUS	Н Н		MOV A,D
		PUSH B		JMP EXITM
		PUSH D	XITFE:	MVI M,00H
27		LXI H,BOARD	EXITM:	POP D
		CALL CWIN		POP B
		CPI 00H		POP H
		JNZ EXITM		RET
		CALL CFULL	MAX: PUS	н н
		CPI 00H		PUSH B
		JZ EXITM		PUSH D
		LXI H,BOARD		LXI H,BOARD
		MVI D,02H		CALL CWIN
		MVI C,09H		CPI 00H
	MINL:	MOV A,M		JNZ EXITMX
		CPI 00H		CALL CFULL
		JNZ MININV		CPI 00H
		MVI M, 0 FEH		JZ EXITMX
		11111 1111 01 1111		OZ ZZINIL

	MAXL:	LXI H,BOARD MVI D,0FFH MVI C,09H MOV A,M CPI 00H JNZ MAXINV MVI M,01H CALL MIN	EX2:MOV	MVI C,09H A,M CPI 00H JZ EX1 INX H DCR C JNZ EX2 POP H
		CPI 01H		MVI A,00H
		JZ XIT01		RET
		CMP D	EX1:POP	
		JNC MAXSKP		MVI A,01H
64	3.5433077	MOV D, A	OT I TO I	RET
28		MVI M,00H	CWIN:	PUSH D
	MAXINV:			LXI D, WINLIST
		DCR C		PUSH H
		JNZ MAXL		LXI H,BOARD
		;NON 01 CASES:		LXI B, 0A000H; POINTER
		MOV A,D		MVI A,08H
	VID01	JMP EXITMX		DCX D
	XIT01:	MVI M,00H	OT OOD I	PUSH B
	EXITMX:		CLOOP: I	PUSH PSW
		POP B		XRA A INX D
		POP H RET		
	CEIIII.			PUSH H
	CFULL:	PUSH H		MVI B,00H XCHG
		LXI H,BOARD		ACIG

	DIED D	101 B
	ADD M	MVIA,00H
	XCHG	RET
	INX H	WINO:
	MOV C, M	POP PSW
	XCHG	POP B
	DAD B	POP H
	ADD M	POP D
	XCHG	MVIA, 0FEH
	INX H	RET
	MOV C, M	WINX:
29	XCHG	POP PSW
	DAD B	POP B
	ADD M	POP H
	POP H ; RESTORING HL	POP D
	CPI 0FAH	MVIA,01H
	JZ WINO	RET
	CPI 03H	; CONVERSION TABLE:
	JZ WINX	WINLIST:.DB 00H,01H,01H
	POP PSW ; RESTORING A	.DB 03H,01H,01H
	DCR A	.DB 06H,01H,01H
	POP B	.DB 00H,03H,03H
	STAX B	.DB 01H,03H,03H
	DIJOIL D	DD 0011 0

MOV C,M

PUSH B

JNZ CLOOP

XCHG DAD B POP B

POP H

POP D

.DB 02H,03H,03H

.DB 00H, 04H, 04H

	.DB 0FEH .DB 00H,0 BMAP:.EQU 8100H .DB 00H,00H,0 .DB 00H,00H,0	0H 1,00H,0FEH 1,001H,001H 0FEH,001H	TBCLRL:	JNZ BCLRL MVI B,09H LXI H,TBOARD MVI M,00H INX H DCR B JNZ TBCLRL LXI H,WINPOS MVI M,00H
30	.DB 00H,00H,0 TBOARD: .EQU 8400 COLOURFLAG .EQU WINPOS: .EQU 8310 MCOUNTER .EQU 83	0Н 8300Н 0Н		INX H MVI M,00H INX H MVI M,00H POP H
J	INIT_RAM:PUSH B PUSH H		DI AVEDIA	POP B RET
	MVI B,090 LXI H,BM RCLRL:MVI M,00H INX H DCR B JNZ RCLR MVI B,090 LXI H,BO BCLRL:MVI M,00H INX H	IAP L H	PLAYERM	PUSH PSW LXI H,BOARD MVI C,00H CALL KEYIN ;0-8 VALUE MAPPED ;REJECTING OTHER KEYPAD INPUTS: CPI 09H JNC INVALID CALL CHECKCORRECT CPI 0AAH
	DCR B			JZ INVALID

	ADD L		POP B	
	MOV L,	A	РОР Н	
	MVI M, (	FEH ;X=01H ASSUMED	RET	
	PUSH B		PLAYERMOVE2:	
	LXI H,I	BOARD	PUSH PSW	
	CALL CWIN POP B		LXI H,BOARD	
			MVIC,00H	
	POP PSV	V	CALL KEYIN	
	RET		CPI 09H	
	INVALID: MVI C	, 0AAH	JNC INVALID1	
	POP PS	SW .	CALL CHECKCORRECT1	
	RET		CPI 0AAH	
	CHECKCORRECT:	PUSH H	JZ INVALID1	
31		PUSH B	ADD L	
		LXI H, BOARD	MOV L, A	
		MOV B, A	MVI M,01H ; P2=01H ASSUMED	)
		MOV A, L	PUSH B	
		ADD B	LXI H,BOARD	
		MOV L, A	CALL CWIN	
		MOV A, M	POP B	
		CPI 00H	POP PSW	
		JZ OK	RET	
		MVI A,0AAH	INVALID1: MVI C,0AAH	
		POP B	POP PSW	
		POP H	RET	
		RET	CHECKCORRECT1: PUSH H	
	OK:	MOV A, B	PUSH B	

	LXI H, BOARD	JNZ XCOLOURMENULOOP	
	MOV B, A	MVIM,01H	
	MOV A, L	XCSKIP2:CALL UPDATE2	
	ADD B	CALL CWIN	
	MOV L, A	CPI 01H	
	MOV A, M	JZ DUMMYPLAYER2WIN	
	CPI 00H	CPI 0FEH	
	JZ OK1	JZ DUMMYPLAYER1WIN	;EDIT TO P2
	MVI A, 0AAH	INVP1:LXI H,STRING13	
	POP B	CALL LCDSTRINGDISP	
	POP H	CALL PLAYERMOVE	
	RET	MOV A, C	
	OK1:MOV A,B	CPI 0AAH	
32	POP B	JZ INVP1	
	POP H	CALL UPDATE2	
	RET	CALL CWIN	
	PLAYERGAME: LXI H, STRING12	CPI 01H	
	CALL LCDSTRINGDISP	JZ DUMMYPLAYER2WIN	
	LXI H, STRING10	CPI 0FEH	
	CALL LCDL2	JZ DUMMYPLAYER1WIN	;EDIT TO P2
	XCOLOURMENULOOP: LXI H, COLOURFLAG	CALL CFULL	
	CALL KEYIN	CPI 00H	
	CPI 0AH	JZ DUMMYDRAW	
	JNZ XCSKIP1	INVP2:LXI H,STRING15	
	MVI M,00H	CALL LCDSTRINGDISP	
	JMP XCSKIP2	CALL PLAYERMOVE2	
	XCSKIP1: CPI 0BH	MOV A, C	

	CPI 0AAH	DAD B
	JZ INVP2	ADD M
	CALL UPDATE2	XCHG
	CALL CWIN	INX H
	CPI 01H	MOV C,M
	JZ DUMMYPLAYER2WIN	XCHG
	CPI 0FEH	DAD B
	JZ DUMMYPLAYERIWIN	ADD M
	CALL CFULL	XCHG
	CPI 00H	INX H
	JZ DUMMYDRAW	MOV C,M
	JMP XCSKIP2	XCHG
	SETWPOS:	DAD B
33	PUSH D	ADD M
	LXI D, WINLIST	POP H ; RESTORING HL
	PUSH H	CPI 0FAH
	LXI H,BOARD	JZ WINO1
	MVI A,08H	CPI 03H
	DCX D	JZ WINX1
	MLOOP1: PUSH PSW	POP PSW ; RESTORING A
	XRA A	DCR A
	INX D	JNZ MLOOP1
	PUSH H	POP H
	MVI B,00H	POP D
	XCHG	MVI A, 00H
	MOV C,M	;EMSG:
	XCHG	LXI H, ERRORMSG

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ADD I	A CONT. T. A
ADD L	MOV L,A
MOV L,A	MOV M, B
MVIM,00H	XCHG
XCHG	INX H
;WP	MOV A, M
INX H	XCHG
MOV A,M	ADD L
XCHG	MOV L, A
ADD L	MOV M, B
MOV L, A	CALL UPDATE2
MVI M,00H	CALL BLINKSOD
CALL UPDATE2	CALL DELAY100MS
CALL BLINKSOD	POP B
CALL DELAY100MS	POP D
; SETTING WINNING COMBO TO B:	POP H
LXI H, WINPOS	RET
LXI D,BOARD	DUMMYPLAYER1WIN: PUSH H
MOV A,M	LXI H, STRING14
XCHG	CALL LCDSTRINGDISP
ADD L	POP H
MOV L, A	PUSH H
MOV M, B	MVIL, 05H
XCHG	CALL SETWPOS
INX H	AGAINPLAYER1: CALL BLINKRCD
MOV A,M	DCR L
XCHG	JNZ AGAINPLAYER1
ADD L	POP H

JMP MAINCODE CALL LCDSTRINGDISP POP H DUMMYPLAYER2WIN: PUSH H PUSH H LXI H, STRING16 CALL LCDSTRINGDISP MVI L, 05H POP H CALL SETWPOS PUSH H AGAINAI: CALL BLINKRCD MVI L, 05H DCR L CALL SETWPOS JNZ AGAINAI POP H AGAINPLAYER2: CALL BLINKRCD DCR L JMP MAINCODE JNZ AGAINPLAYER2 POP H DUMMYDRAW: PUSH H JMP MAINCODE LXI H, STRING7 DUMMYPLAYERWIN: PUSH H CALL LCDSTRINGDISP LXI H, STRING4 POP H CALL LCDSTRINGDISP PUSH H POP H MVI L, 03H PUSH H AGAINDRAW: MVI A, 0AAH OUT 00H MVI L, 05H CALL SETWPOS OUT 01H AGAINPLAYER: CALL BLINKRCD OUT 02H DCR L CALL DELAY100MS JNZ AGAINPLAYER CALL DELAY100MS POP H CALL DELAY100MS JMP MAINCODE CALL DELAY100MS DUMMYAIWIN: PUSH H MVI A,055H LXI H, STRING6 OUT 00H

	OUT 01H		STRING2:	.DB "AI MOVE",00H		
	OUT 02H		STRING3:	.DB "Player Move",00H		
	CALL DEI	LAY100MS	STRING4:	.DB "Player Wins!",00H		
	CALL DEI	LAY100MS	STRING6:	DB "AI Wins!",00H		
	CALL DEI	LAY100MS	STRING7:	.DB "It 's a Draw!",00H		
	CALL DEI	LAY100MS	STRING11:	.DB "Play Vs. AI?",00H		
	DCR L		STRING12:	.DB "Player1 is:",00H		
	JNZ AGAI	NDRAW	STRING13:	.DB "Player1's Turn:",00H		
	POP H		STRING14:	.DB "Player1 Wins!",00H		
	JMP MAIN	ICODE .	STRING15:	.DB "Player2's Turn:",00H		
; List of strings used:			STRING16:	.DB "Player2 Wins!",00H		
37	STRING5:	.DB "Play First?",00H	STRING17:	.DB "MICROPROCESSOR",00H		
	STRING8:	.DB "A) Yes B) No",00H	STRING18:	.DB "PROJECT BY:",00H		
	STRING9:	.DB "Play as:",00H	STRING19:	.DB " $155/EC/15$ ",00H		
	STRING10:	.DB "A) Green B) Red",00H	STRING20:	.DB "196/EC/15",00H		
	STRING1:	.DB "Tic-Tac-Toe",00H	ERRORMSG:	.DB "ERROR!",00H		

### 4 Gantt Chart Revisited

The project duration was 16 weeks, starting from January 1, 2018 till May 23, 2018. The planned and actual project implementation routine is given below. Moreover, the Gantt Chart initially proposed is shown in the following figure.

Table 2: Actual v/s Proposed Schedule

Task	Start Date	End Date	Duration	Actual Start Date	Actual End Date
Project Proposal	05-Jan	15-Jan	10	05-Jan	15-Jan
C Code Prototype	12-Jan	14-Jan	2	12-Jan	14-Jan
Basics of 8085 & Assembly Language	02-Jan	01-Apr	89	02-Jan	20-Mar
Analysing Hardware Requirements	01-Feb	$07 ext{-} ext{Feb}$	6	01-Feb	07-Feb
Schematic Development	07-Feb	24-Feb	17	07-Feb	16-Mar
Constructing the Board Layout	24-Feb	14-Mar	18	16-Mar	29-Mar
Ordering and Obtaining the PCB	15-Mar	29-Mar	14	29-Mar	07-Apr
Board Fabrication	30-Mar	04-Apr	5	08-Apr	12-Apr
SoftwareDevelopment(1): Basic Tic-Tac-Toe Model	15-Mar	01-Apr	17	12-Mar	05-Apr
SoftwareDevelopment(2): Constructing the Minmax Algorithm Model	01-Apr	15-Apr	14	17-Mar	22-Mar
Conducting Alpha Tests	15-Apr	25-Apr	10	12-Apr	25-Apr
Preparing Documentation	01-Apr	25-Apr	24	25-Apr	30-Apr
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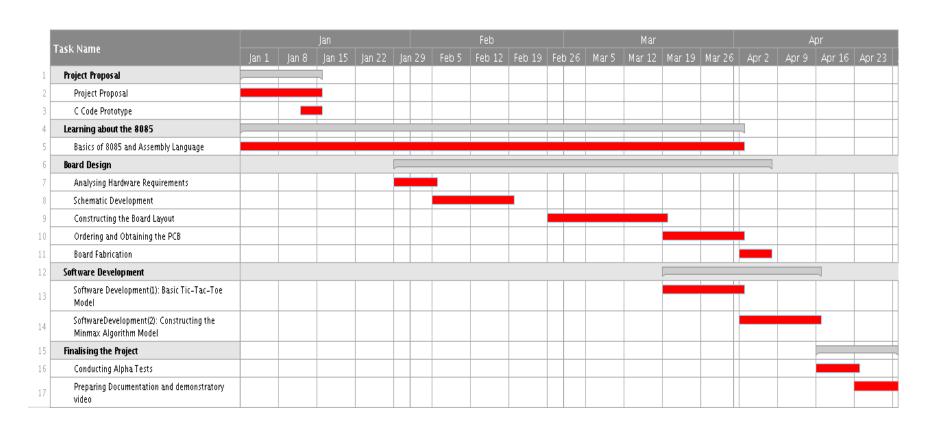


Figure 7: Proposed Gantt Chart

# 5 Summary

#### References

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