AMERICAN INTERNATIONAL UNIVERSITY – BANGLADESH (AIUB)
Where leaders are created

Implementation of 4 bit Arithmetic Logic Unit

Course Teacher: Richard Victor Biswas
Lecturer
Department of Electrical and Electronic Engineering

Presented By,
Shilamoni Shaha Neir
20-43640-2

Outline of the Presentation

- Objectives (1 slide, several lines, numbered) << What are purposes of this work?
- Introduction (2-3 slides) << Background, motivation, and What has been done.
- Research/Working Method (1-2 slides) << What are the working principles?
- Description of the Work (2-3 slides) << How has the work done? Circuit/Block Diagram.
- Results and Discussions (in the form of Tables/Graphs/Plots/Images/Photos/ Figures in 2-6 slides) << What is your present outcome? Discuss each result/outcome.
- Conclusions (1-2 slides) << What is your summary?
- Future Works (1 slide) << What do you want to do next? Or How someone can carry further research on it?

Objectives of the Work

- To Develop and functionally validate a fully operational 4-bit Arithmetic Logic Unit (ALU).
- To Analyze and explain the implemented ALU's architectural design and operational principles.
- To design and construct dedicated test benches.
- Evaluate the implemented ALU and compare it to alternative technologies.
- To test the movement of data and control signals through the ALU during different operations.

Introduction

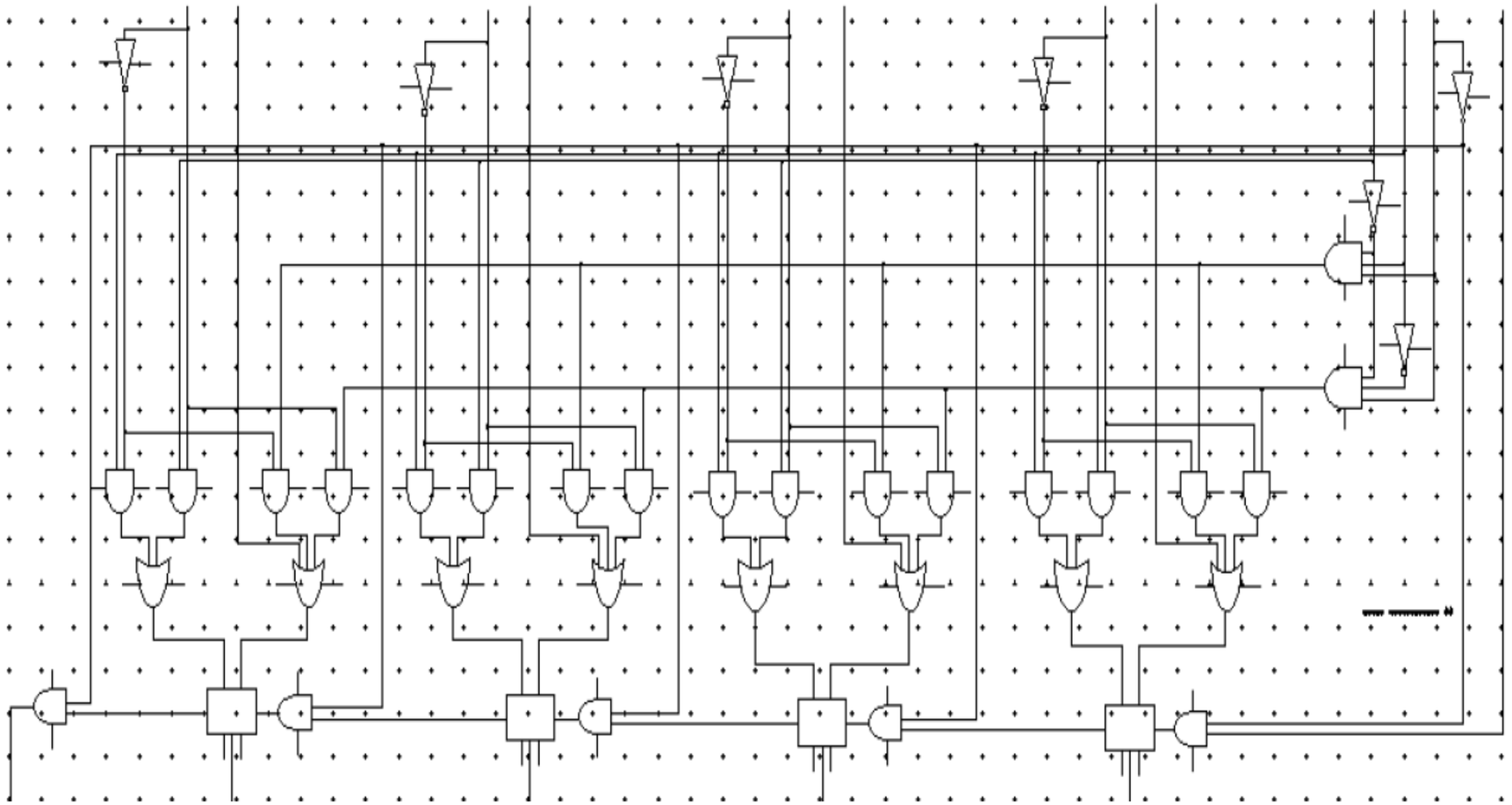
- Motivitaion of doing this project:The Arithmetic logic unit (ALU) which considered an essential component in many applications such as Microprocessor, digital signal processing, image processing, etc.
- It is a new concept of comparing the technologies to implement 4 Bit ALU.
- In previous papers we did not found the trade off with Transmission gate.
- In other papers we saw they have used Multiplexer but we did not use any multiplexer in our implementation .

Introduction…

Works has done in previous papers From the literature review:

1. In the majority of designs, there exists a trade-off between power, delay and area
2. To improve the performance and power dissipation of a chip, a paper present an Arithmetic and Logic Unit (ALU) using the "Power performance tunable Pseudo-Dynamic topology".
3. Delay Optimization of 4-Bit ALU Designed in FS-GDI Technique
4. Low Power 4-Bit Arithmetic Logic Unit Using
5. Full-Swing GDI Technique

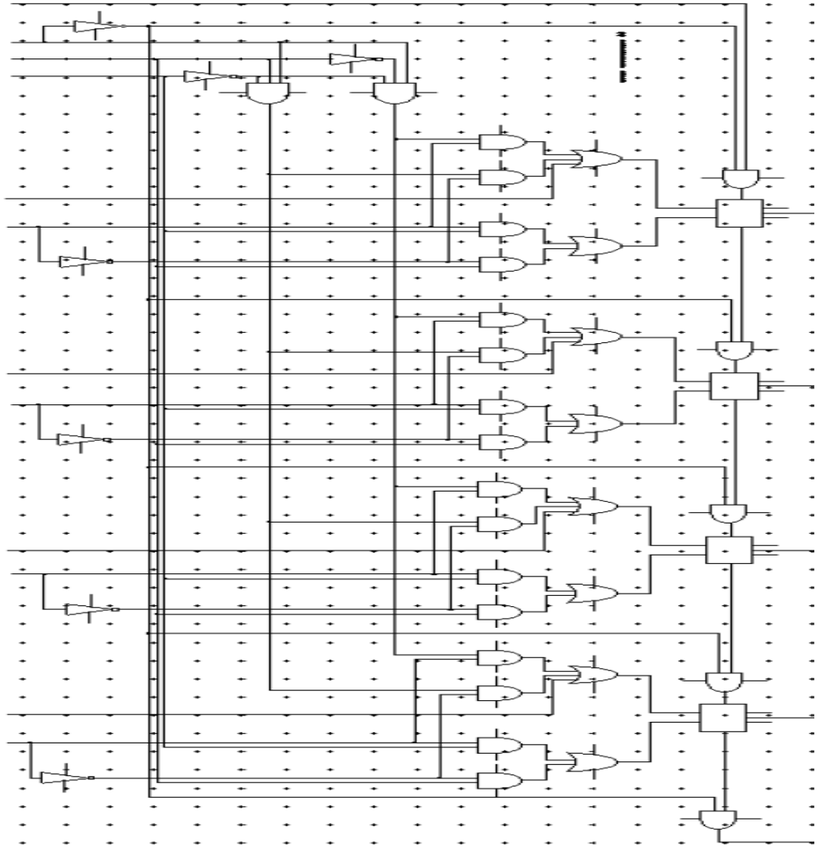
Working Method



4-bit ALU diagram

Working Method…

- 4-Bit ALU Operation:
- The 4-bit ALU takes four pairs of binary inputs: (a1, b1), (a2, b2), (a3, b3), and (a4, b4). It utilizes four full adders and produces four outputs (s1, s2, s3, s4) and a final carry-out (cout).



Working Method…

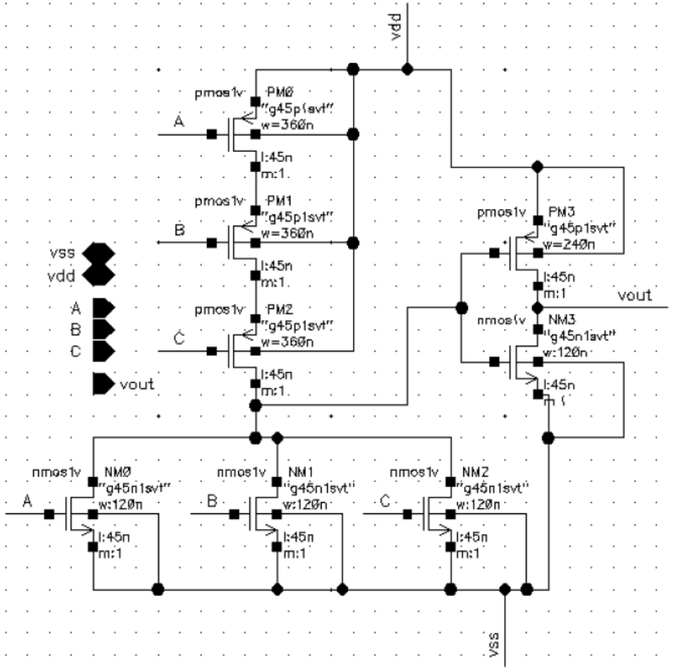
Internal Processing:

Full Adders: Each pair of inputs (a, b) enters a full adder along with a carry-in (cin) from the previous stage (except cin=0 for the first adder). The adder outputs the corresponding sum (s) and carry-out (cout).

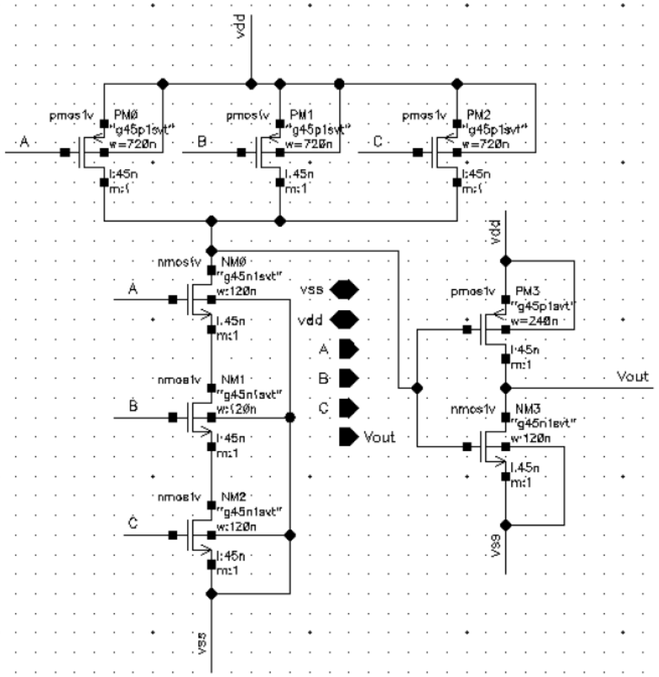
Selection Logic: A control signal, S0, determines whether the carry-out from each full adder participates in the next stage. If S0 is low, the carry-out is ignored, and the operation becomes purely logical. Otherwise, the carry-out acts as a carry-in for the next adder, enabling arithmetic operations.

AND Gates: Two 3-input OR gates and four 2-input OR gates process the signals based on the selection lines S0, S1, and S2. These gates combine the sum outputs (s) and selected carry-out signals (cout) to generate the final ALU outputs (s1, s2, s3, s4).

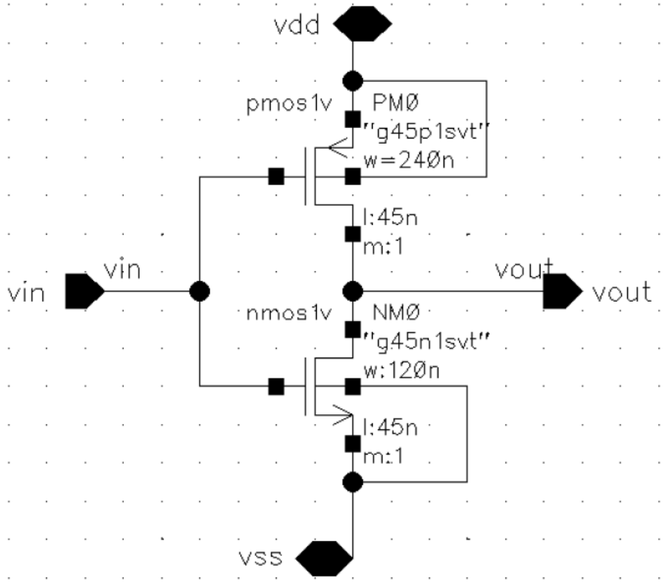
Description of the Work



3 bit or

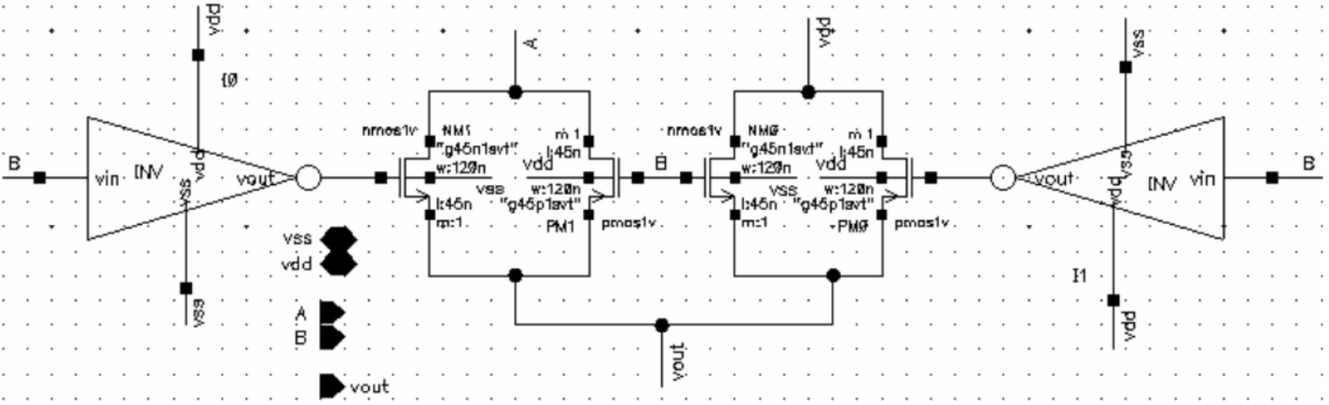


3 bit and

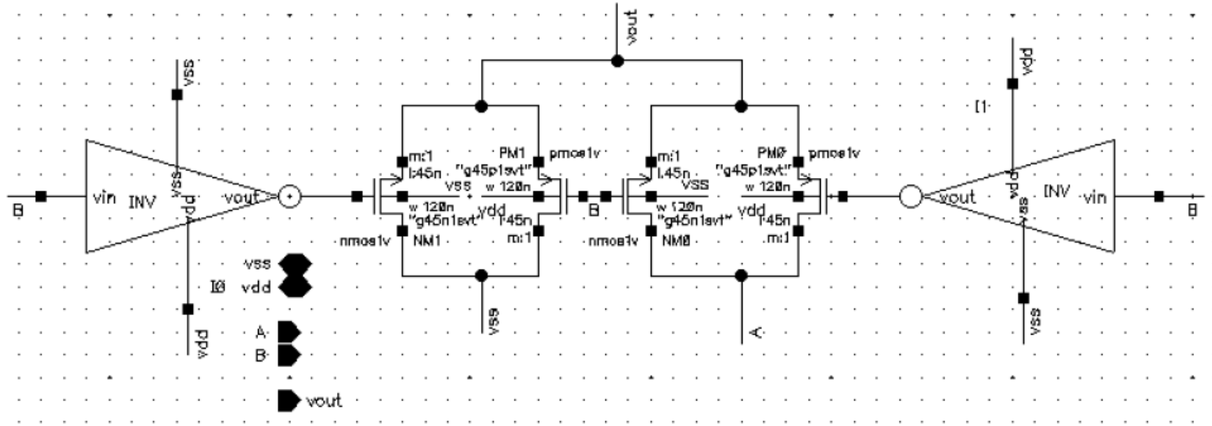


Inverter

Description of the Work…

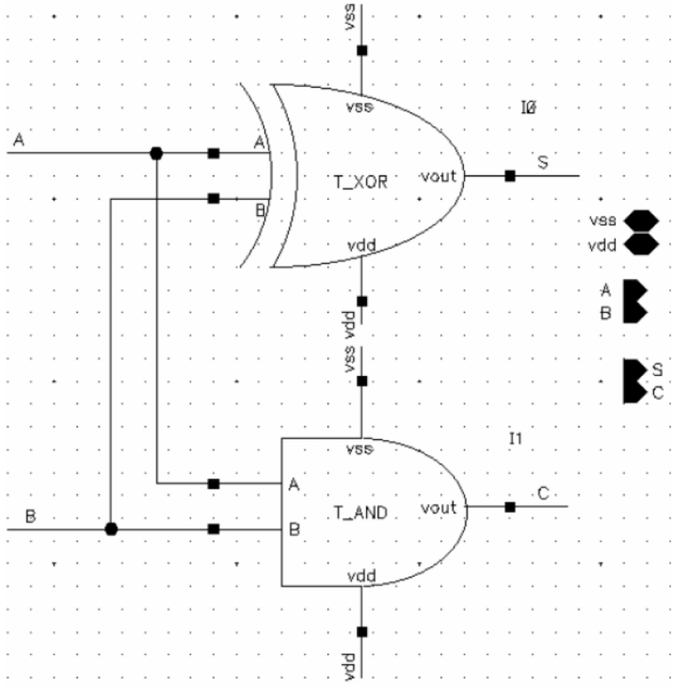


Transmission And

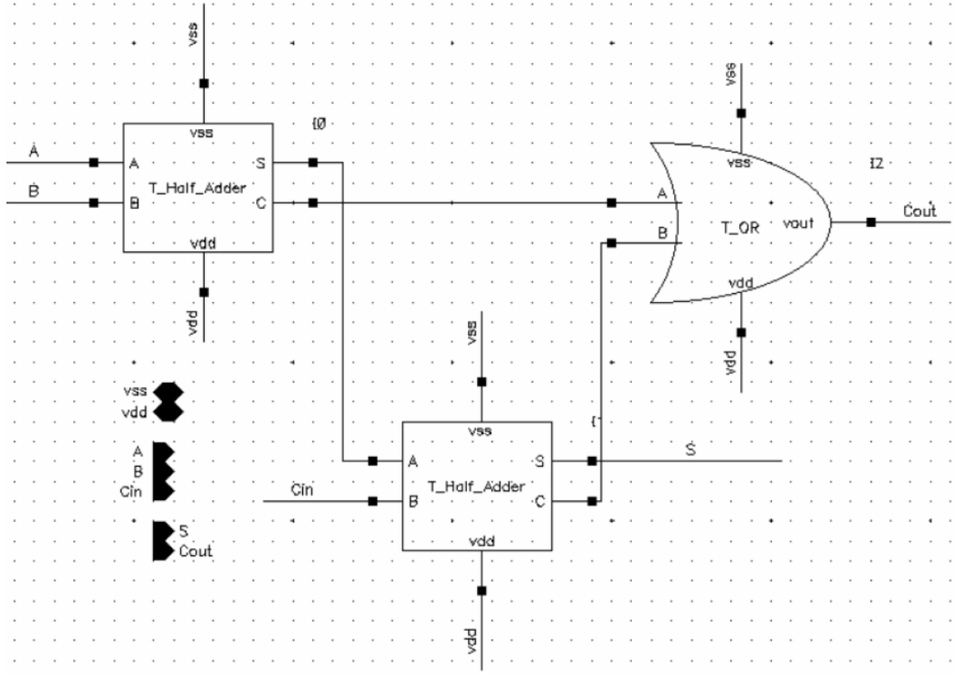


Transmission or

Description of the Work…



Transmission Half adder



Transmission full adder

Results and Discussions

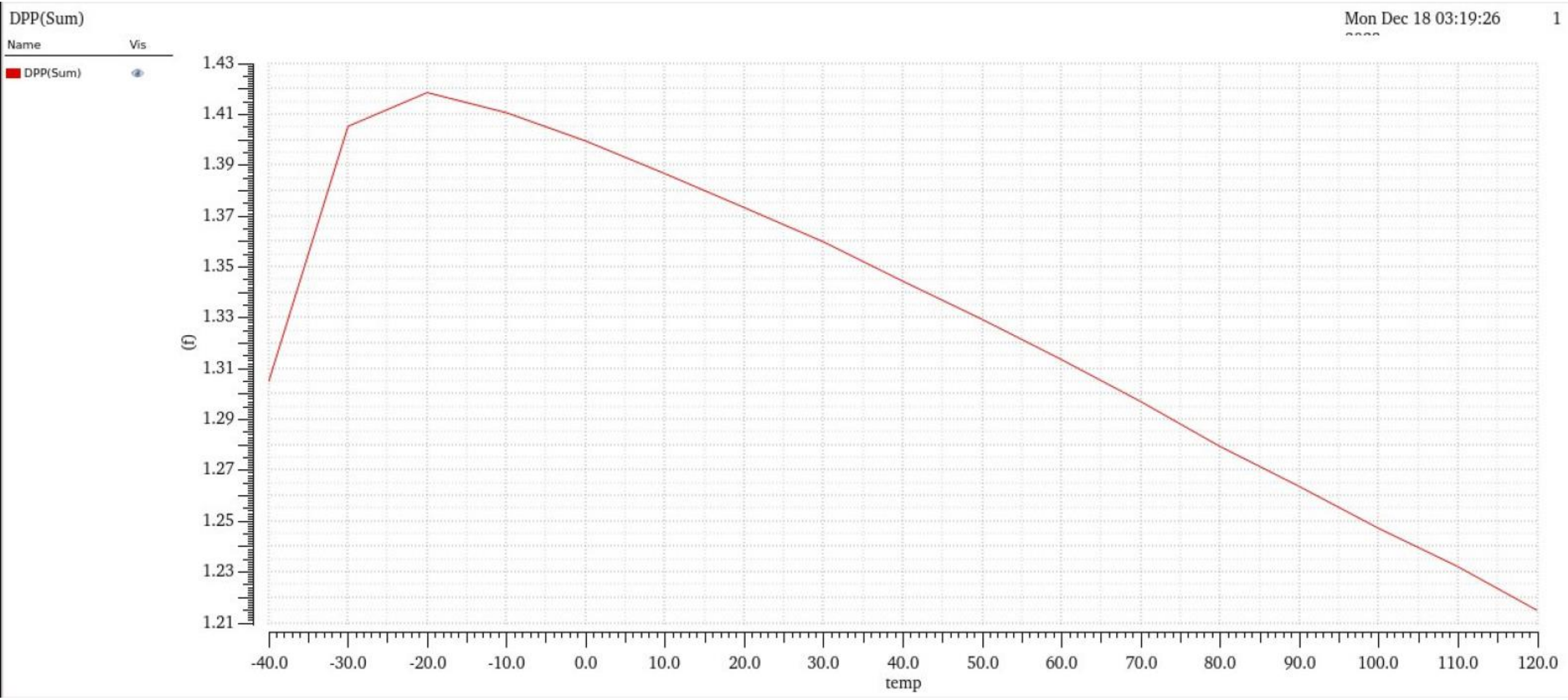
Technology	Cmos				
Output	S1	S2	S3	S4	C_{out}
Skew	342.979G	342.962G	342.962G	342.962G	334.46G
Propagation	67.6548p	67.6549p	67.6549p	67.6549p	40.011n
Static power	194.278n	168.542n	86.3476n	86.6481n	96.6353n
Fall time	3.73201p	3.73219p	3.73219p	3.73219p	2.12643p
Rise time	3.73201p	3.73219p	3.73219p	3.73219p	2.12643p
Delay Power Product	1.314*10^-17	1.14*10^-17	5.841*10^-18	5.862*10^-18	3.8664*10^-15
Fan IN	12	12	12	12	12
Frequency	62.9029M	63.9317M	50.8164M	50.8132M	26.7817M

Technology	Pseudo				
Output	S1	S2	S3	S4	C_{out}
Skew	247.559G	247.586G	247.586G	248.722G	235.378G
Propagation	62.9747p	62.982p	62.982p	63.1955p	40.0096n
Static power	389.73u	389.648u	390.054u	390.053u	389.765u
Fall time	5.17048p	5.16991p	5.16991p	5.14631p	3.50496p
Rise time	5.17048p	5.16991p	5.16991u	5.14631p	3.50496p
Delay Power Product	2.45*10^-14	2.454*10^-14	2.456*10^-14	2.464*10^-14	1.56*10^-11
Fan IN	12	12	12	12	12
Frequency	62.902M	38.3334M	50.8149M	50.811M	26.782M

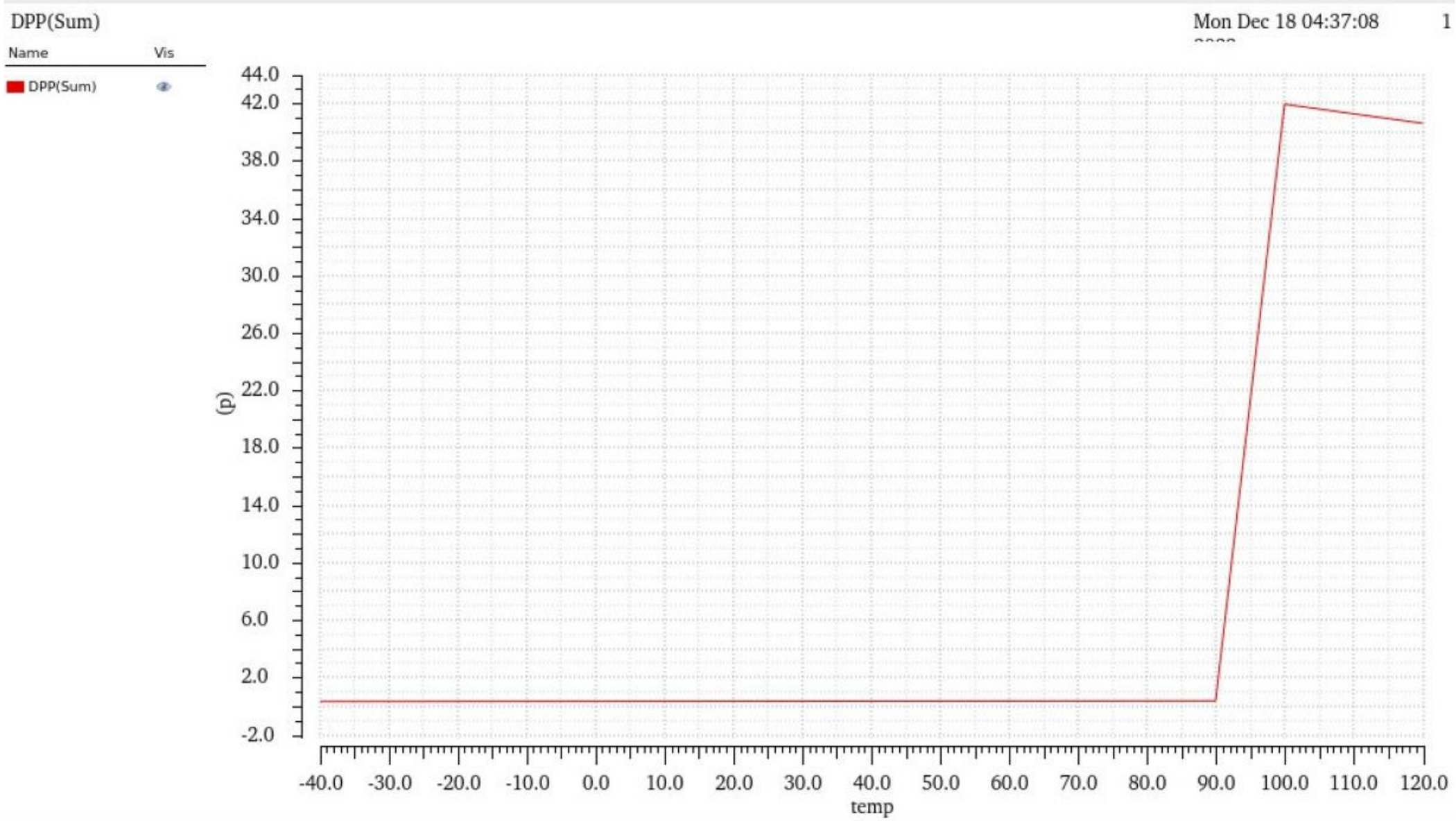
Technology	Dynamic				
Output	S1	S2	S3	S4	C_{out}
Skew	448.475G	445.827G	445.827G	445.827G	396.527G
Propagation	18.0005p	18.0005p	18.0005p	18.0005p	4.99722n
Static power	2.27842m	213.5u	2.25571m	2.17535m	219.569u
Fall time	1.76626p	1.76626p	1.76626p	1.76626p	1.84281p
Rise time	1.76626p	1.76626p	1.76626p	1.76626p	1.84281p
Delay Power Product	4.101*10^-14	3.843*10^-15	4.060*10^-14	3.916*10^-14	1.097*10^-12
Fan IN	13	13	13	13	13
Frequency	163.78M	152.756M	203.15M	159.05M	131.75M

Technology	Transmission				
Output	S1	S2	S3	S4	C_{out}
Skew	141.049G	193.523G	193.524G	164.883G	1.27676G
Propagation	36.6943p	36.1983p	36.2147p	37.846p	-10.0098n
Static power	3.51854u	2.03991u	1.88836u	1.83718u	135.558u
Fall time	2.26871p	1.67725p	1.67725p	3.29012p	37.5952p
Rise time	2.26871p	1.67725p	1.67725p	3.29012p	37.5952p
Delay Power Product	129.11*10^-18	73.8411*10^-18	68.3865*10^-18	69.5298*10^-18	1.3569*10^-12
Fan IN	12	12	12	12	12
Frequency	25M	50.817M	38.981M	34.5444M	27.7789M

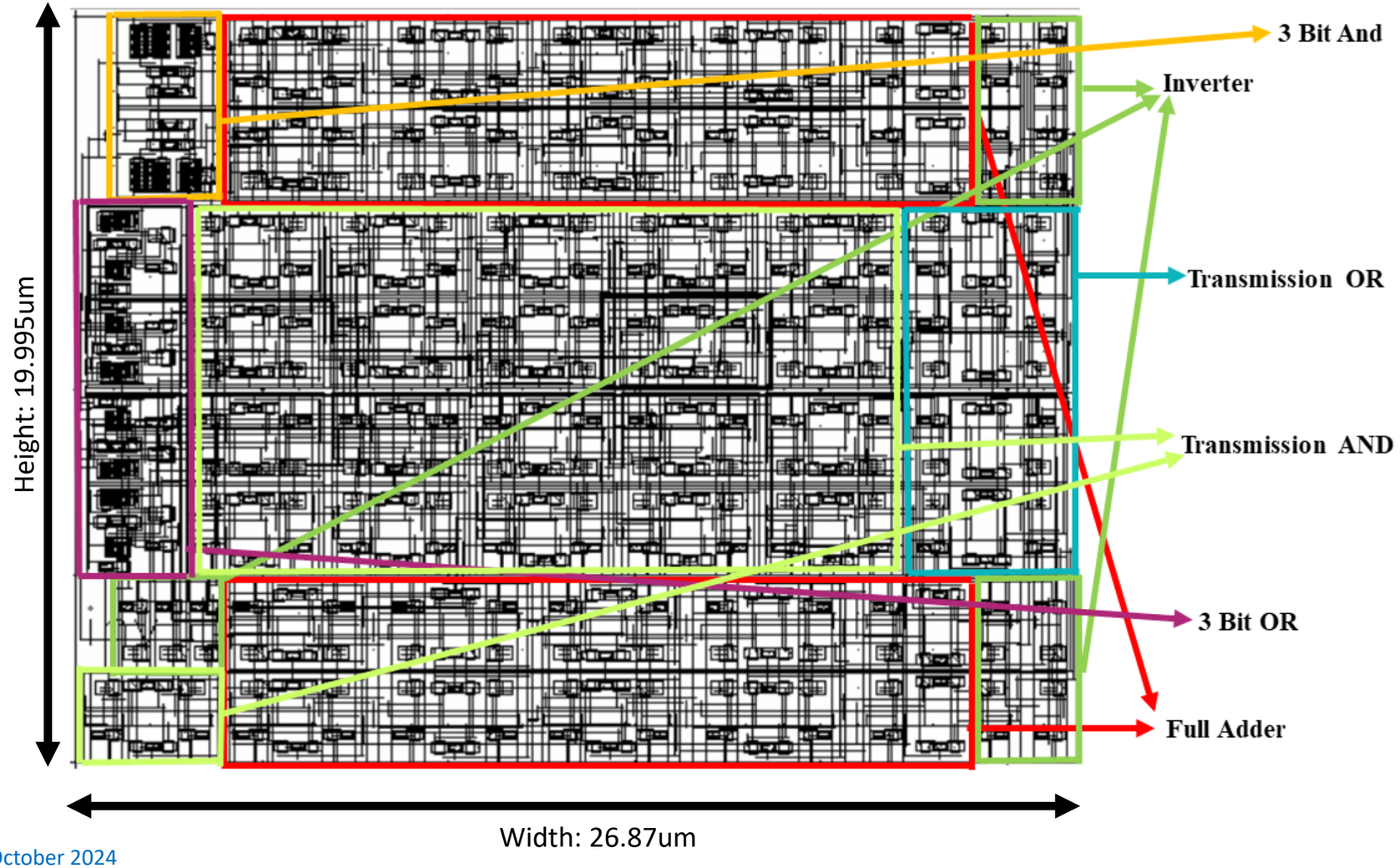
Transmission Gate



Pseudo Nmos Logic

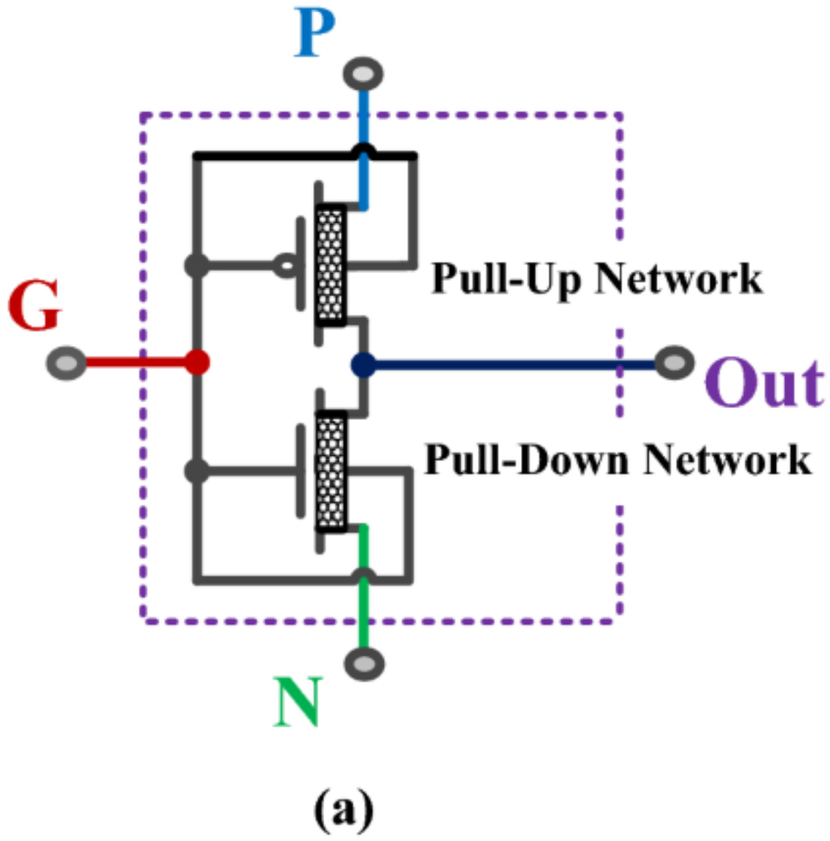


Conclusions

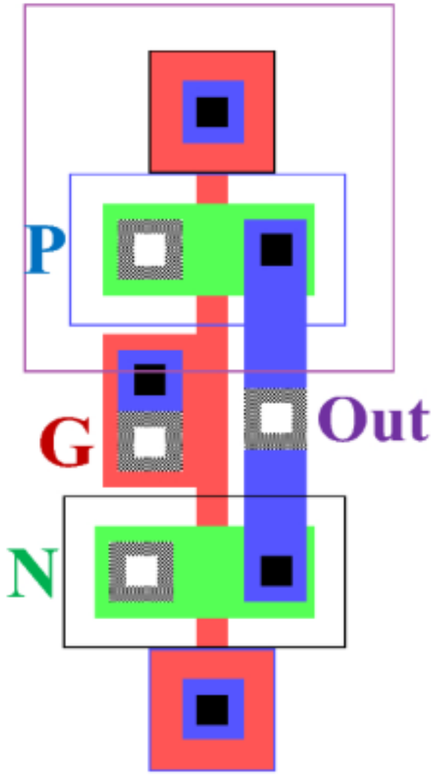


Total Area: 537.265 pm^2

Future Scopes



(a)

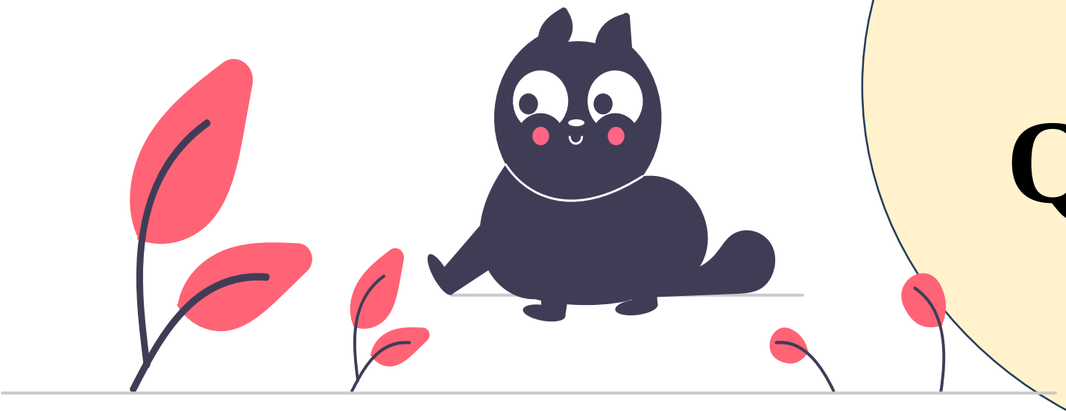


(b)

I. Reducing Power Consumption

II. Minimal Delay

III. Reducing Area



Any Questions?