TFE4141 Design of digital systems 1

Assignment 2: Understanding the Delta-delay

Task 1

- 1. Read the paper: Time and delta-delay in VHDL (found under *Learning materials* on *Blacboard*).
- 2. Explain in your own words what happens in a simulation cycle. If you want you may illustrate your explanation with a flow diagram. Keep your answer short.
- 3. Explain what happens to signals that are assigned values with and without **explicit delays**.

Task 2

Given the following two concurrent (samtidige) processes in an architecture:

```
Q <= A nor QN;
QN <= B nor Q;
```

Given the following stimuli:

```
A <= '1'; B <= '0';

wait for 10 ns;

A <= '0';

wait for 10 ns;

B <= '1';

wait for 10 ns;

B <= '0';

wait for 10 ns;

B <= '1'; A <= '1';
```

- 1. Use the type **std_ulogic** as defined on the next page. Make a timing diagram for A, B, Q, and QN. Make sure that you include all delta-cycles.
- 2. Does the simulation stop after all stimuli have been applied and the two processes Q and QN are suspended, or do you experience oscillations?
- 3. Write VHDL-code with entity and architecture that implements the processes Q and QN. Write a testbench which applies the given stimuli to this entity.

Use the type std ulogic which is defined as follows:

```
TYPE std_ulogic IS ( 'U', -- Uninitialized 'X', -- Forcing Unknown '0', -- Forcing 0 '1', -- Forcing 1 'Z', -- High Impedance 'W', -- Weak Unknown 'L', -- Weak 0 'H', -- Weak 1 '--', -- Don't care );
```

Note: To make this type available you must include the following in you code:

```
library ieee;
use ieee.std_logic_1164.all;
```

These code lines must be written above the entity and architecture declaration. When a simulation starts, a signal not given a specific initialization value, will be assigned the first value in the list, in this case 'U' – (Uninitialized). Later on the signal value will typically change into 'X', '1' or '0'.