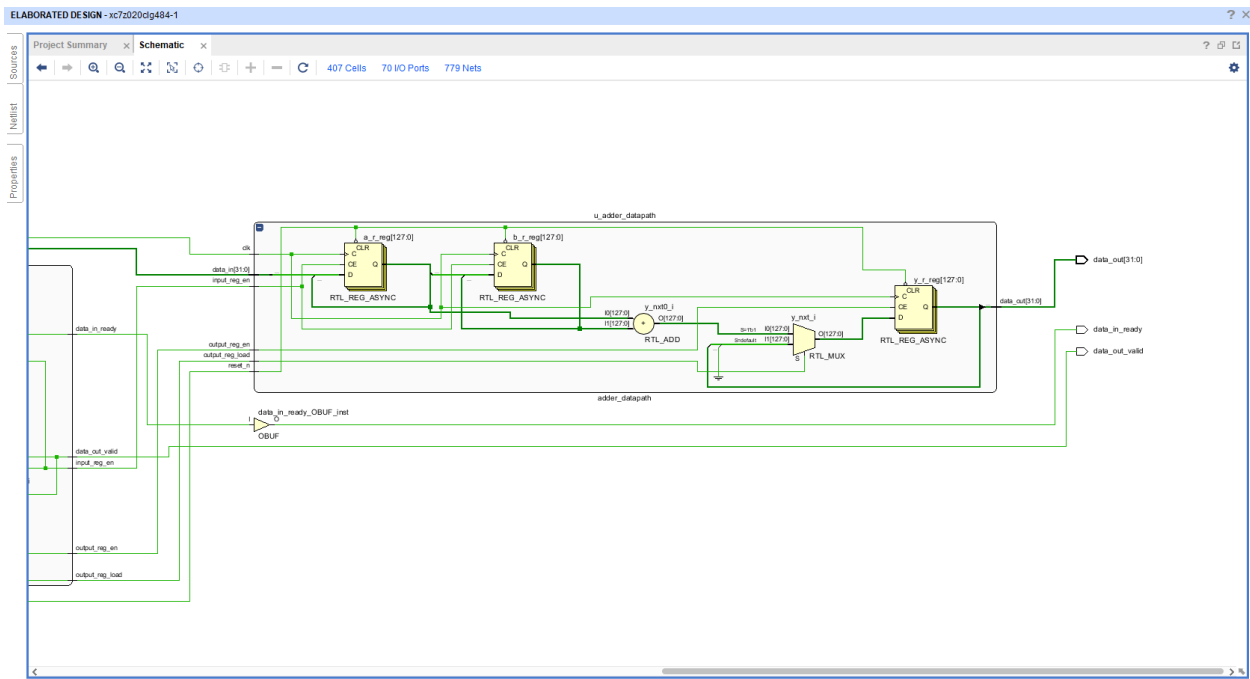


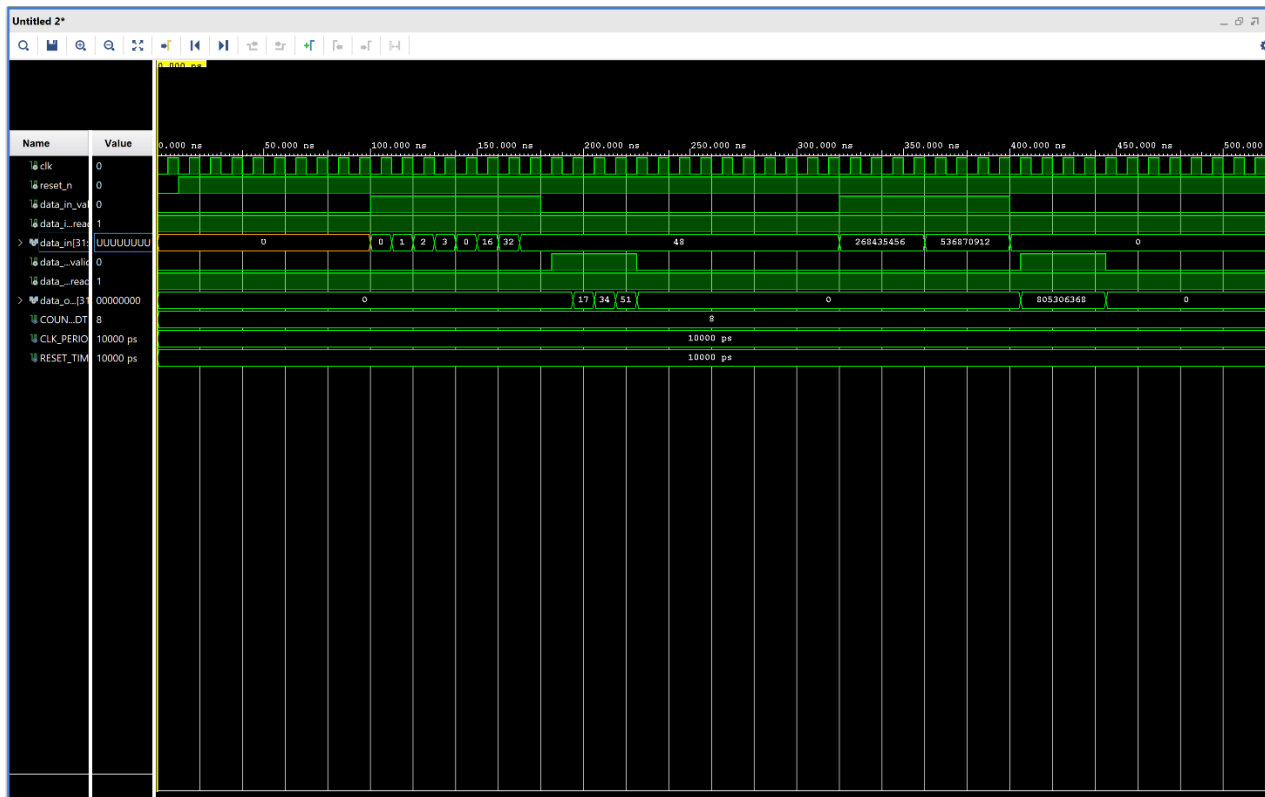
Task 1

The microarchitecture for the data path of the design is as follows:



Task 2

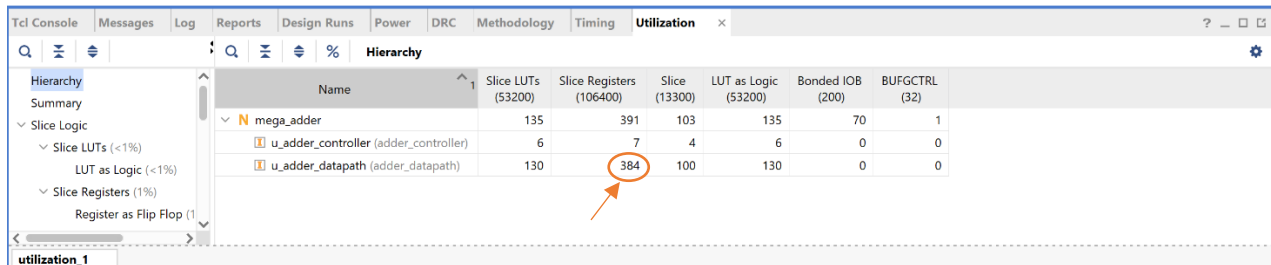
If we run the testbench, we can see that the simulation result is as follows:



Task 3

Both A and B are 128-bit numbers. Therefore, each of them needs 128 flip-flops to be written. Moreover, Y as a result of the add of A and B, is 128 bit and therefore we need another 128 flip-flops to write the result of the adder. Hence, we need 384 flip-flops in total.

If we run the synthesis, we can see that the number of flip-flops in the Datapath is 384 (according to the below picture). Therefore, we have counted the number of flip-flops correctly.

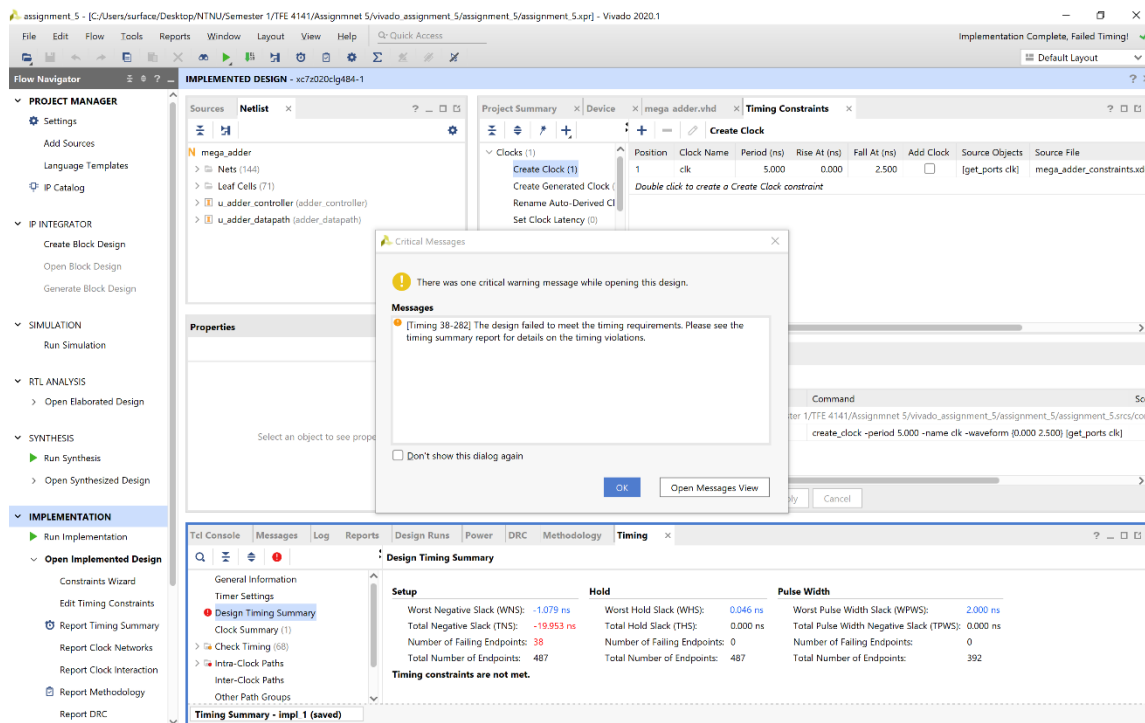


The screenshot shows the 'Utilization' tab in the Vivado IDE. The 'Hierarchy' pane on the left shows the design structure. The main table lists the utilization for various components. The 'u_adder_datapath' component is highlighted with a red circle, showing 384 flip-flops.

Name	Slice LUTs (53200)	Slice Registers (106400)	Slice (13300)	LUT as Logic (53200)	Bonded IOB (200)	BUFCTRL (32)
mega_adder	135	391	103	135	70	1
u_adder_controller (adder_controller)	6	7	4	6	0	0
u_adder_datapath (adder_datapath)	130	384	100	130	0	0

Task 4

When the timing constrain is set to 5 ns, the negative slack will be added to that time, so the frequency is going to be $(1 / (5 + \text{negative slack})) = 166 \text{ MHz}$. The result of the Implementation is as follows:



The screenshot shows the Vivado IDE with the 'Design Timing Summary' report open. The report indicates that the design failed to meet the timing requirements. A 'Critical Messages' dialog box is also visible, stating: 'There was one critical warning message while opening this design. [Timing 38-282] The design failed to meet the timing requirements. Please see the timing summary report for details on the timing violations.'

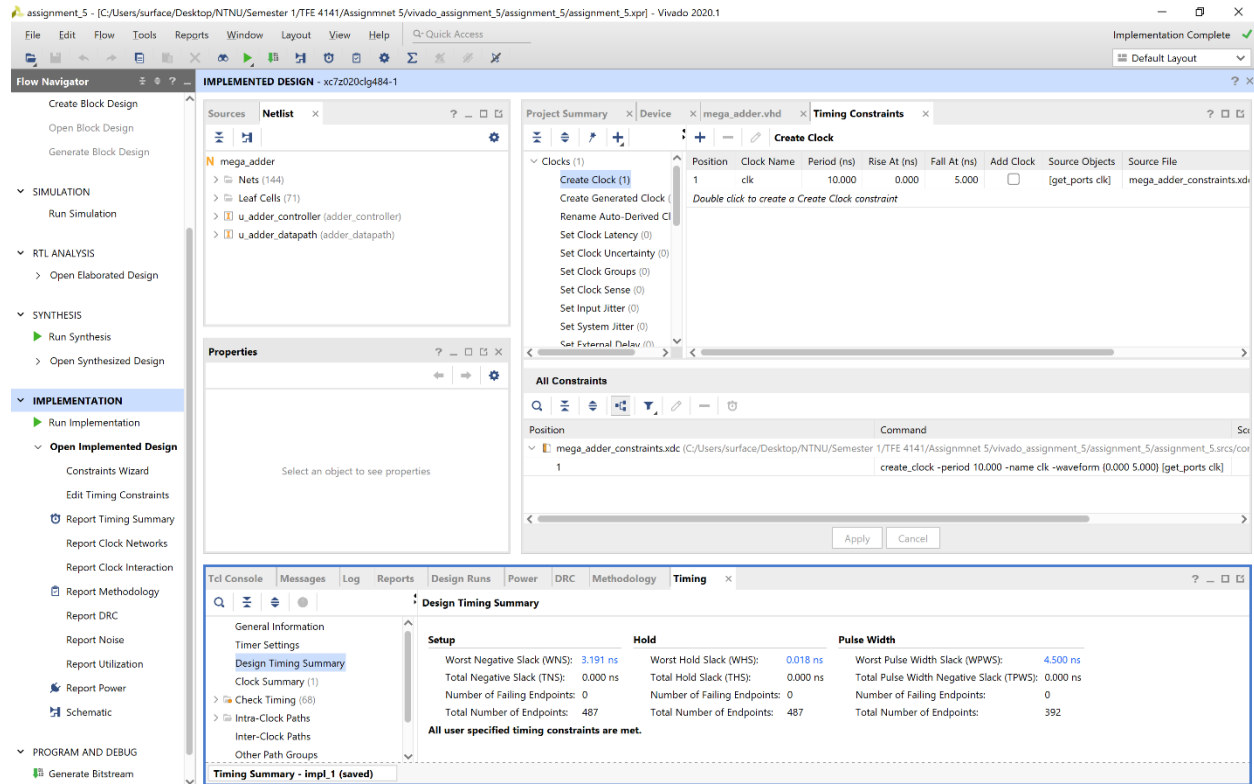
Design Timing Summary

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): -1.079 ns	Worst Hold Slack (WHS): 0.046 ns	Worst Pulse Width Slack (WPWS): 2.000 ns
Total Negative Slack (TNS): -19.953 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 38	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 487	Total Number of Endpoints: 487	Total Number of Endpoints: 392

Timing constraints are not met.

Because of the fact that the time we need for the process to be done in each cycle is more than 5ns, the synthesizer will be adopted (increased) so that it will be able to synthesize. Therefore, the operating frequency will be decreased.

To be on the safe side, we choose 10ns as the timing constrain. In that case, we will have positive slack instead of the negative one. The result of the Implementation is as follows:



Task 5

The critical path happens as we wait and shift the input data every time and after getting all the 256 bits, we finally start doing the addition operation and make the output available every 32 bits.

To improve the design, one possible solution can be starting the addition operation immediately after getting the first 32 bits of the second data (5th 32 bits of the input). This way, we can start adding the first 32 LSBs earlier and putting them on the output signal after being added and we even can use 32bit adder with carry on for that purpose. The overall look of the microarchitecture can be seen in the picture below:

