Design of a four-pixel Digital Camera

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***Abstract*-This project is introduced to give experience in the design of analog and digital circuits and give an insight into some methods used in the industry. We will focus on the design of a four-pixel digital camera. The design is divided into two parts: The analog part, which uses pixel sensors that consists of a photogate circuit, a three-stage comparator, and an 8-bit dynamic memory. In this part, the analog signal will be received and transformed into digital. The digital part, which consists of the control circuit that controls the pixel array and all the input signals of the pixel sensors. Also, the state transitions happen as a result of this digital control.**

In this project, Ng-Spice is used for analog simulations and Verilog is used for digital simulations. Test benches are designed to adjust and verify the source files and scale the design.

Index terms- Digital Pixel sensors, Digital Pixel Arrays, ADC, memory, image sensor.

I. INTRODUCTION

Digital applications are becoming more and more common in our daily lives and in many cases, replacing analog applications. However, since the world we live in is an analog world, digitalization cannot completely remove the need for analog applications. What we see today is that we are converging toward a mixture of analog and digital systems.

One example is the camera. Previously, until the introduction of the digital camera in 1975, cameras worked by exposing a chemical film to light for a user-defined period. In digital cameras, a photodiode is used to generate current. When the camera is instructed by the user to capture a photo, the diode is used to charge a capacitor. The voltage of the capacitor is amplified and read by an Analog to Digital Converter (ADC or A/D). This is done using a ramp signal and a comparator, and finally a memory to store and send the results. The internal mechanics of the camera, such as erasing, controlling the exposure time and the readout of data is controlled by a control circuit. Figure 1 shows a very simplified view of a digital camera.

Today, digital cameras dominate the market, with mechanical cameras becoming almost useless. Camera technology progresses each year with more advanced circuits and capture capabilities, as well as allowing for a more user-friendly experience than mechanical cameras. As these cameras are becoming more advanced while reproducing better images, they are still required to shrink in physical size. CMOS technology can be a solution to the challenges faced when shrinking physical size while increasing the performance.

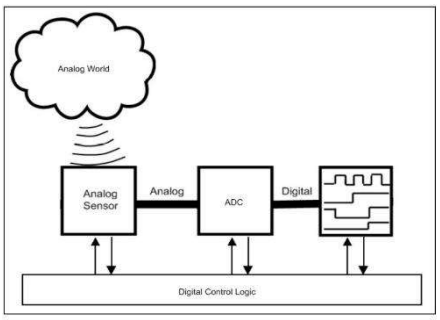

Figure 1 - very simplified view of a digital camera

In the years after the key reference [1], the approaches to design pixel sensors have changed and today, we have approaches like described in [2] that uses a sequential triple quantization (3Q) scheme that enables ultra-wide DR in a single exposure and single-pixel readout while achieving low power consumption. These features make the sensor ideally suitable for battery-powered, always-on, mobile CV applications. Furthermore, they introduce a novel 3Q scheme that enables single exposure HDR operation to quantize the signal in linear high gain mode (PD ADC) for low light pixels, in linear low gain mode (FD ADC) for medium light pixels, and in pseudo-logarithmic TTS mode for high light pixels. These three modes operate sequentially within a single exposure, and each pixel "automatically" selects its optimal mode based on its own local light level.

In this project, we design a four-pixel digital camera which can then be used for an n-pixel camera since the basic functions will be the same. In order to start the design, we first need to design the analog part.

As described before, this section consists of a sensor, a comparator and, an 8-bit memory. We use models for each specific part of the circuit since we do not have these parts in our spice simulator. In the key reference that is used in this project [1], it is fully described how the design of the pixel has been conducted. The design of the pixel sensor can be seen in figure 2.

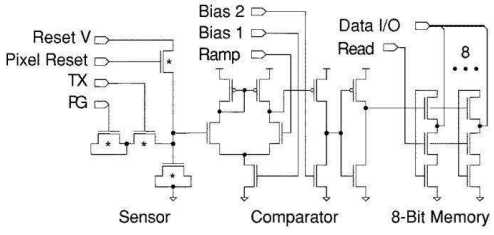

Figure 2 – Design of a pixel sensor

In the design of the analog part of this project, we used this schematic to write the source code for the pixel sensor and tested it with test benches in order to verify that this model works. After this verification, we can use this model to create the four-pixel digital camera as the goal of the project.

In order to form the pixel array, we design a control unit which is the digital part of this project. Using this control unit, we are able to select each of four pixels repeatedly. This task is done by manipulating the read signal that is gone into the pixel sensors.

The rest of the paper is organized as follows. In section II, we describe the basic theory needed in the implementation of the design of the pixel sensors. In section III, we describe how we designed our pixel sensor array and pixel array, what decisions we made in the analog design, and how we divided up the digital part of the design and how did we manage to control the pixel array. In section IV, we demonstrate the results of our designs for both analog and digital sections using the test benches and simulations. In section V, we explain what the circuit and results show. Finally, in section VI, we demonstrate next steps that could be done to improve the project.

II. THEORY

In this section, we introduce the applied theory that is needed for the implementation of the design.

A. Field-Effect Transistors

Field-Effect Transistors are a fundamental building block of modern electronics design since they are able to be produced quite small and they are by far the most used components in integrated circuit design and our design. The most common type of FETs is NMOS and PMOS. These are transistors created by silicon dioxide, where the substrate, two heavily doped regions, and a gate electrode creates the device terminals. For NMOS the substrate is of p-type and the terminals are made up of n-doped regions. The opposite is true for PMOS, n-type substrate and p-doped regions make up the terminals. This similar structure with opposite regions, makes the NMOS and PMOS complementary as the polarities are opposite of each other [3].

B. CMOS

Complementary MOS (CMOS) is a technology that uses both NMOS and PMOS transistors to create digital and analog integrated circuits. CMOS is the most widely used IC technology, as it has taken over many applications that for a long time, only were possible by bipolar devices.

As mentioned before, transistors are made up of heavily doped regions and a gate electrode. To induce a channel in a for instance PMOS transistor, a negative voltage with a higher magnitude than a threshold needs to be applied to the gate terminal. This forms a current channel between the source and drain terminal [3]. The condition can be described as:

$$|V_{gs}| \geq |V_t| \tag{1}$$

To make a current I_D flow between Drain and Source, a negative voltage V_{DS} is connected to the drain terminal [3]. The mobility of the electrons in the channel follows the following relation:

$$\mu C_{ox} \tag{2}$$

The transconductance parameter of the transistor k_p, which is proportional to the aspect ratio of the transistor:

$$k_p = \mu C_{ox} \frac{W}{L} \tag{3}$$

Finally, the current flow through the transistor can be calculated keeping in mind the different working areas of the transistors.

C. Leakage through transistors

In this project, we will assume that all voltage transients are so slow that no leakage current is present between the gate and the other ports of any of the transistors. In the same way, we assume there are no leakage currents through any of the capacitors.

As described in the previous section, the current from drain to source is proportional to the size of the transistors ($I_D \propto \frac{W}{L}$). This also makes sense from a geometric point of view. In order to minimize the leakage current through a transistor that is shut off, $\frac{W}{L}$ should be minimized. The transistors are therefore optimized with this in mind.

III. IMPLEMENTATION

In this section, we will elaborate on how we proceeded with the design of this project. We will divide the implementation into analog and digital sections.

A. Analog Design

In order to design the pixel sensor, we use the design shown in figure 2. To proceed with the design, we have to implement that figure in a source file. Therefore, we start by connecting the transistors and wiring them together.

After the circuit is done, we need to configure the sizing of the transistors. For this purpose, first, we need to figure

out the current of the current source in the model-based version of the design (e.g., we have a model instead of the actual transistor-based comparator). After figuring out the current needed to drive the circuit, we use the equation of the current through a transistor to figure out the sizing of the transistors ($I_D \propto \frac{W}{L}$)[4].

Finally, we input the correct sizing of the transistors in the source file and this way, the analog design of the pixel sensor is done.

The way the circuit works is we first store a voltage in the capacitor (this voltage is transferred to the capacitor from the photodiode via the switch) and name this voltage VSTORE. Then, we need to input VSTORE to our comparator which has the other input connected to a ramp signal. The output of the comparator is then inverted and connected to the memory to store the data there.[4]

This concludes the analog section of the design. After this, we have to use this pixel sensor, in the pixel array and control it using the digital design of the circuit.

B. Digital Design

In the digital design, first, we need to form the 4×4 pixel array from the pixel sensor. In order to do this, we need to define a selector so that we can read the data from each sensor and then go to the other one. The method used in this project is defining the READ as a 4-bit signal and assigning each of the bits to one pixel sensor. Then, when we want to select one pixel, we change the bit specified to that pixel sensor to '1' in our state machine. This way, we can read the pixels one after the other and hence, form the pixel array.

Then, we need to design a counter so that we can transfer between the states of the digital camera (ERASE -EXPOSE – CONVERT – READ - IDLE). We assume that each of the states takes some amount of time which is defined in the source file. Then, using the counter, we can easily transfer to another state when the defined time of each state is done.

IV. RESULT

In this section, we review the result of the simulations done on our designs and source files. This is done using the test benches that we have created. First, we demonstrate the results from the analog design and then, we display the results of the digital design.

A. Analog Design Results

First, we go through the results of the simulation in analog design. The first verification is that the output of the comparator works as expected. The expected result was that it should compare the VSTORE (which is the output of the analog pixel sensor) to the ramp signal and when the ramp is higher than VSTORE, it pulls the output high. This way, we convert the analog signal into digital bits so that we will be able to store them in the memory. This result is shown in Figure 3.

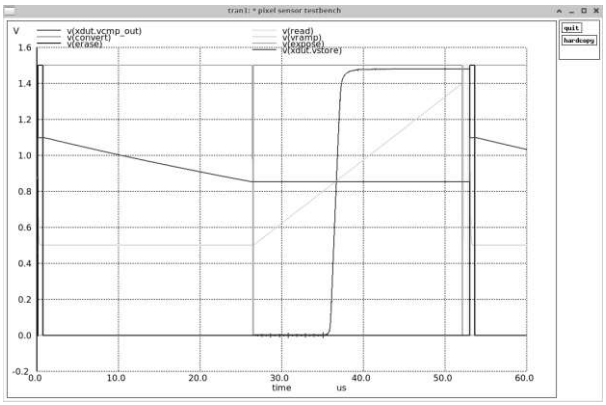

Figure 3 – Analog simulation result

In Figure 4 the output of each memory bit can be seen. This demonstrates that the conversion from pixel's analog output to digital is done correctly.

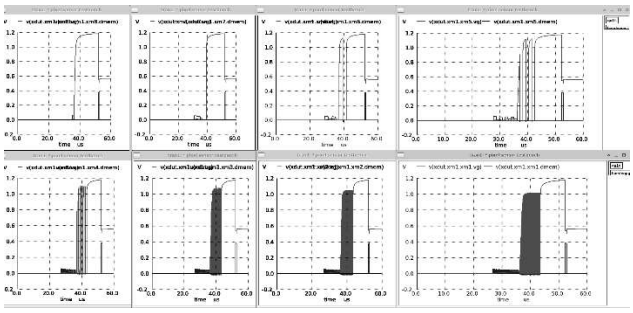

Figure 4 – 8-bit memory output

B. Digital Design Results

In this section, we verify the results of the implementation of the digital design. The first verification is checking whether the reading process is done correctly one pixel after another or not. The result for this verification is demonstrated in Figure 5. It is clear to see that first, the bit of the READ assigned to pixel number one gets high and the reading process of that pixel is done. Then, we see that the result of the reading process is sent to the pixelDataOut. After reading the first pixel, we proceed to the next pixel and change the bit assigned to that pixel to high while changing the previous pixel to low. It can be seen that the result of the second pixel reading process is stored in pixelDataOut after the data stored from the previous pixel. This process goes on until the last pixel read is done and we have all the data transferred to pixelDataOut.

Figure 5 – Read process of the pixels

After verifying that the reading process is done correctly, we need to verify that the state transition is done correctly. The result of the state transition between CONVERT state (010 defined in the Verilog file) to the READ state (011) is shown in Figure 6. It can be seen that when the counter reaches the limit defined for the duration of CONVERT, it resets, and we transfer into the READ state and the counter once again counts for the duration defined for the reading process and this is valid for every other state transition. In Figure 6 it can also be seen that after the reading process is done, the read_done process that shows the reading process is done, goes high.

Figure 6 – Verification of the state transition

Therefore, it can be seen that the digital design is done correctly, and the results demonstrated in this section can verify that.

V. DISCUSSION

The results of the design show that although this is called a digital camera, the analog part of the design is inseparable from it. The reason for this is that the connection to the real world which is physical is done through the analog part of the digital camera. Therefore, it is critical to design the analog part carefully since the model of that analog design is used in the digital design. If that model does not function well, the final result would be false even though all the controls are done correctly by the digital design.

This was done in this project since it can be seen from the verification results that the circuit is operating correctly. If the analog model had a problem, no matter how accurate we designed the state transitions and control signals, we still would have false results.

VI. FUTURE WORK

One of the aspects of the project that can be improved is using a gray counter instead of a regular counter. This was ok to ignore for the purpose of this project since we could not get the ADC to work accurately that way. However, it would be a good improvement for future work.

The reason for this is that we have an analog side and a digital side for the circuit and these two are not synchronous. Therefore, we do not know when the comparator which works as the ADC unit is going to flip and this is dangerous since in the digital side, everything changes at the same time. As a result, we will not have any idea what data we have stored. Using gray coding we only change one bit every clock cycle if we have a linear ramp.

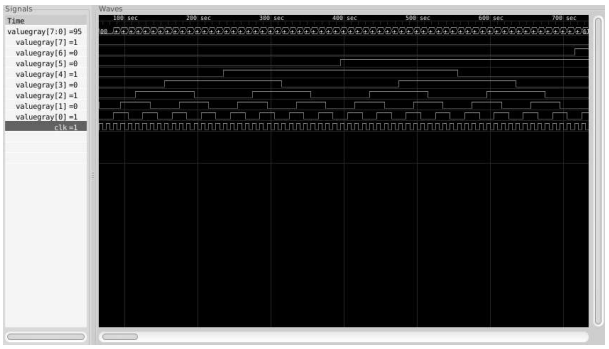

Figure 7 – Gray counter implementation

The implementation of the gray counter was done during this project and the result of the verification is shown in Figure 7. However, we did not connect this module to the actual circuit due to the fact that it would result in inaccuracy of the ADC unit in this design.

VII. CONCLUSION

In this project, we designed and implemented a four-pixel digital camera. First, we designed the analog section using a pixel sensor, a comparator, and a memory. In this section, the analog signal was received and transformed into digital bits. Then we controlled the circuit with our digital design to be able to change between different states of operation in the digital camera.

We used Ng-Spice for our analog design verification and Verilog for our digital design verification. The results of the verification showed that we were able to implement our design correctly and get the desired results.

VIII. APPENDIX

The Spice and Verilog files along with the test benches designed for each part of verification of the design is attached to the appendix of this document.

REFRENCES

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