Republic of the Philippines
BATANGAS STATE UNIVERSITY
The National Engineering University
Alangilan Campus
Golden Country Homes, Alangilan, Batangas City, Batangas, Philippines 4200
Tel Nos.: (+63 43) 425-0139 loc. 2121 / 2221
E-mail Address: ceafa@g.batstate-u.edu.ph | Website Address: http://www.batstate-u.edu.ph

College of Engineering – Department of Electrical Engineering

COMPUTER ENGINEERING PROGRAM
INTRODUCTION TO HDL
LABORATORY REPORT 5
COUNTERS

Name: Gamboa, Jave Danielle M. **Section: CpE - 3101**
Sr-Code: 23-03647

1. **Activity's Intended Learning Outcomes (ILOs)**
   At the end of this activity, the student shall be able to:
   a. **Implement and simulate** a 3-bit UP asynchronous counter and a 3-bit DOWN synchronous counter in Verilog to observe their counting sequences under clock pulses.
   b. **Analyze and verify** counter behavior using output logs and timing diagrams, highlighting differences between asynchronous and synchronous operation.
2. **Objectives of the Activity**
   The activity aims to:
   a. To reinforce understanding of **sequential circuits** and how counters are realized using flip-flops.
   b. To practice **Verilog coding** for both asynchronous and synchronous counter designs.
   c. To use a **testbench and simulation tools** to observe counting sequences and wrap-around behavior.
   d. To analyze differences in timing between asynchronous and synchronous counters.

Sample Verilog Code:

FOR DESIGN

```
module ff_ff (
  input clk,
  input rst,
  input A,
  input B,
  output reg X
);
  always @(posedge clk or posedge rst) begin
     case ({A, B})
       //Conditions
     endcase
   end
  end
```

College of Engineering – Department of Electrical Engineering

```
endmodule

module counter_des (
  input clk,
  input rst,
  output [3:0] X
);
  //Conditions
endmodule
```

FOR TEST BENCH

```
module tb_counter;
  reg clk, rst;
  wire [3:0] X;

  counter_des uut (.clk(clk), .rst(rst), .Q(Q));

  initial begin
    $dumpfile("counter.vcd"); $dumpvars;
    $display("table");

//rst

    // Generate clock pulses
//Displaying
      end
    end

    $finish;
  end
endmodule
```

Republic of the Philippines
BATANGAS STATE UNIVERSITY
The National Engineering University
Alangilan Campus
Golden Country Homes, Alangilan, Batangas City, Batangas, Philippines 4200
Tel Nos.: (+63 43) 425-0139 loc. 2121 / 2221
E-mail Address: ceafa@g.batstate-u.edu.ph | Website Address: http://www.batstate-u.edu.ph

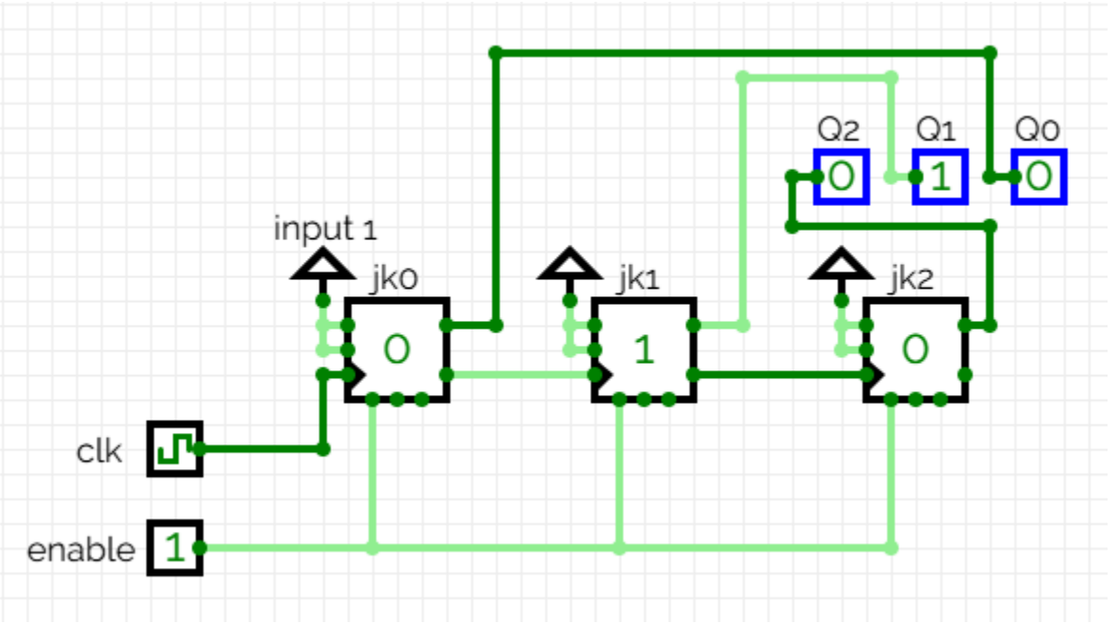
College of Engineering – Department of Electrical Engineering

----------*ASSESSMENT STARTS HERE*----------

ASSESSMENT 1: ***3-BIT UP ASYNCHRONOUS COUNTER***

A **3-bit UP asynchronous counter** that increments its count on each clock pulse, with outputs changing in a ripple fashion.

A. CIRCUIT DIAGRAM:



B. VERILOG CODE *(paste the actual code)*:
Design Code:

```
module joke_ff (
  input clk,
  input rst,
  input J,
  input K,
  output reg Q
);
  always @(posedge clk or posedge rst) begin
    if (rst)
      Q <= 0;
    else begin
      case ({J, K})
        2'b00: Q <= Q;      // No change
        2'b01: Q <= 0;      // Reset
        2'b10: Q <= 1;      // Set
        2'b11: Q <= ~Q;     // Toggle
      endcase
```

College of Engineering – Department of Electrical Engineering

```
    end
  end
endmodule

module asyncUpCounter3bit (
  input clk,
  input rst,
  output [2:0] Q
);
  joke_ff jk0 (.clk(clk),   .rst(rst), .J(1'b1), .K(1'b1), .Q(Q[0]));
  joke_ff jk1 (.clk(~Q[0]), .rst(rst), .J(1'b1), .K(1'b1), .Q(Q[1]));
  joke_ff jk2 (.clk(~Q[1]), .rst(rst), .J(1'b1), .K(1'b1), .Q(Q[2]));
endmodule
```

Testbench Code:

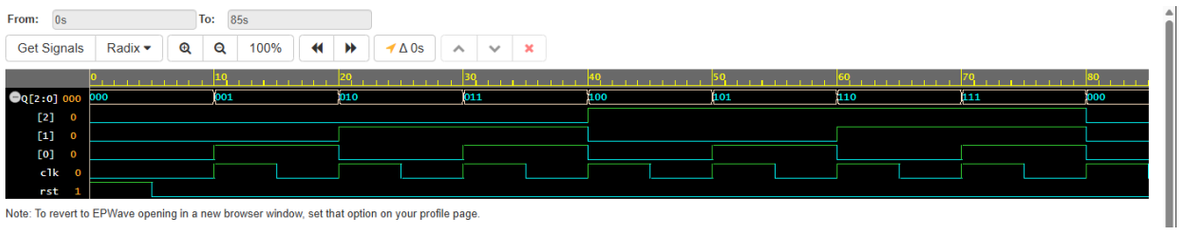
```
module tb_asyncUpCounter3bit;
  reg clk, rst;
  wire [2:0] Q;

  asyncUpCounter3bit uut (.clk(clk), .rst(rst), .Q(Q));

  initial begin
    $dumpfile("counter_3bit.vcd");
    $dumpvars;
    $display("Time | clk rst |  Q");
    $display("-----+---------+-----");

    clk = 0; rst = 1;
    #5 rst = 0; // release reset

    repeat (16) begin
      #5 clk = ~clk; // Toggle clock
      if (clk) begin // only display at posedge
        $display("%4t |  %b   %b  | %b",
          $time, clk, rst, Q);
      end
    end

    $finish;
  end
endmodule
```

College of Engineering – Department of Electrical Engineering

C. OUTPUT LOG (the output of your verilog code)

```
[2025-12-03 11:04:16 UTC] iverilog '-Wall' '-g2012' design.sv testbench.sv  && unbuffer vvp a.out
VCD info: dumpfile counter_3bit.vcd opened for output.
VCD warning: $dumpvars: Package ($unit) is not dumpable with VCD.
Time | clk rst |  Q
-----+---------+-----
  10 |  1   0  | 000
  20 |  1   0  | 001
  30 |  1   0  | 010
  40 |  1   0  | 011
  50 |  1   0  | 100
  60 |  1   0  | 101
  70 |  1   0  | 110
  80 |  1   0  | 111
testbench.sv:24: $finish called at 85 (1s)
Finding VCD file...
./counter_3bit.vcd
[2025-12-03 11:04:17 UTC] Opening EPWave...
Done
```

D. EPWave



Note: To revert to EPWave opening in a new browser window, set that option on your profile page.

E. **Activity Conclusion/Takeaways** *(Discuss what happened to the circuit and the EPWave, and your conclusions)*

In the circuit, the inputs for the clock of the flip flops excluding the first one will come from the output of the previous flipflop. For the asynchronous up counter, the inputs for clock will come from the Q inverse of the previous flip flops. The complete output of the counter is binary numbers counting up from 000 to 111.

The EPWave waveform showed that each flip-flop did not change at the same time. Only Q0 changed directly with the clock, and Q1 and Q2 followed afterward because their clock inputs depended on the previous flip-flop outputs meaning the flip-flops are not triggered simultaneously,

The asynchronous counter correctly counted from 000 to 111, but the EPWave waveform showed that the flip-flops did not update at the same time. Because each flip-flop's clock (except the first) came from the previous stage's inverted output, the bits changed one after another. This confirms the expected behavior of an asynchronous counter.

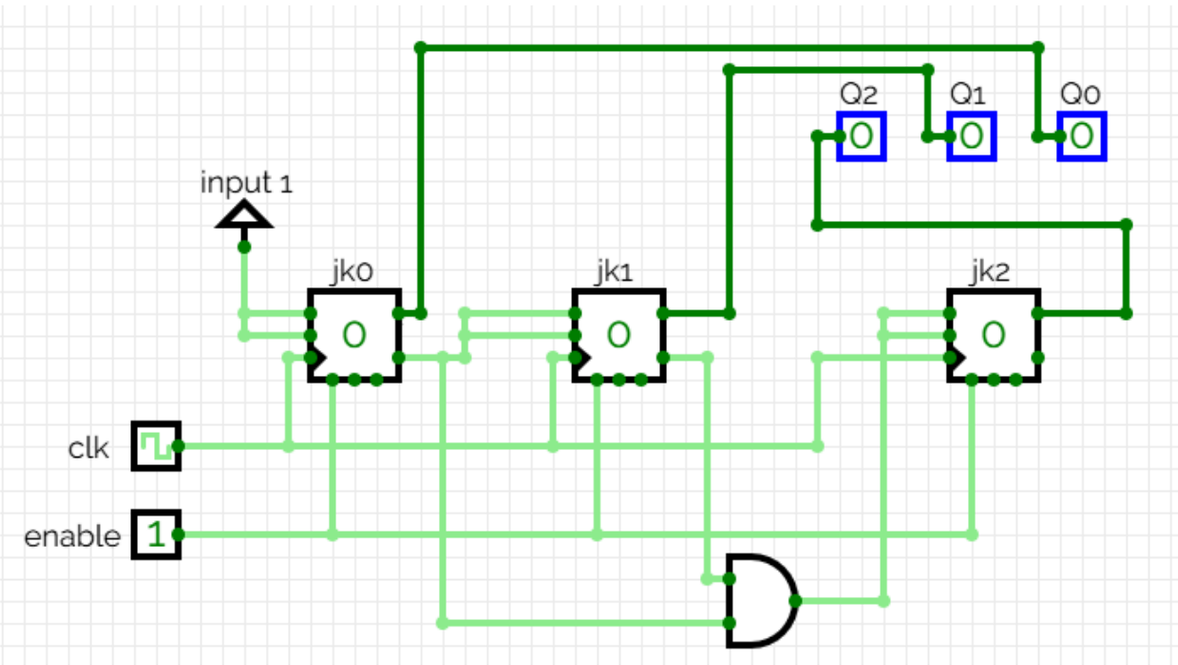
Republic of the Philippines
BATANGAS STATE UNIVERSITY
The National Engineering University
Alangilan Campus
Golden Country Homes, Alangilan, Batangas City, Batangas, Philippines 4200
Tel Nos.: (+63 43) 425-0139 loc. 2121 / 2221
E-mail Address: ceafa@g.batstate-u.edu.ph | Website Address: http://www.batstate-u.edu.ph

College of Engineering – Department of Electrical Engineering

ASSESSMENT 2: ***3-BIT DOWN SYNCHRONOUS COUNTER***

A **3-bit DOWN synchronous counter** that decrements its count on each clock pulse, with all flip-flops triggered simultaneously.

A. CIRCUIT DIAGRAM:



B. VERILOG CODE *(paste the actual code)*:

Design Code:

```
module joke_ff (
  input clk, input rst,
  input J, input K,
  output reg Q
);
  always @(posedge clk or posedge rst) begin
    if (rst) Q <= 0;
    else begin
      case ({J,K})
        2'b00: Q <= Q;      // no change
        2'b01: Q <= 0;      // reset
        2'b10: Q <= 1;      // set
        2'b11: Q <= ~Q;     // toggle
      endcase
    end
  end
endmodule
```

College of Engineering – Department of Electrical Engineering

```
module syncDownCounter3bit (
  input clk, input rst,
  output [2:0] Q
);

  joke_ff jk0 (.clk(clk), .rst(rst), .J(1'b1), .K(1'b1), .Q(Q[0]));
  joke_ff jk1 (.clk(clk), .rst(rst), .J(~Q[0]), .K(~Q[0]), .Q(Q[1]));
  joke_ff jk2 (.clk(clk), .rst(rst), .J(~Q[0] & ~Q[1]), .K(~Q[0] & ~Q[1]), .Q(Q[2]));
endmodule
```

Testbench Code:

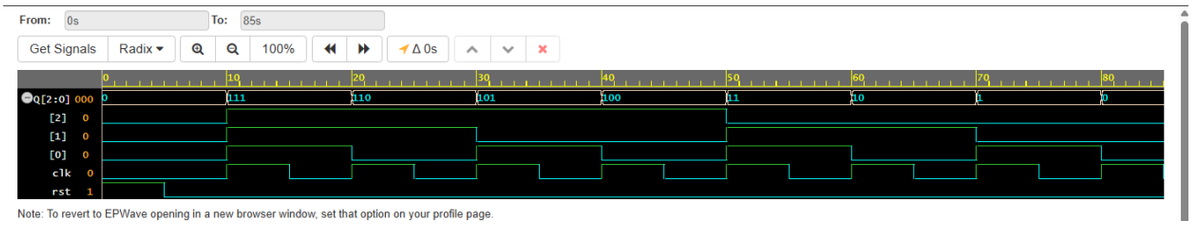
```
module tb_syncDownCounter3bit;
  reg clk, rst;
  wire [2:0] Q;

  syncDownCounter3bit uut (.clk(clk), .rst(rst), .Q(Q));

  initial begin
    $dumpfile("counter_3bit.vcd");
    $dumpvars;
    $display("Time | clk rst |  Q");
    $display("-----+---------+-----");

    clk = 0; rst = 1;
    #5 rst = 0; // release reset

    repeat (16) begin
      #5 clk = ~clk; // toggle clock
      if (clk) begin // only display at posedge
        $display("%4t |  %b   %b  | %b",
          $time, clk, rst, Q);
      end
    end

    $finish;
  end
endmodule
```

College of Engineering – Department of Electrical Engineering

C. OUTPUT LOG (the output of your verilog code)

```
[2025-12-03 11:03:46 UTC] iverilog '-Wall' '-g2012' design.sv testbench.sv  && unbuffer vvp a.out
VCD info: dumpfile counter_3bit.vcd opened for output.
VCD warning: $dumpvars: Package ($unit) is not dumpable with VCD.
Time | clk rst |  Q
-----+---------+-----
  10 |  1   0  | 000
  20 |  1   0  | 111
  30 |  1   0  | 110
  40 |  1   0  | 101
  50 |  1   0  | 100
  60 |  1   0  | 011
  70 |  1   0  | 010
  80 |  1   0  | 001
testbench.sv:24: $finish called at 85 (1s)
Finding VCD file...
./counter_3bit.vcd
[2025-12-03 11:03:47 UTC] Opening EPWave...
Done
```

D. EPWave



E. **Activity Conclusion/Takeaways** *(Discuss what happened to the circuit and the EPWave, and your conclusions)*

In the circuit, the inputs for jk1 and jk2 depend on the previous outputs. JK of jk1 is the Q inverse of jk0. JK of jk2 is both the Q inverse of jk0 combined by “and” gate. The least significant bit will be coming from jk0 and the most significant bit will be from jk2. The complete output of the counter is binary numbers counting down from 111 to 000.

The EPWave waveform clearly showed that all three flip-flops updated their outputs at the same moment, because they shared the same clock input. It also showed that the logic expressions controlling JK inputs worked correctly where each flip-flop toggled only when the conditions for down-counting were met.

The synchronous down counter correctly counted from 111 down to 000, with jk1 and jk2 toggling based on the required logic derived from the previous outputs. The EPWave confirmed that all flip-flops updated simultaneously since they shared the same clock, and the JK logic activated only under the proper down-counting conditions. This shows the coordinated behavior expected from a synchronous counter.

Republic of the Philippines
BATANGAS STATE UNIVERSITY
The National Engineering University
Alangilan Campus
Golden Country Homes, Alangilan, Batangas City, Batangas, Philippines 4200
Tel Nos.: (+63 43) 425-0139 loc. 2121 / 2221
E-mail Address: ceafa@g.batstate-u.edu.ph | Website Address: http://www.batstate-u.edu.ph

College of Engineering – Department of Electrical Engineering

CRITERIA	SCORE
Code	
The code is completely functional and responds correctly producing the correct outputs. **(5 Points)**	
The code is correct regarding syntax but required output is incorrect. **(3 Points)**	
The code has several syntax errors. **(1 Points)**	
Circuit Diagram	
Diagram is complete, clear, and accurately reflects counter logic and flip-flop connections. **(5 Points)**	
Diagram is mostly correct but has minor errors or missing labels. **(3 Points)**	
Diagram is unclear, incomplete, or incorrect. **(1 points)**	
Overall Work	
Student's work shows complete understanding of problem and all requirements. Able to explain entire program and design correctly as it is. **(10 Points)**	
Student's work shows understanding of problem and most requirements. Able to explain some program and design. **(7 Points)**	
Student's work shows slight understanding of problem and requirements. Unable to explain program and design. **(5 Points)**	
TOTAL SCORE:	
Percentage Score= (Total Score/20) * 100	
Other Comments:	