

CSARCH1 Design Exercise #2
S14 - Group 3

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Submitted to:
The best CSARCH1 professor *Sir Carlo Adriano*
That will definitely accept our late submission 😊

March 23, 2024

Dice Game

I. Introduction

BoBing (also known as Bo Bing or Pua Tiong Chiu) is a traditional Chinese dice game typically played during the Mid-Autumn Festival. It involves rolling dice and matching the resulting combinations to win prizes. **Below are the objectives of the game as specified in the [specification](#):**

Input: Each dice D_i is represented as a 3-bit input. There are 6 dice ($D1, D2, D3, D4, D5, D6$) in BoBing.

Output: The output consists of $P1, P2, P3, P4, P5, P6$ representing (1st Prize, 2nd Prize, 3rd Prize, 4th Prize, 5th Prize, 6th Prize). Only one LED should be lit up when a valid prize is won. If any of the dice is invalid, all the lights will light up.

Limitations: You can use logic gates, multiplexers and decoders.

II. Truth Table (Dice Table) & Winning Requirements

Taken from the [specifications](#), there are 2 columns in the table; with the first being '3-bit input D' represents the 3-bit binary input to the circuit labeled as "D", while the second column 'Dice Value' displays the decimal value equivalent to the 3-bit binary input. Each row shows a different combination of 0s and 1s for the 3-bits.

3-bit input D	Dice Value
000	Invalid
001	1
010	2
011	3
100	4
101	5
110	6
111	Invalid

From the dice inputs up above, the win requirements for each prize will be shown below:

Win requirements		<i>Note:</i> The subscript denotes number of times dice value is rolled X and Y means any 2 different dice values
Prize	Requirements	Requirements (Mathematical Notation)
1st prize	Any 4 4-faced dice, or 5 of any number	$1_5 + 2_5 + 3_5 + 4_4 + 5_5 + 6_5$
2nd prize	All numbers 1-6, or 3 of one number and 3 of another number	$1_1 2_1 3_1 4_1 5_1 6_1 + X_3 Y_3$
3rd prize	3 4-face dice + 3 of any number	4_3
4th prize	4 of the same number except four	$1_4 + 2_4 + 3_4 + 5_4 + 6_4$
5th prize	2 4-face dice + 4 of any number	4_2
6th prize	1 4-face die + 5 of any number	4_1

III. Circuit Verse

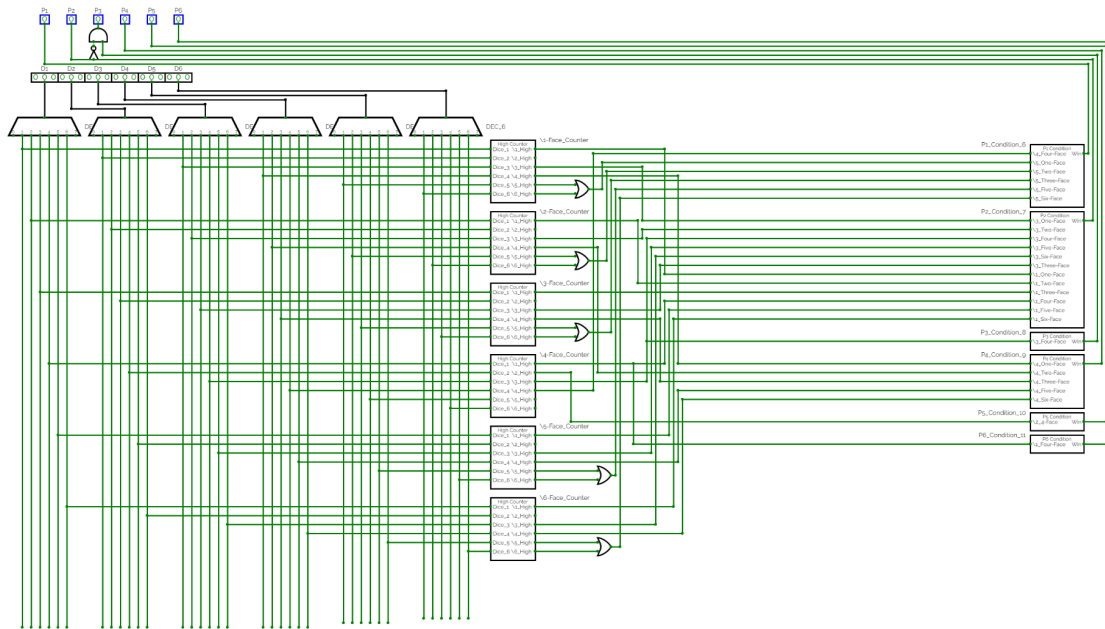


Figure 1. Full Image of Circuitverse Diagram

Element Usage Report from our diagram:

- Input - 38 times
- OrGate - 8 times
- Output - 18 times
- Adder - 4 times
- Splitter - 1 times
- Decoder - 7 times
- ConstantVal - 1 times
- AndGate - 3 times
- NorGate - 1 times
- NotGate - 2 times
- XnorGate - 1 times
- SubCircuit - 12 times

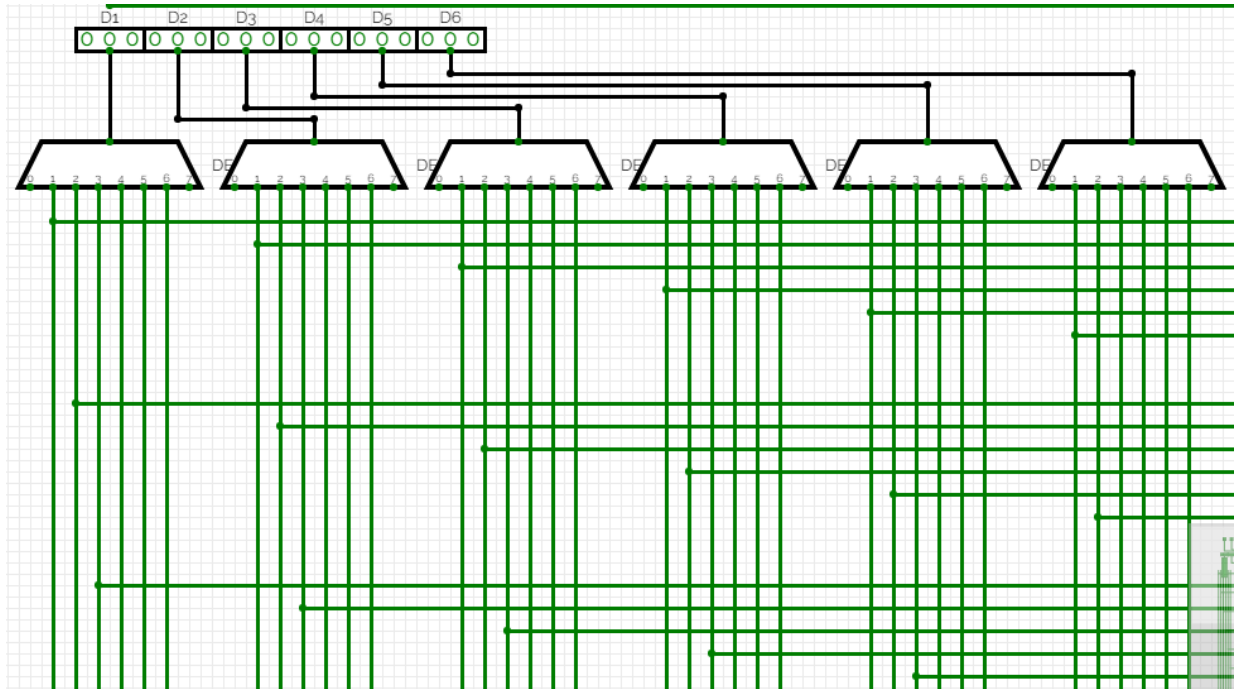


Figure 1.1. Dices connected to respective Decoders

All six dice are connected to their respective decoder chips, these chips convert the binary code from the dice roll (0s and 1s) into a decimal output representing the number rolled on that particular chip.

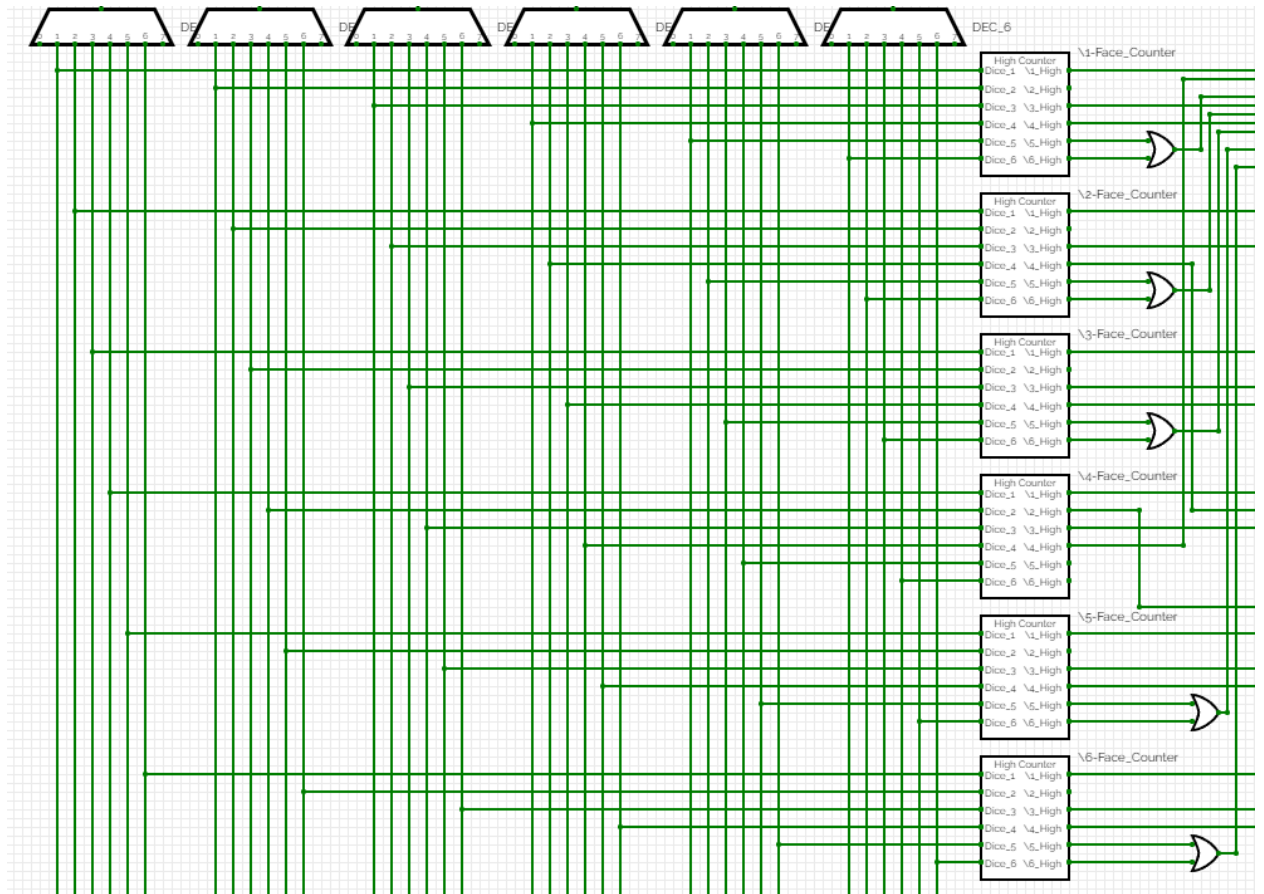


Figure 1.2. 6 Decoders connected to 6 Counters

1 to 8 decoders were used to extract the corresponding decimal value from the 3 bit input. Output values 1-6 from each are then fed to the sub circuit High Counter. It counts how many of the inputs are high (1) and gives a high signal on its output equivalent to the count of high signals in the input.

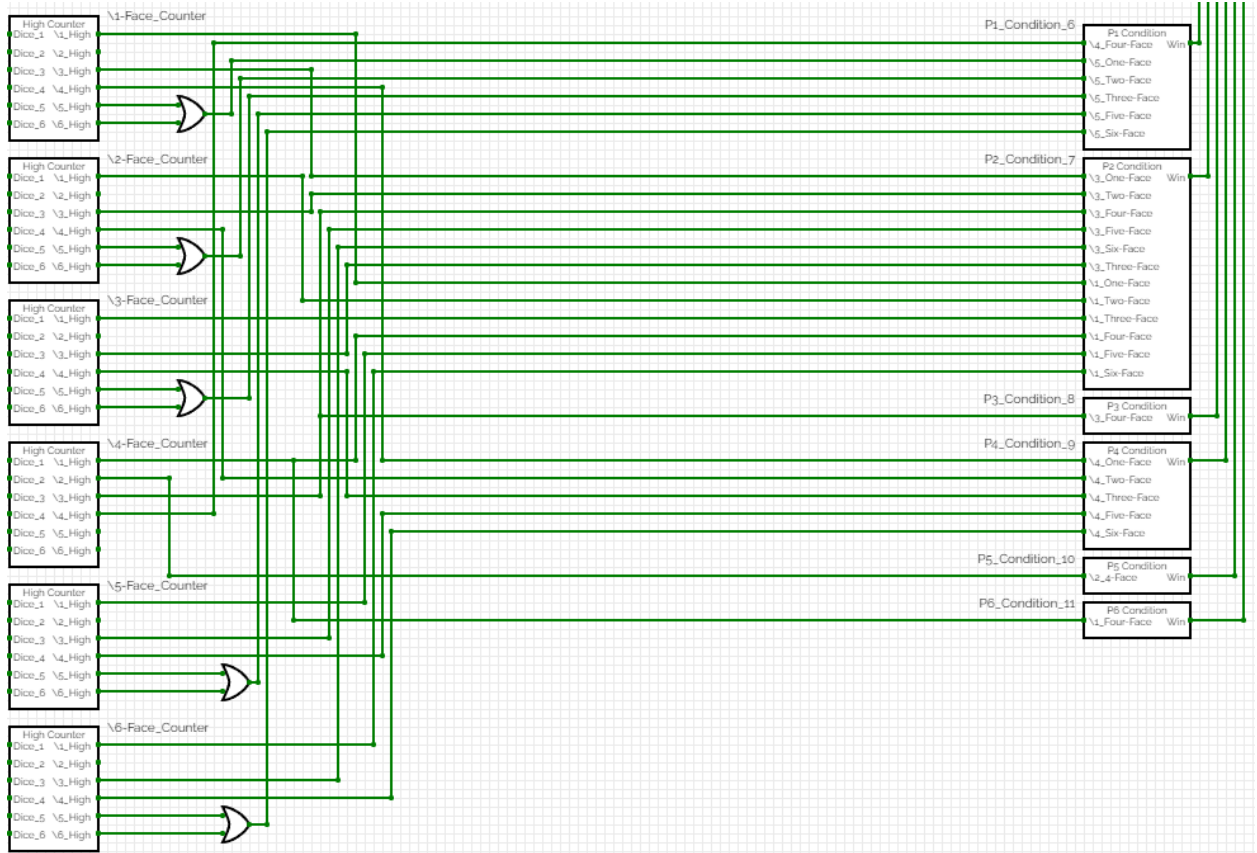


Figure 2. Counters connected to check Prize Conditions

High counter outputs are then fed to sub circuits containing different prize conditions. Or gates are used on some conditions where counts greater or equal than the specified ones can be considered. Once processed inside each prize condition sub circuit, respective prize output will light up showing the user which prize they got.

Different circuits other than “Main”

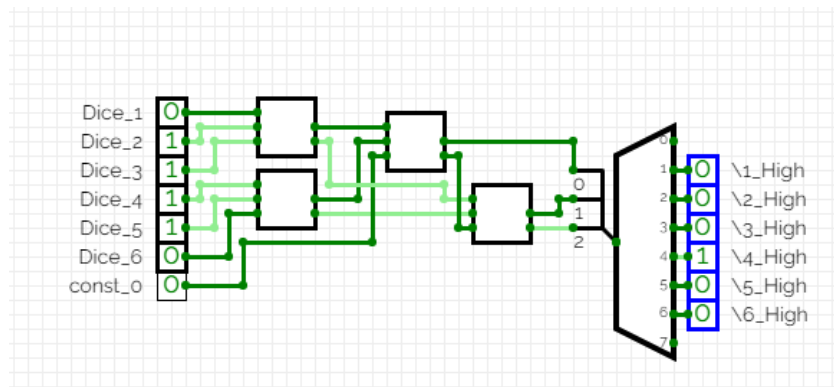


Figure 2.1 High Counter

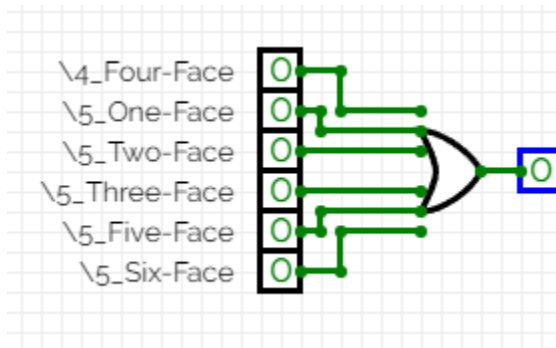


Figure 2.2 Prize 1 Condition

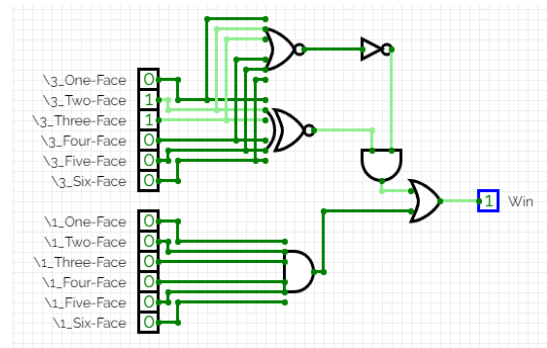


Figure 2.3 Prize 2 Condition

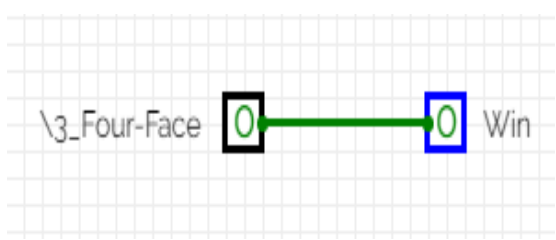


Figure 2.4 Prize 3 Condition

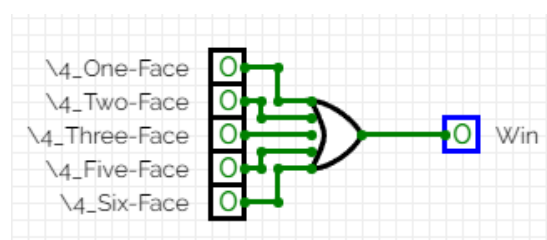


Figure 2.5 Prize 4 Condition

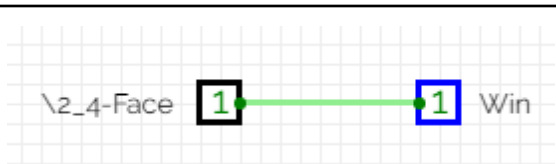


Figure 2.6 Prize 5 Condition

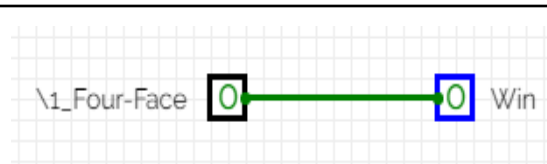
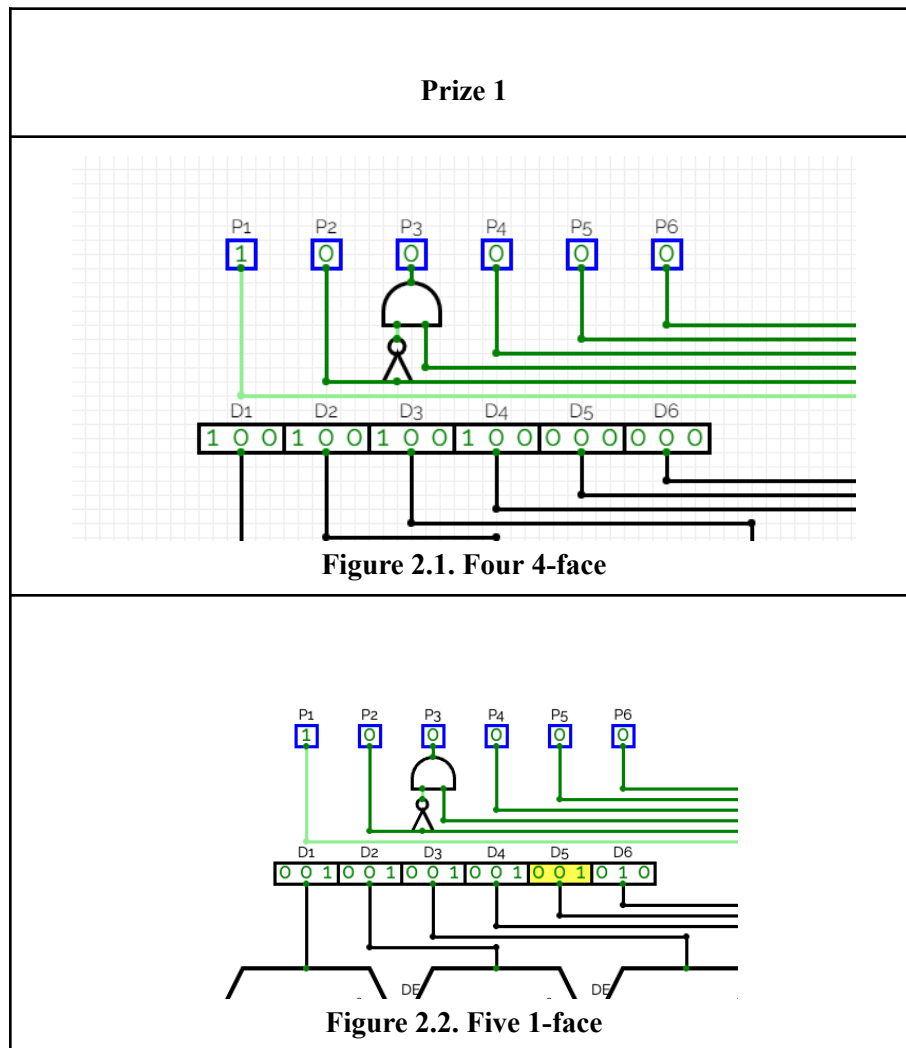


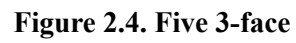
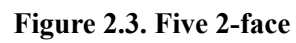
Figure 2.7 Prize 6 Condition

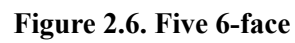
IV. Prize Outputs

All 16 prizes were organized taken by our Circuit Verse diagram in descending order from P1 - P6.

Prize 1: 5 approaches
Prize 2: 2 approaches
Prize 3: 1 approach
Prize 4: 5 approaches
Prize 5: 1 approach
Prize 6: 1 approach







The diagram illustrates a combinational logic circuit for a 6-bit adder. At the top, six inputs labeled P1 through P6 are shown, each with a green square containing a 0 or 1. P1=0, P2=1, P3=0, P4=0, P5=0, P6=0. A carry-in input (represented by a stick figure) is also shown. The circuit uses AND gates to generate carry signals (D1-D6) and OR gates to generate sum signals (D1-D6). The output is a 6-bit register with the value 001010. Below the register, three 7-bit adders are shown, each with inputs 1 through 7 and a carry-in input.

Figure 2.7. All numbers (1,2,3,4,5,6)

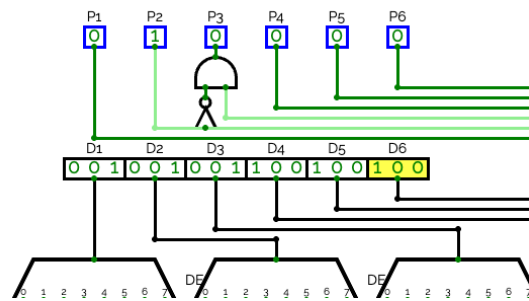


Figure 2.8. Three of a number, and three of another number

Prize 3

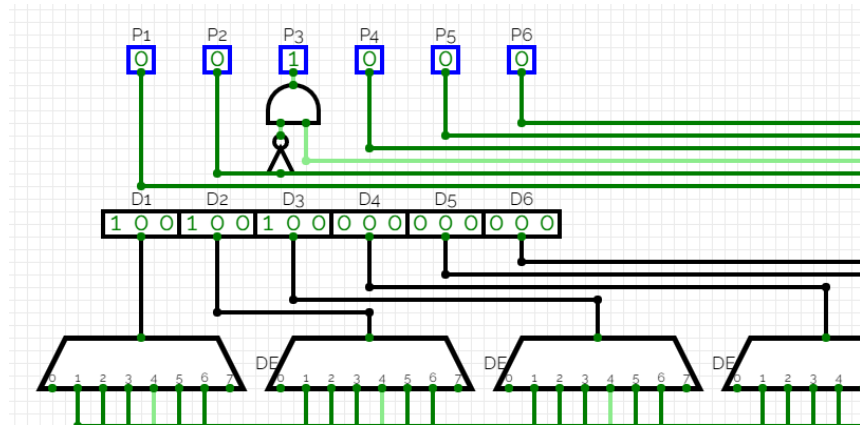


Figure 2.9. Three 4-face, and three of another number

Prize 4

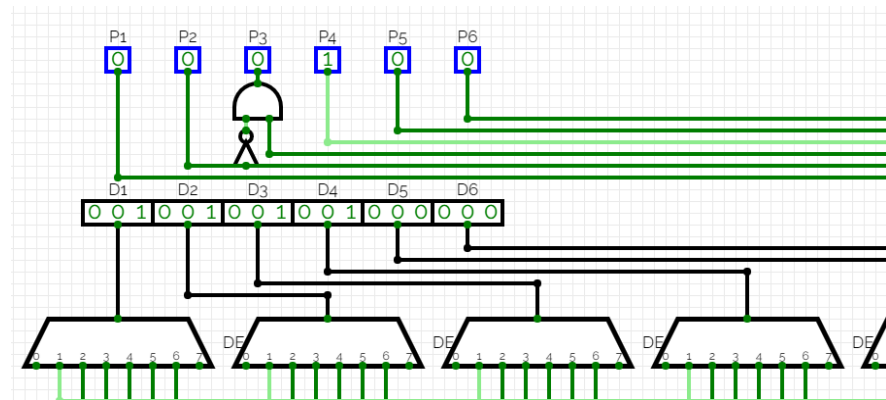


Figure 2.10. Four 1-face

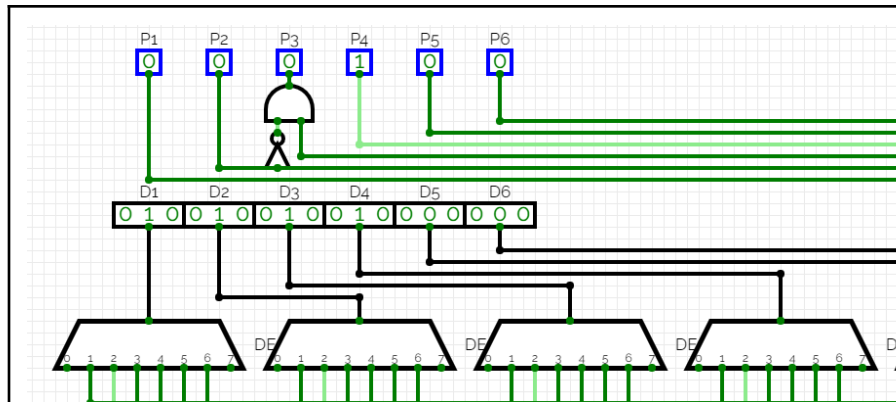


Figure 2.11. Four 2-face

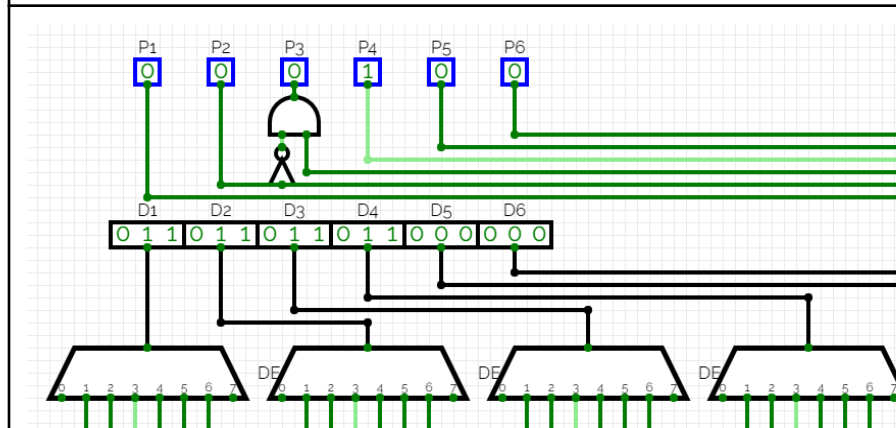


Figure 2.12. Four 3-face

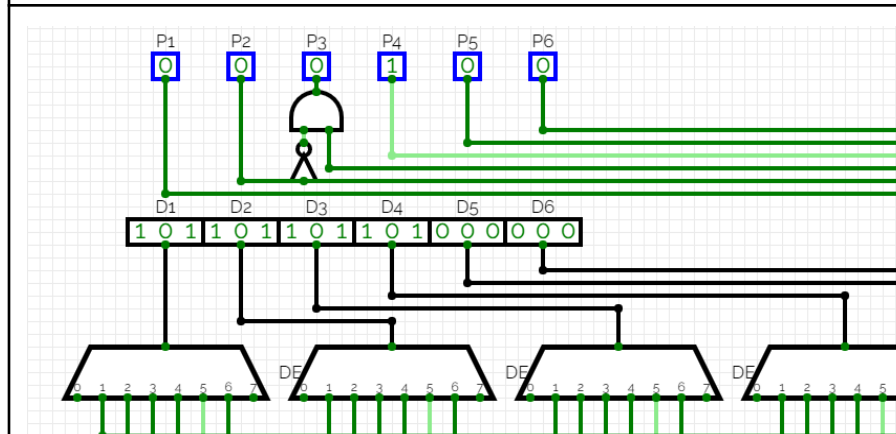
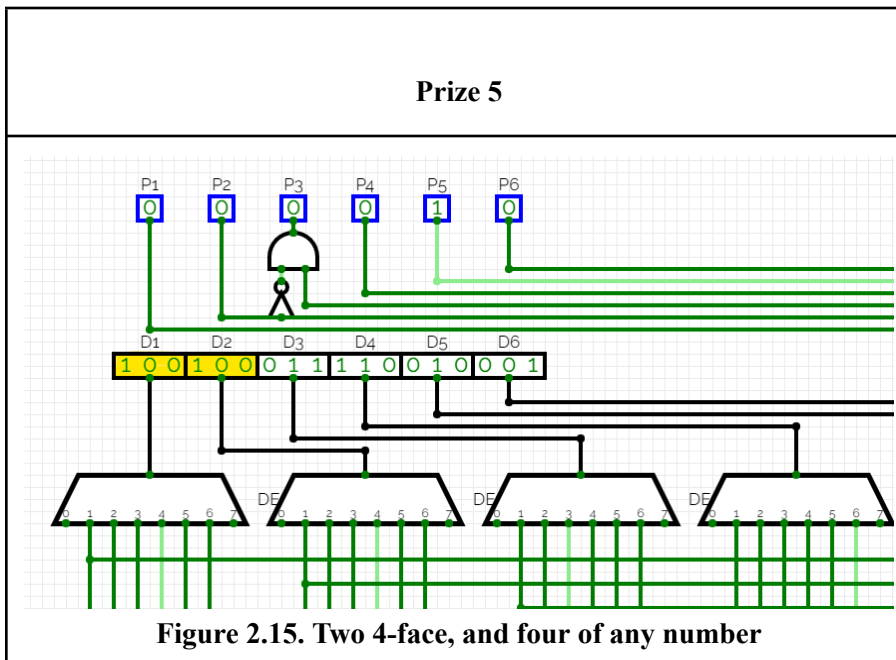
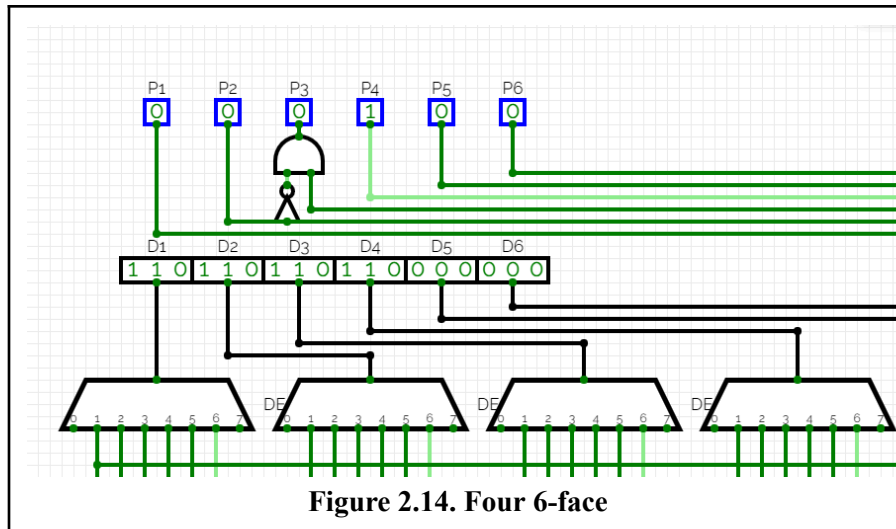


Figure 2.3. Four 5-face



Prize 6

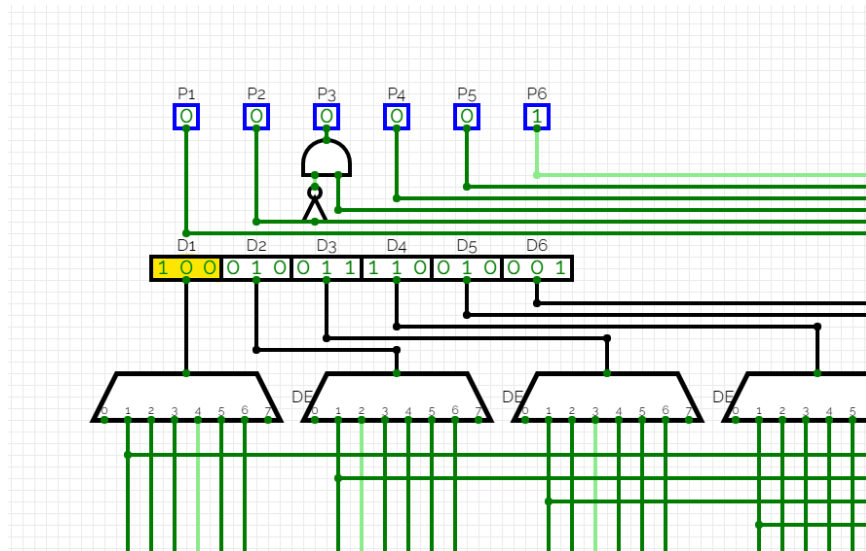


Figure 2.16. One 4-face, and five of any number