4.3.1

Without:

I-Mem, Reg, Mux, ALU, D-Mem, Mux

Cycle time = 400 + 200 + 30 + 120 + 350 + 30 = **1130 ps**

With:

Cycle time = 1130 + 300 = **1430 ps**

4.3.2

$$speed\ up = \frac{execution\ time\ before\ improvement}{execution\ time\ after\ improvement} = \frac{1130}{0.95 * 1430} = \mathbf{0.83}$$

4.3.3

It has three MUX and two ADD units

Cost without improvement:

Cost = 1000 + 2*30 + 3 * 10 + 100 + 200 + 2000 + 500 = 3890

Cost with improvement:

Cost = 3890 + 600 = 4490

4490/ 3890 = 1.15

Performance ratio = 1.15/0.83 = **1.39**

4.4.1

200 ps since I-Mem = 200ps

4.4.2

IMem, Sign extend, shift left, add, Mux

Cycle time = 200 + 15 + 10 + 70 + 20 = **315 ps**

4.4.3

IMem, Reg, Mux, ALU, Mux

Cycle-time = 200 + 90 + 20 + 90+ 20 = **420 ps**

4.4.4

All instructions except jump instructions that are pc relative

4.4.5

Jump instruction

4.4.6

Now we need an ALU and register write process, which result in

Cycle time = 420 + 90 = 510 ps

This will be the critical path because it is the longest time to execute these instructions

4.7.1

Sign-extension: 0000 0000 0000 0000 0000 0000 0001 0100

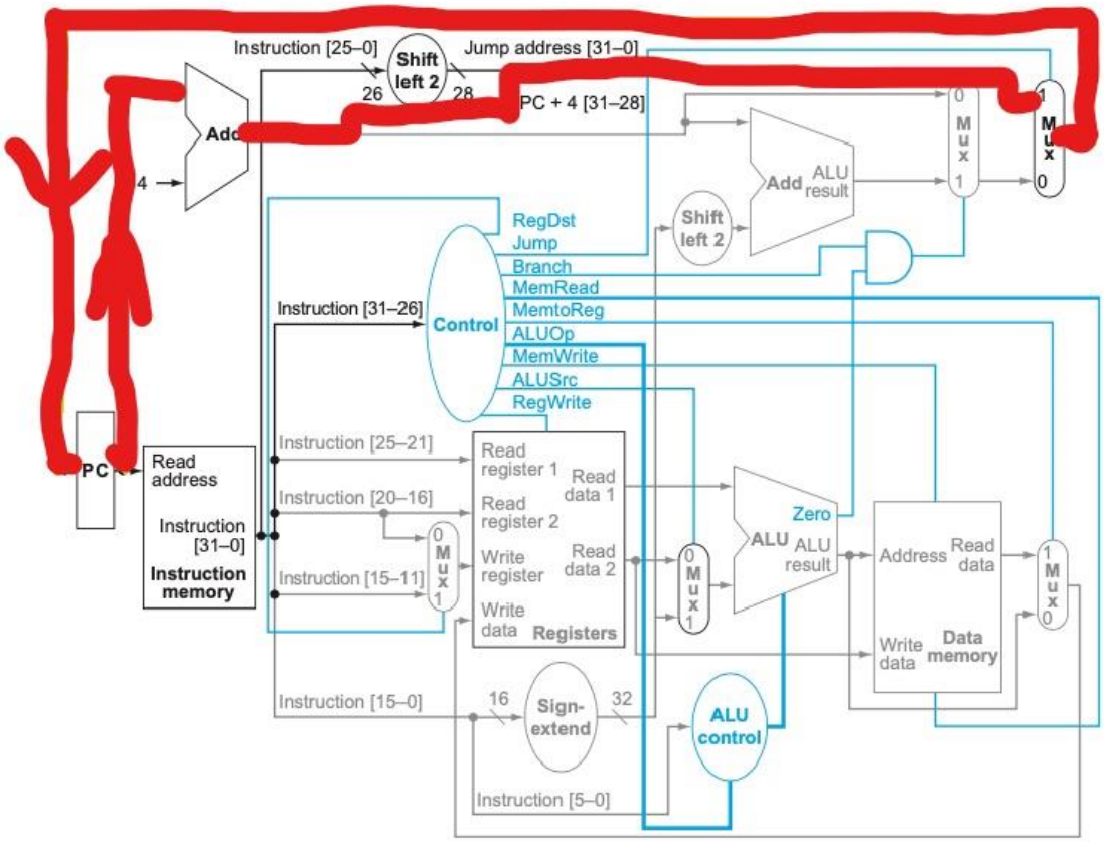
Shift to left 2: 0001 1000 1000 0000 0000 0101 0000

4.7.2

ALUop = 00 (least significant 2 bits)

Instruction = 010100

4.7.3



4.7.4

Write register Mux: 2 or 0, not used

ALU Mux: 20 (0001 0100)

Brank and jump Mux: PC + 4

ALU/Mem Mux: write register Mux is not used, so it contains X

4.7.5

ALU unit: -3 and 20

Add (branch unit): PC + 4 and 80

Add (PC): PC and 4

4.7.6

Read register 1: 0011, **3**

Read register 2: 0010, **2**

Write data: X

Write register: X (2 or 0)

Register write: 0

4.8.1

Pipelined: **350 ps**

Non pipelined: 250 + 350 + 150 + 300 + 200 = **1250 ps**

4.8.2

Pipelined:

LW uses all 5 stages

350 * 5 = **1750 ps**

Non pipelined:

1250 ps

4.8.3

Split the longest stage will reduce cycle time, so we want to split **ID stage**.

New clock-cycle: **300 ps**

4.8.4

Count LW and SW instruction

Utilization of data memory = 20% + 15% = **35 % of the clock cycle**

4.8.5

Count ALU and LW instruction

Utilization of write Register port = 20% + 45% = **65% of the clock cycle**